N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} 60V
- I_D 350mA
- $R_{DS(ON)}$(at V_{GS}=10V) 1000mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) 1400mΩ

General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Low input Capacitance
- Fast Switching Speed
- Low Input / Output Leakage
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V	-	-	1	μA
		V_{DS}=60V, V_{GS}=0V, Tj=150	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±30V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.6	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=350mA	-	730	1000	mΩ
		V_{GS}=4.5V, I_D=200mA	-	890	1400	
Diode Forward Voltage	V_{SD}	I_S=350mA, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	20	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	350	mA
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=30V, V_{GS}=0V, f=1MHz	-	34	-	pF
Output Capacitance	C_{oss}		-	6	-	
Reverse Transfer Capacitance	C_{rss}		-	2	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=30V, I_D=1A	-	1.7	-	nC
Gate-Source Charge	Q_{gs}		-	0.57	-	
Gate-Drain Charge	Q_{gd}		-	0.3	-	
Reverse Recovery Charge	Q_{rr}	I_F=1A, di/dt=100A/us	-	4	-	nC
Reverse Recovery Time	t_{rr}		-	14	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=30V, I_D=1A R_{GEN}=3Ω	-	4	-	ns
Turn-on Rise Time	t_r		-	19	-	
Turn-off Delay Time	$t_{D(off)}$		-	12	-	
Turn-off fall Time	t_f		-	24	-	

A. Repetitive Rating: Repetita2

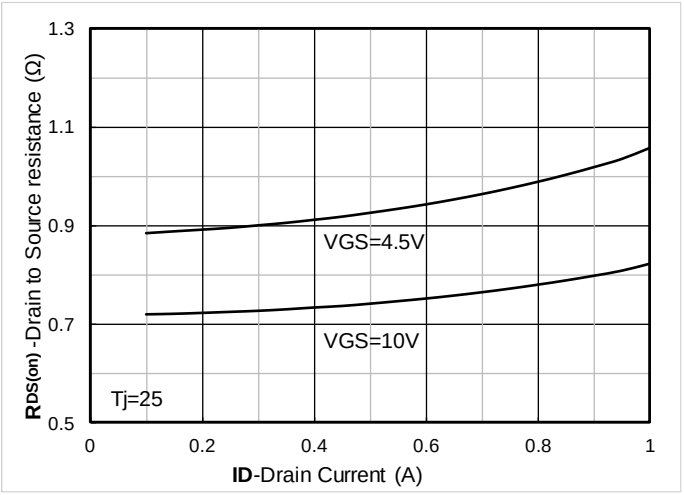

Figure 7. $R_{DS(on)}$ VS Drain Current

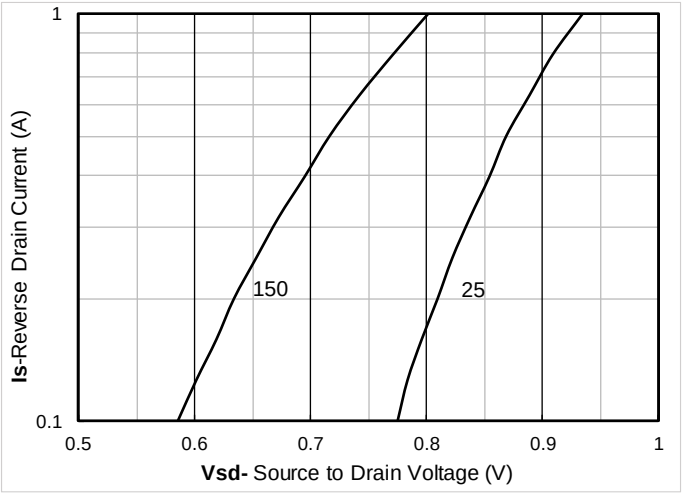

Figure 8. Forward characteristics of reverse diode

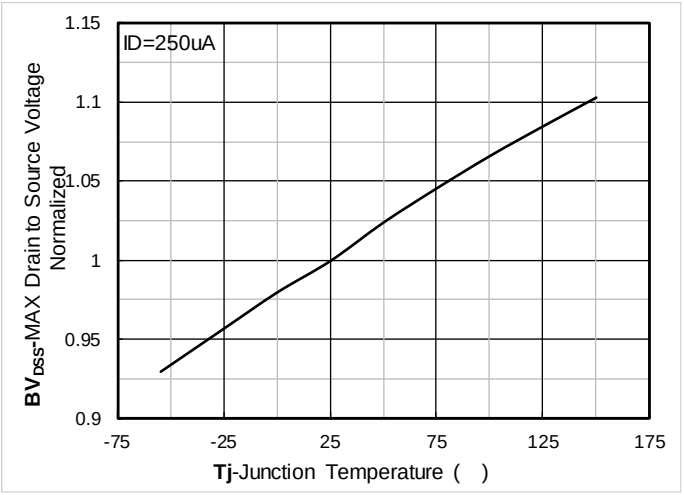

Figure 9. Normalized breakdown voltage

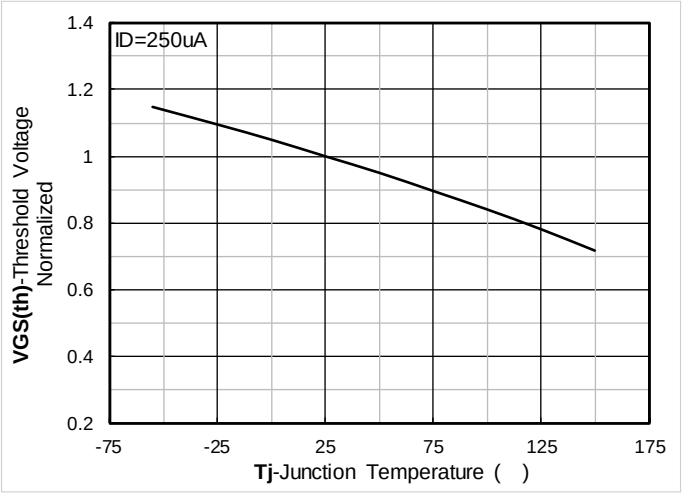

Figure 10. Normalized Threshold voltage

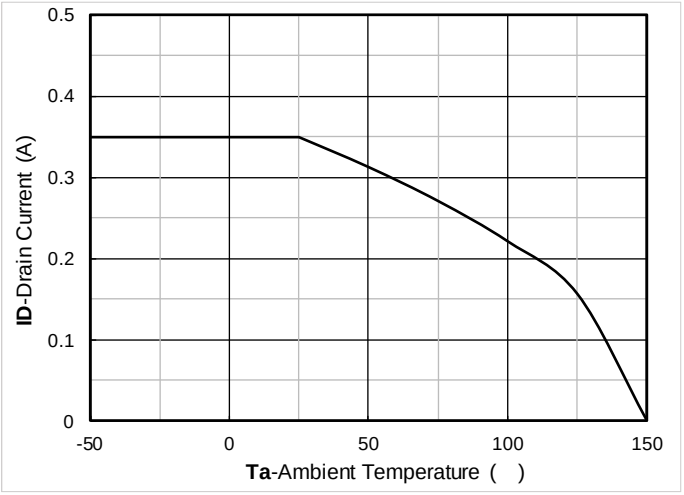

Figure 11. Current dissipation

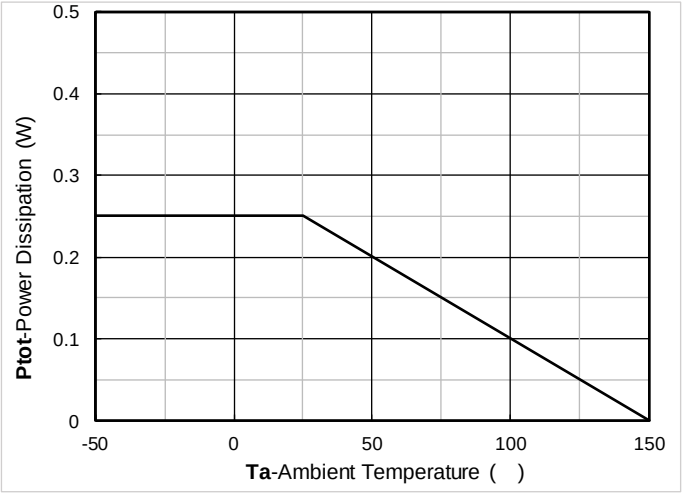

Figure 12. Power dissipation

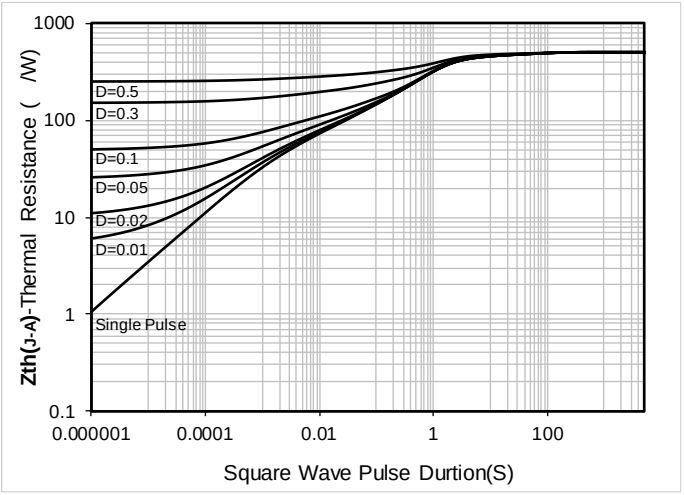

Figure 13. Maximum Transient Thermal Impedance

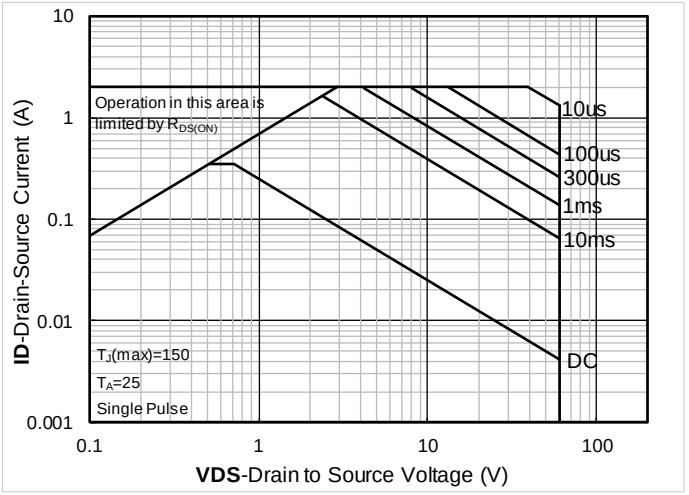

Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

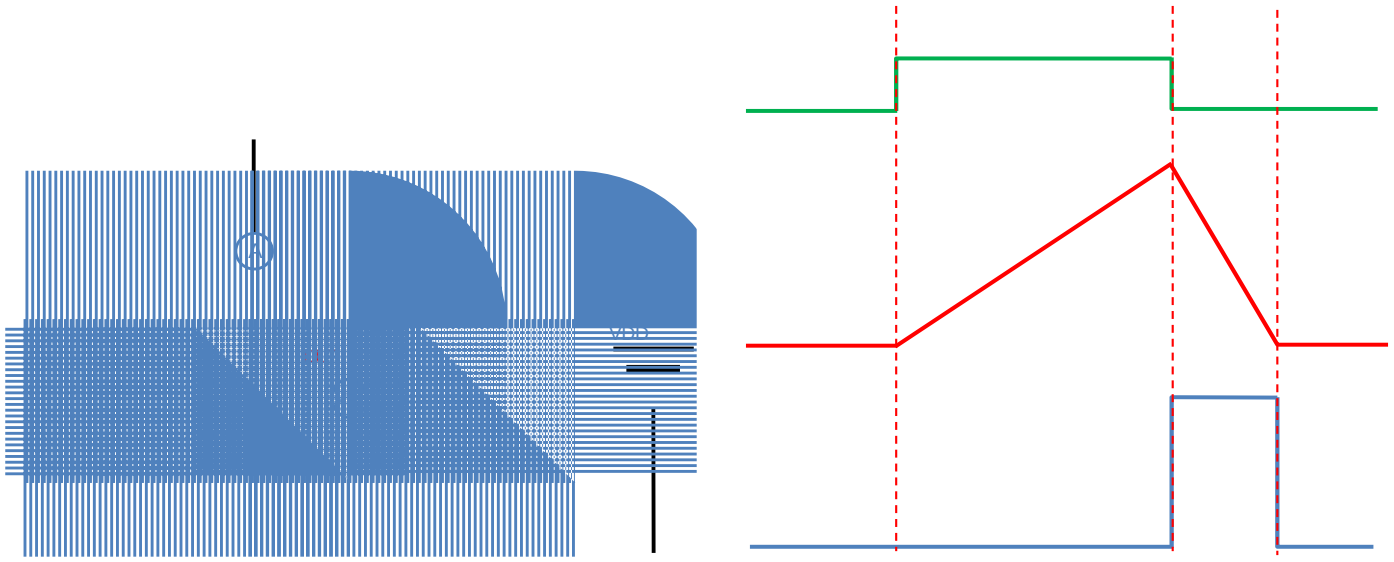

Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

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