



BSS123T

Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
		$V_{DS}=100V, V_{GS}=0V, T_J=150$	-	-	100	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=200mA$	-	2.4	3.4	
		$V_{GS}=4.5V, I_D=200mA$	-	2.65	3.6	
Diode Forward Voltage	V_{SD}	$I_S=200mA, V_{GS}=0V$	-	-	1.2	V
Gate resistance	R_G	$f=1MHz,$	-	5.5	-	
Maximum Body-Diode Continuous Current	I_S		-	-	200	mA
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V, f=1MHz$	-	33	-	pF
Output Capacitance	C_{oss}		-	3.5	-	
Reverse Transfer Capacitance	C_{rss}		-	1	-	
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=50V, I_D=1A$	-	1.8	-	nC
Gate-Source Charge	Q_{gs}		-	0.6	-	
Gate-Drain Charge	Q_{gd}		-	0.3	-	
Reverse Recovery Charge	Q_{rr}	$I_f=1A, di/dt=100A/us$	-	6	-	nC
Reverse Recovery Time	t_{rr}		-	20	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=50V, I_D=1A$ $R_{GEN}=3$	-	4	-	ns
Turn-on Rise Time	t_r		-	20	-	
Turn-off Delay Time	$t_{D(off)}$		-	7	-	
Turn-off fall Time	t_f		-	31	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. P_d is based on max. junction temperature, using junction-case thermal resistance.

C. The value of R_{JA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with $T_A=25$. The maximum allowed junction temperature of 150. The value in any given application depends on the user's specific board design.



Typical Electrical and Thermal Characteristics Diagrams

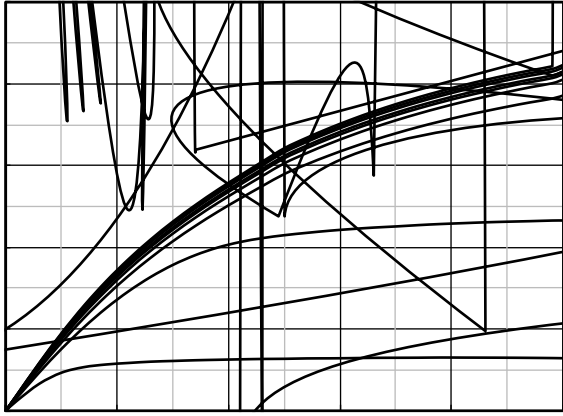


Figure 1. Output Characteristics

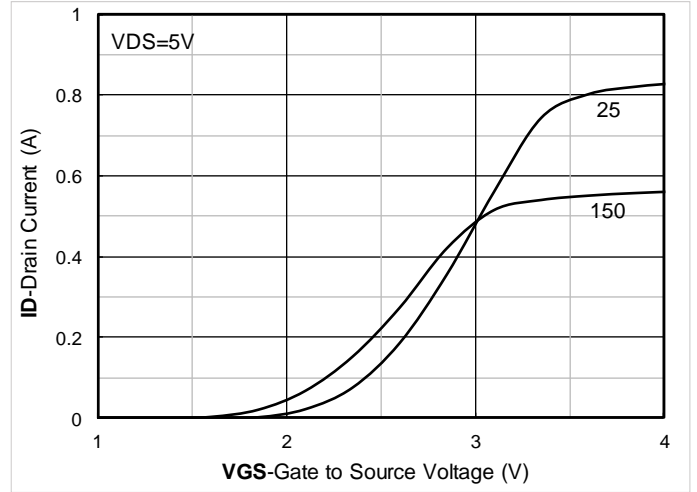


Figure 2. Transfer Characteristics

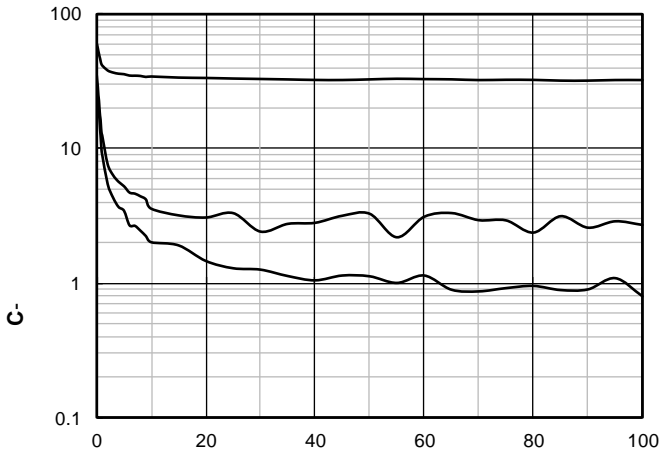


Figure 3. Capacitance Characteristics

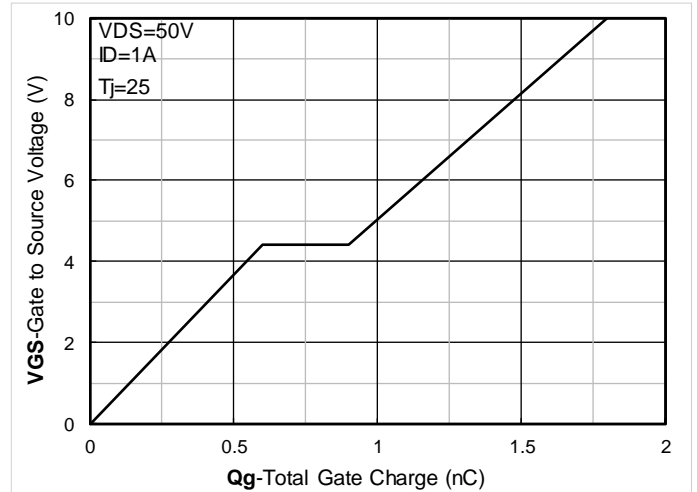


Figure 4. Gate Charge

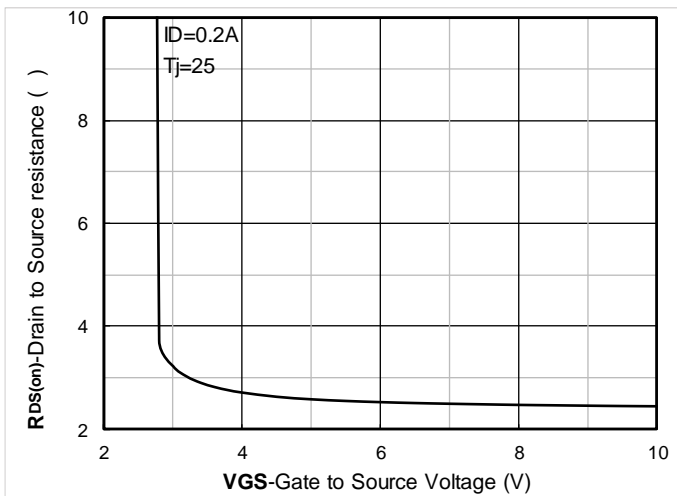


Figure 5. On-Resistance VS Gate to Source Voltage

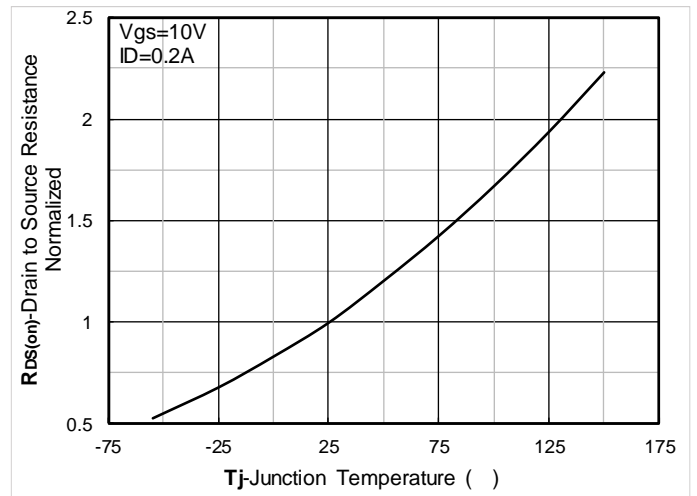


Figure 6. Normalized On-Resistance



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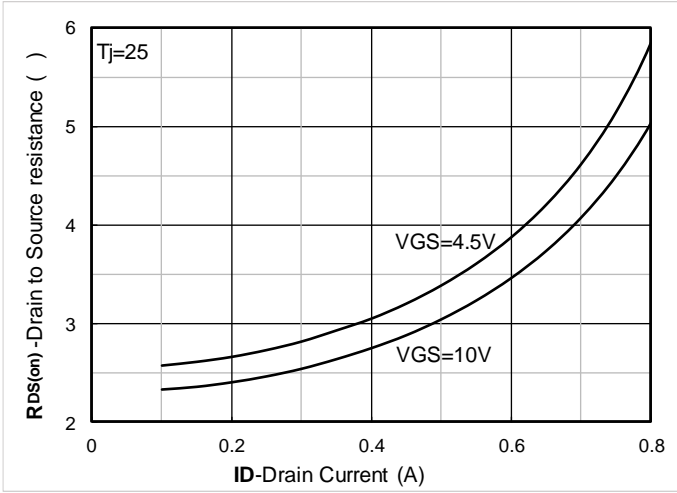


Figure 7. $R_{DS(on)}$ VS Drain Current

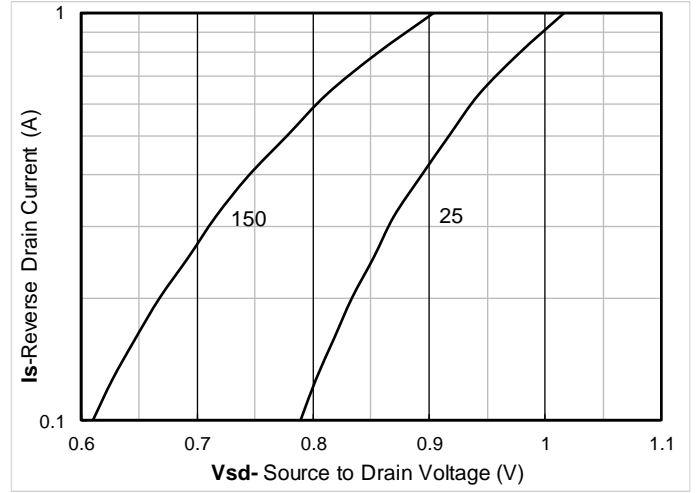


Figure 8. Forward characteristics of reverse diode

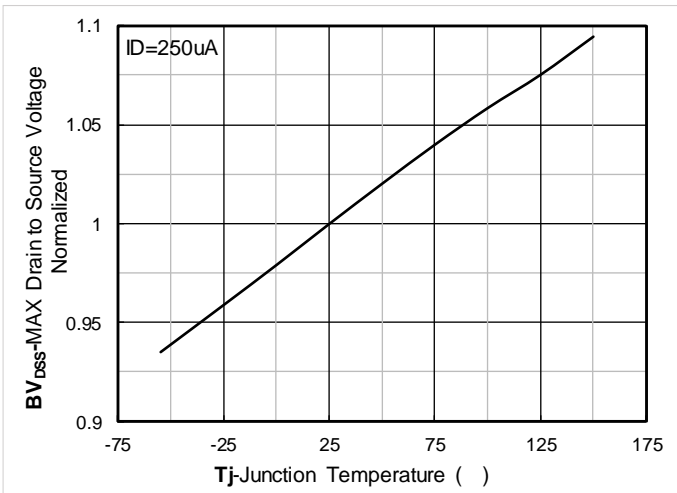


Figure 9. Normalized breakdown voltage

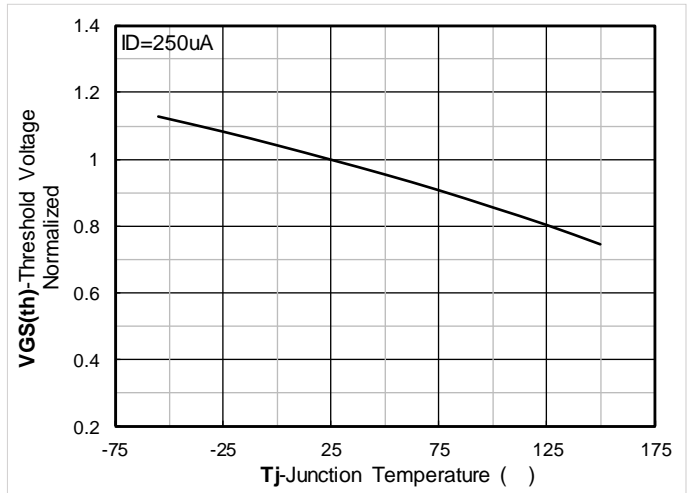


Figure 10. Normalized Threshold voltage

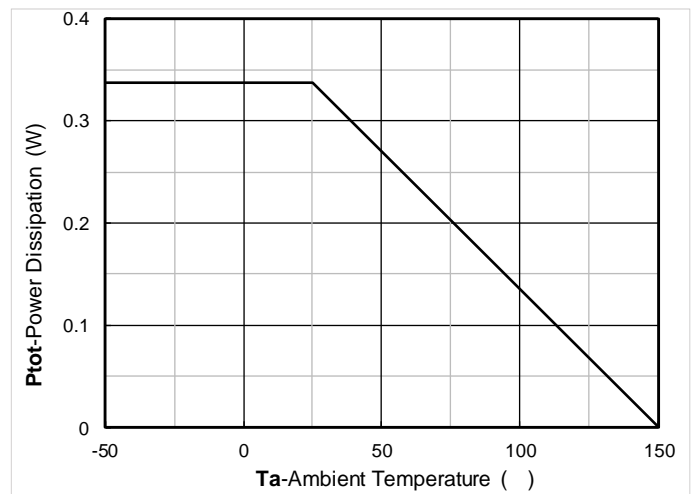
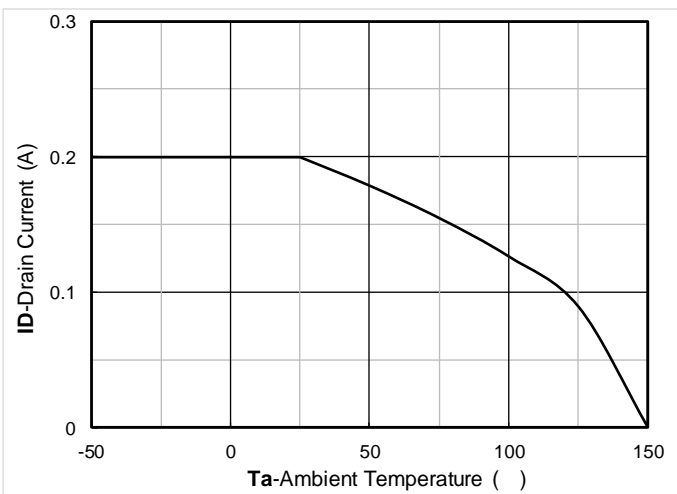


Figure 11. Current diss0 g G -0.00888 Tc(.)TJETQq0.000008882 0 596.04 842.04 reW*7 10n2402.82 337.01 Tm0

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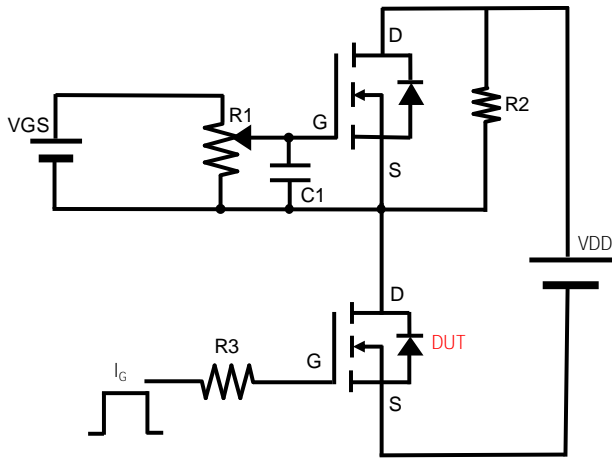


Figure B. Gate Charge Test Circuit & Waveform

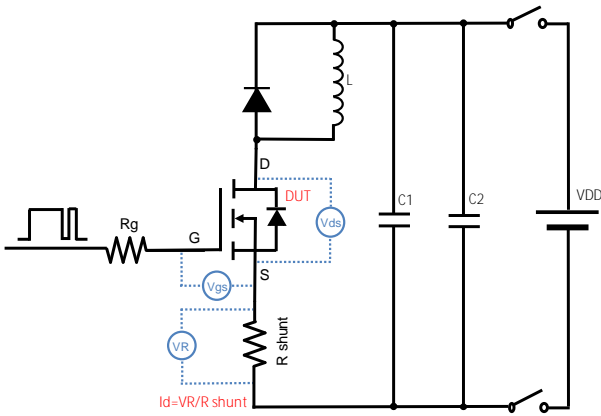


Figure C. Resistive Switching Test Circuit & Waveform

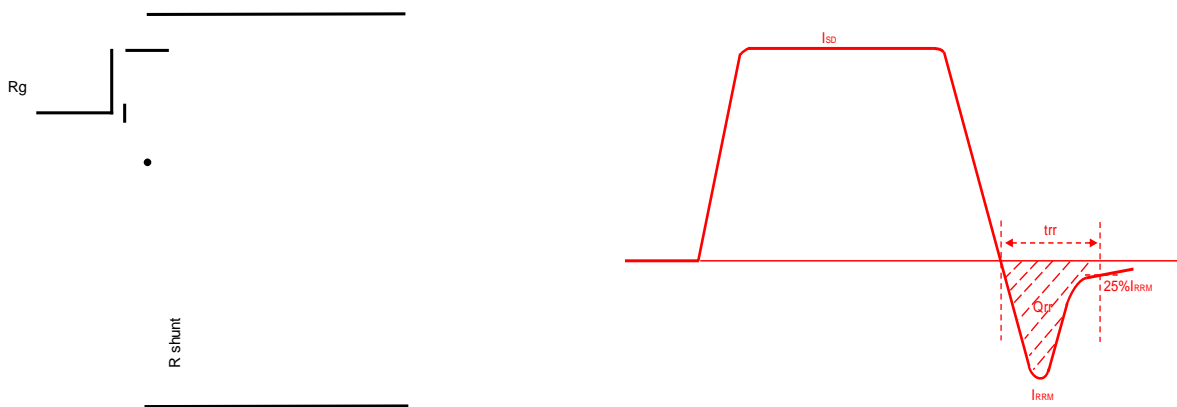
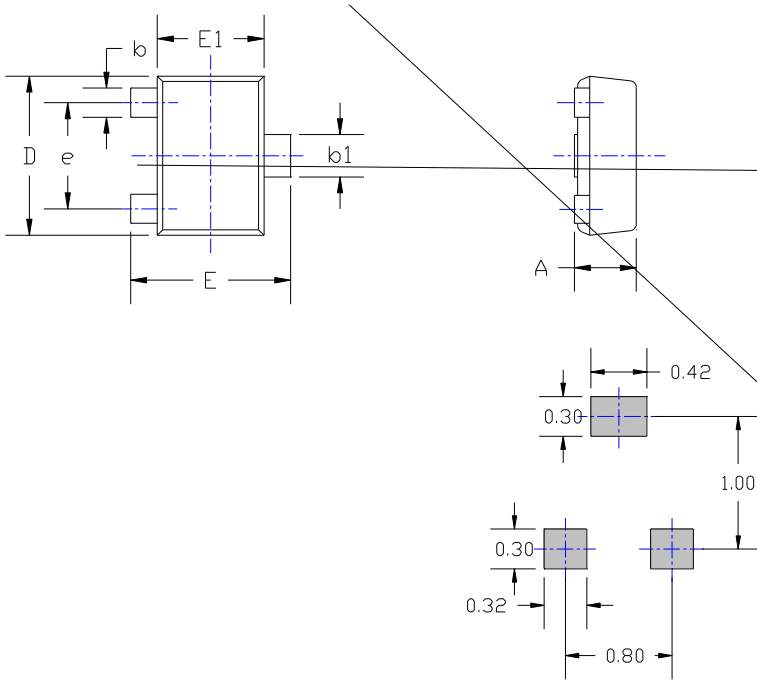


Figure D. Diode Recovery Test Circuit & Waveform



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SOT-723 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.017	0.022	0.430	0.550
A1	0.000	0.002	0.000	0.050
b	0.007	0.011	0.170	0.270
b1	0.011	0.015	0.270	
c	0.003			
D	0.045	0.049	1.150	1.250
E	0.045	0.049	1.150	1.250
E1	0.030	0.033	0.750	0.850
e	0.031TYP.		0.800TYP.	
	7°REF.		7°REF.	

NOTE:
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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