



# YJB180G04C

## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	40V
$I_D$	180A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	2.0m
$R_{DS(ON)}$ ( at $V_{GS}=4.5V$ )	3.0m
100% EAS Tested	
100% $V_{DS}$ Tested	

### General Description

Split gate trench MOSFET technology  
Excellent stability and uniformity  
Moisture Sensitivity Level 1  
Epoxy Meets UL 94 V-0 Flammability Rating  
Halogen Free

### Applications

Power switching application  
Portable equipment

### Absolute Maximum Ratings ( $T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	40	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ C$	$I_D$	28	A
	$T_A=100^\circ C$		17	
	$T_C=25^\circ C$		180	
	$T_C=100^\circ C$		113	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	720	A
Avalanche energy <sup>B</sup>		EAS	961	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ C$	$P_D$	5	W
	$T_A=100^\circ C$		2	
	$T_C=25^\circ C$		208	
	$T_C=100^\circ C$		83	



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## Electrical Characteristics ( $T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$				



## Typical Electrical and Thermal Characteristics Diagrams

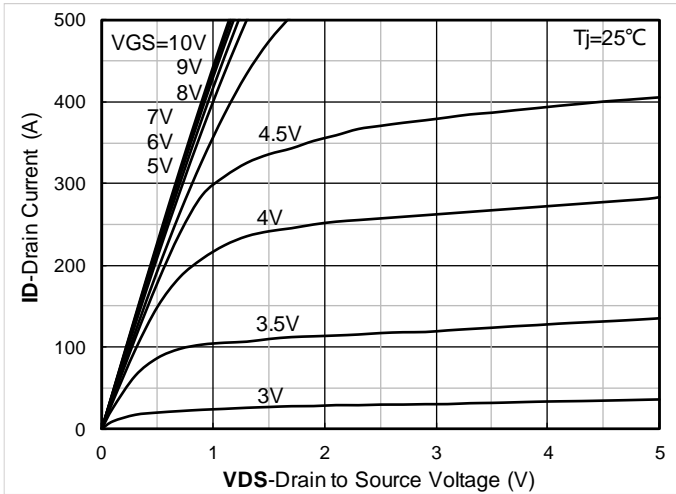


Figure 1. Output Characteristics

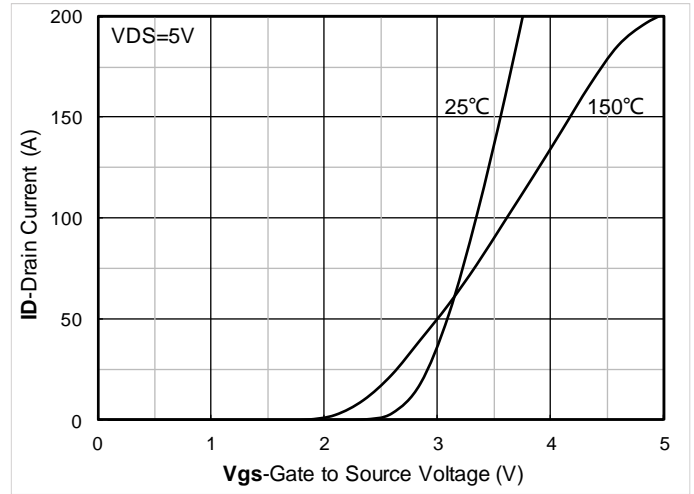


Figure 2. Transfer Characteristics

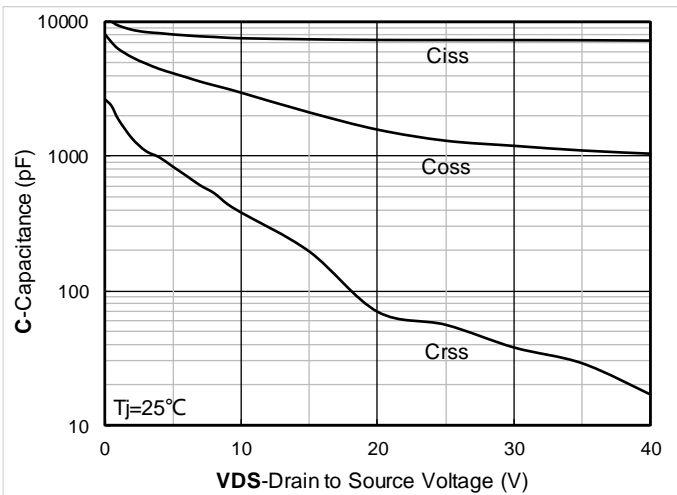


Figure 3. Capacitance Characteristics

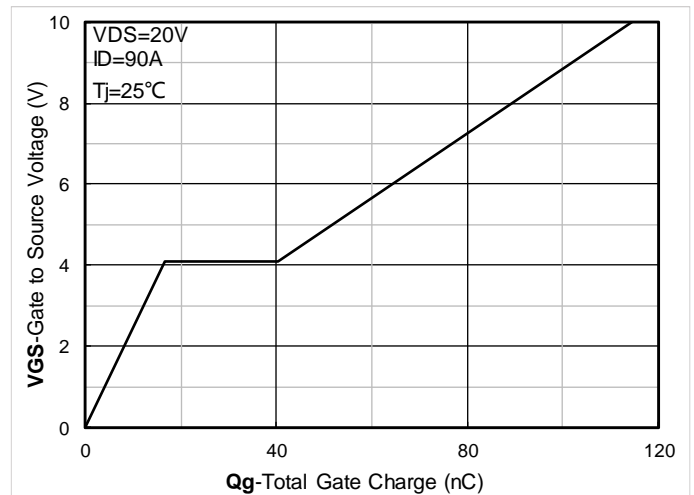


Figure 4. Gate Charge

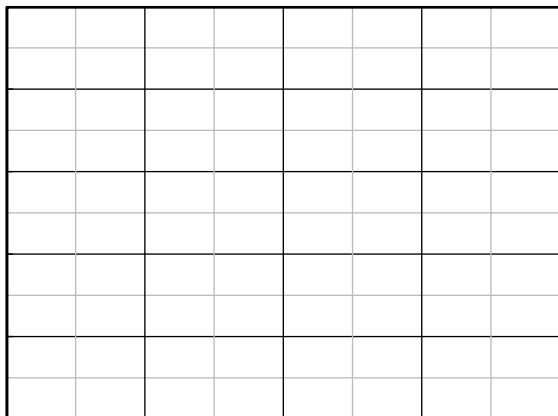


Figure 5. On-Resistance vs Gate to Source Voltage

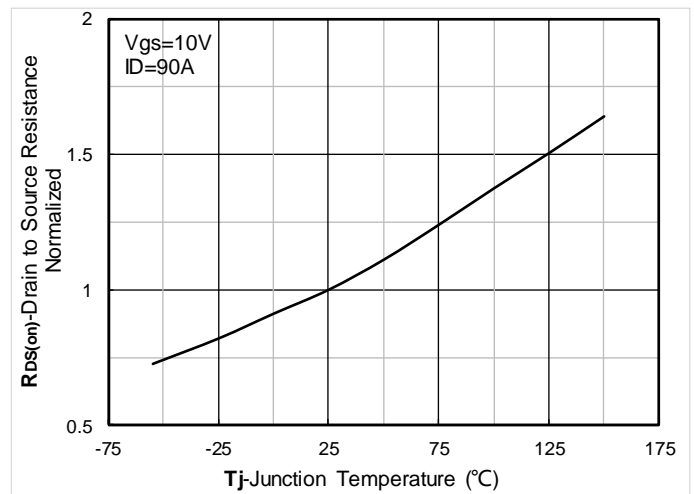


Figure 6. Normalized On-Resistance

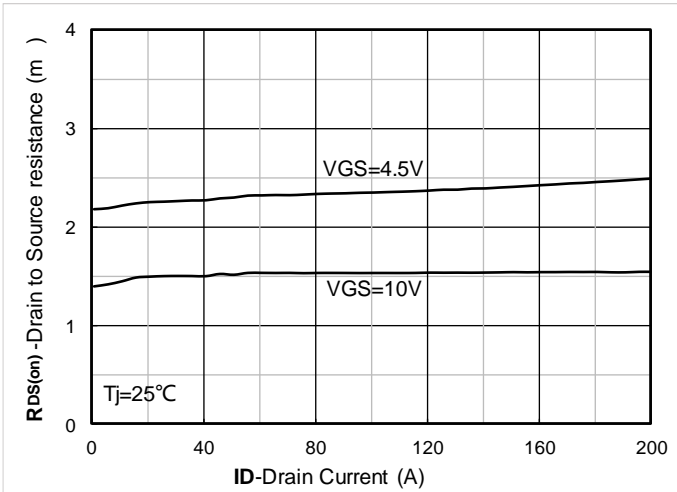


Figure 7. RDS(on) VS Drain Current

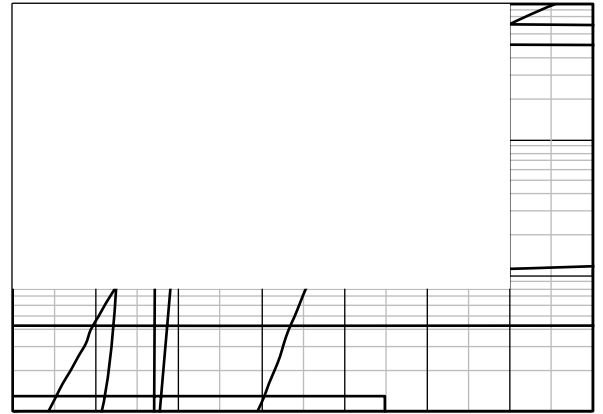


Figure 8. Forward characteristics of reverse diode

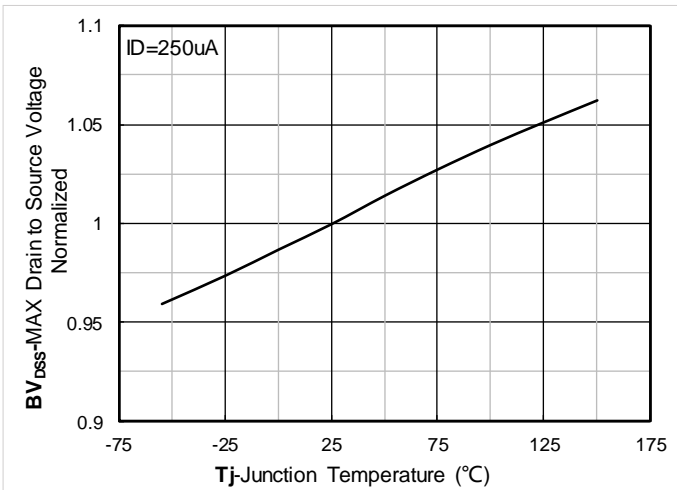


Figure 9. Normalized breakdown voltage

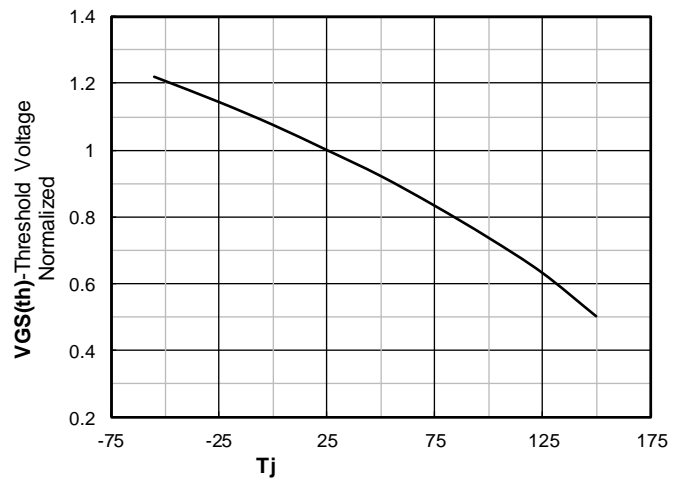


Figure 10. Normalized Threshold voltage

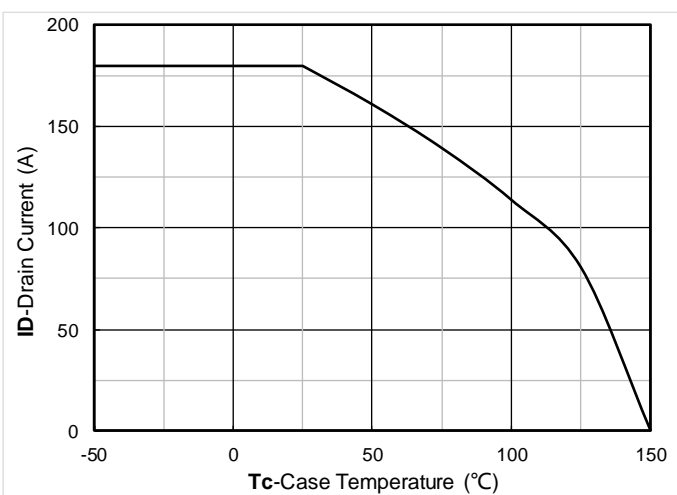


Figure 11. Current dissipation

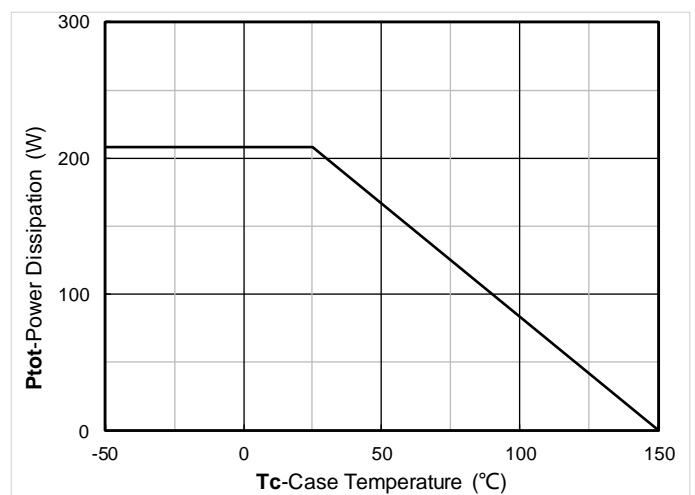


Figure 12. Power dissipation

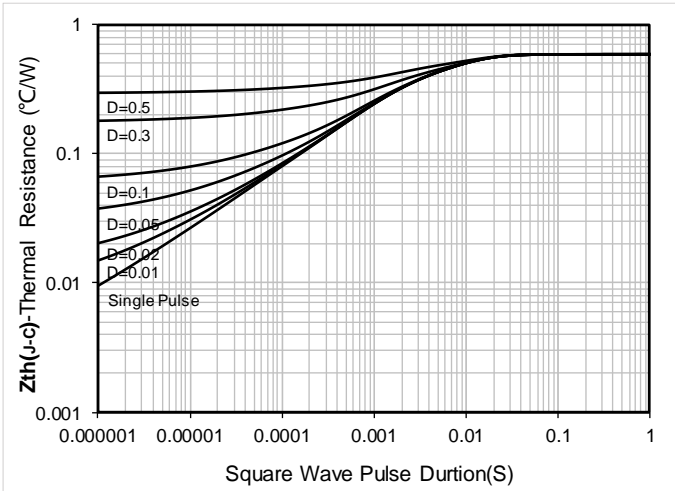


Figure 13. Maximum Transient Thermal Impedance

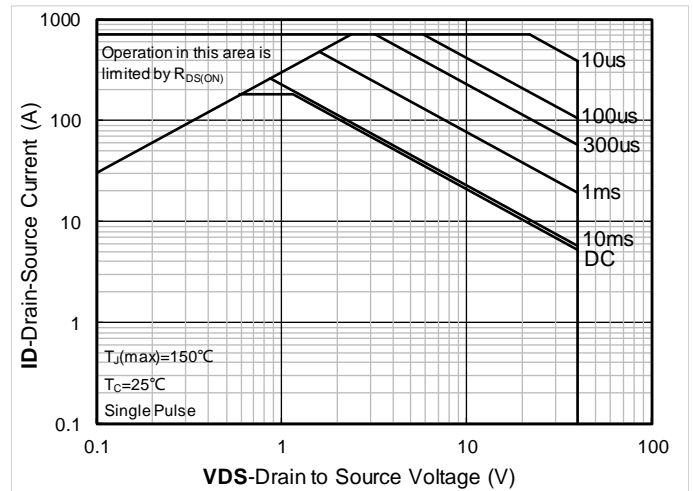


Figure 14. Safe Operation Area

## Test Circuits & Waveforms

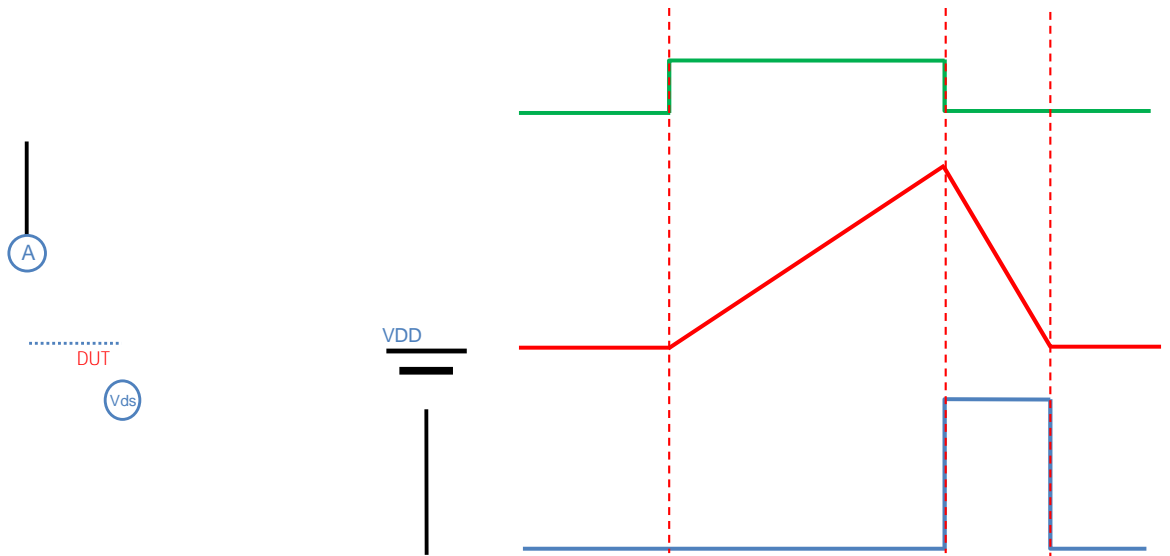


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

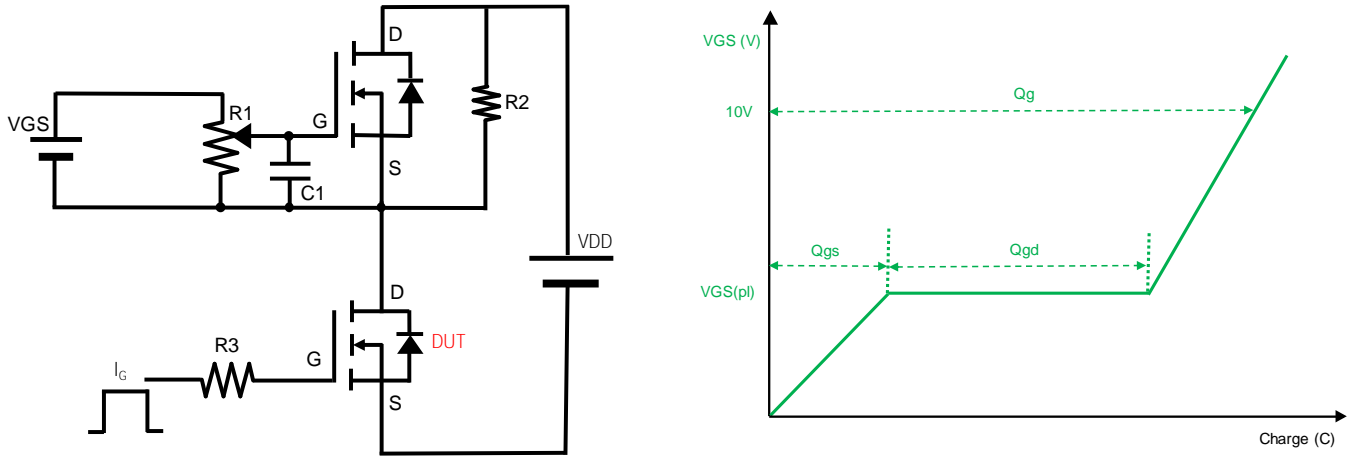


Figure B. Gate Charge Test Circuit & Waveform

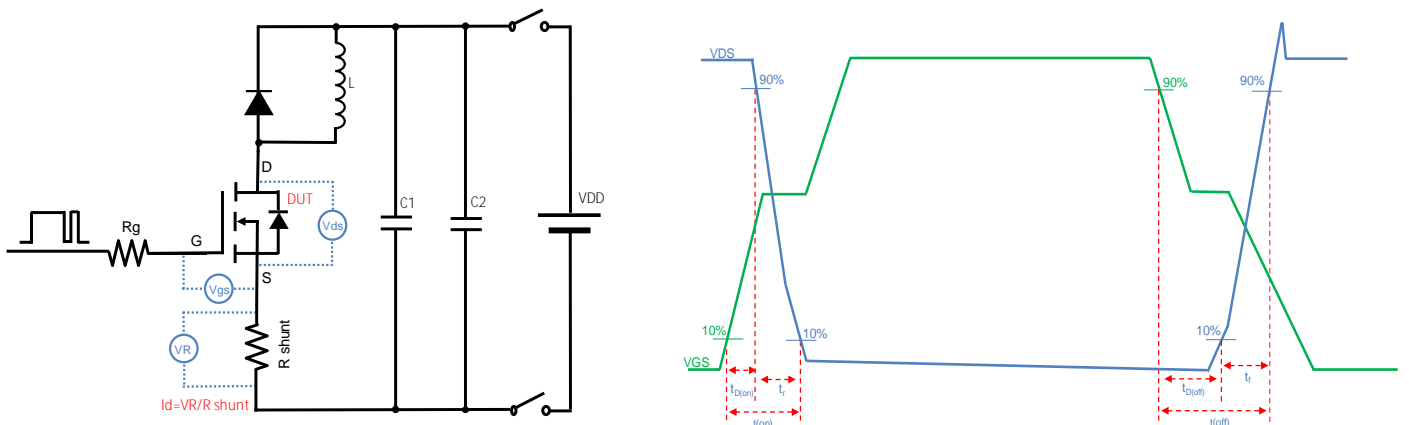


Figure C. Resistive Switching Test Circuit & Waveform

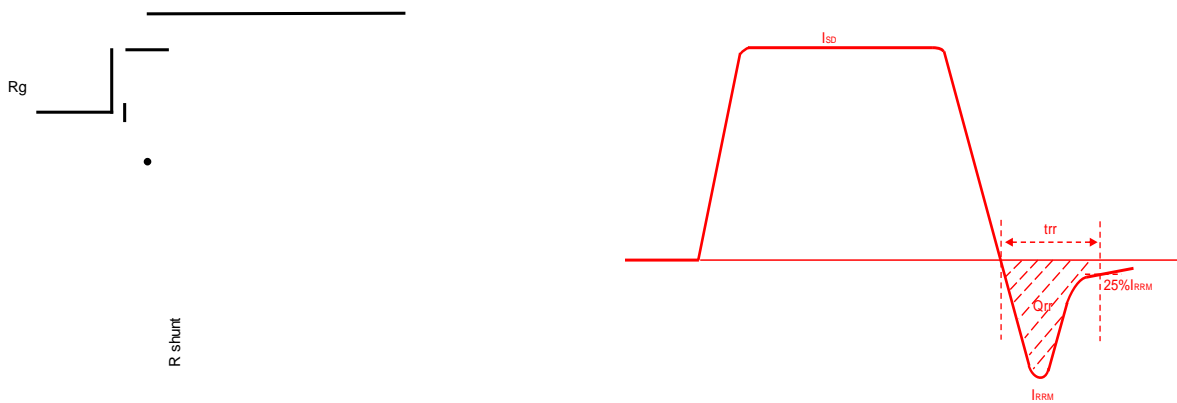
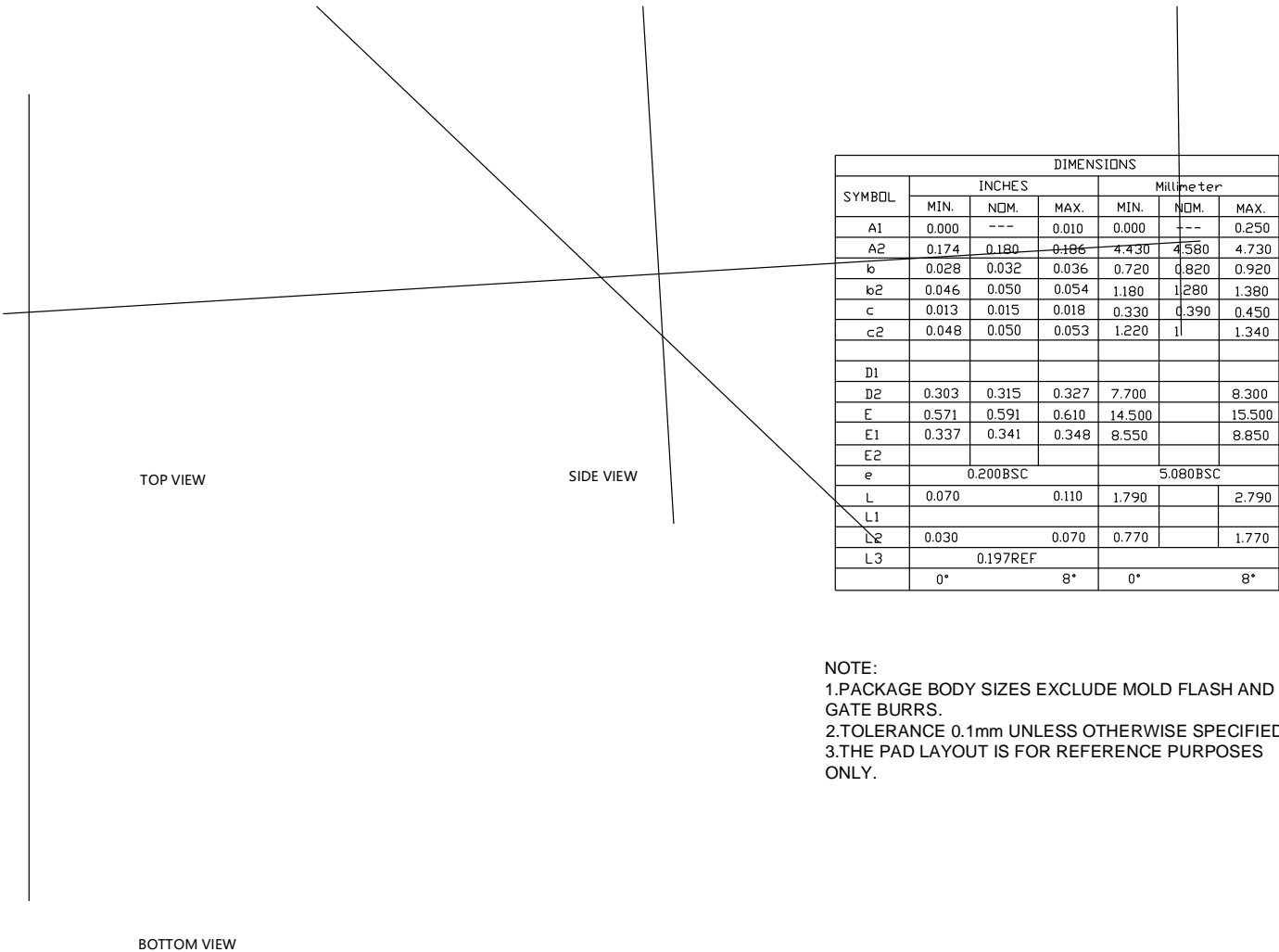


Figure D. Diode Recovery Test Circuit & Waveform



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## TO-263-HY Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.010	0.000	---	0.250
A2	0.174	0.180	0.186	4.430	4.580	4.730
b	0.028	0.032	0.036	0.720	0.820	0.920
b2	0.046	0.050	0.054	1.180	1.280	1.380
c	0.013	0.015	0.018	0.330	0.390	0.450
c2	0.048	0.050	0.053	1.220	1.1	1.340
D1						
D2	0.303	0.315	0.327	7.700		8.300
E	0.571	0.591	0.610	14.500		15.500
E1	0.337	0.341	0.348	8.550		8.850
E2						
e	0.200BSC			5.080BSC		
L	0.070		0.110	1.790		2.790
L1						
L2	0.030		0.070	0.770		1.770
L3	0.197REF					
	0°		8°	0°		8°

### NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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