



N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	60V
I_D	200A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	2.9 mohm
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	3.9 mohm
100% EAS Tested	
100% V_{DS} Tested	

General Description

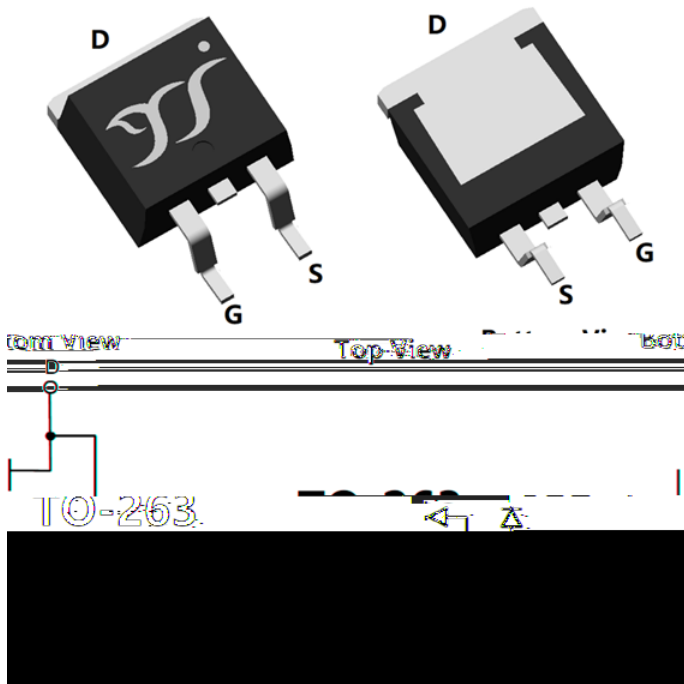
Split Gate Trench MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$

-0 Flammability Rating

alogen Free

Applications

Isolated DC-DC Converters
Motor control
Invertors



Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	60	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current ^A	I_D	$T_C=25$	200
		$T_C=100$	125
Pulsed Drain Current ^B	I_{DM}	600	A
Avalanche energy ^C	EAS	506	mJ
Total Power Dissipation ^D	P_D	260	W
Thermal Resistance Junction-to-Case	R_{JC}	0.48	/ W
Thermal Resistance Junction-to-Ambient ^E	R_{JA}	28	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 +150	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJB200G06C	F2	YJB200G06C	800	/	8000	13 reel



Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V			1	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ± 20V, V _{DS} =0V			± 100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250	1.2	1.6	2.2	V
Static Drain-Source On-Resistance	R _{Ds(ON)}	V _{GS} = 10V, I _D =20A		2.35	2.9	m
		V _{GS} = 4.5V, I _D =15A		2.9	3.9	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V			1.2	V
Maximum Body-Diode Continuous Current	I _S				200	A
Dynamic Parameters						

Input Capacitance

C_{iss}

V_{DS}=25V, V_{GS}=0V, f= 24.84 reW*n /P



Typical Performance Characteristics

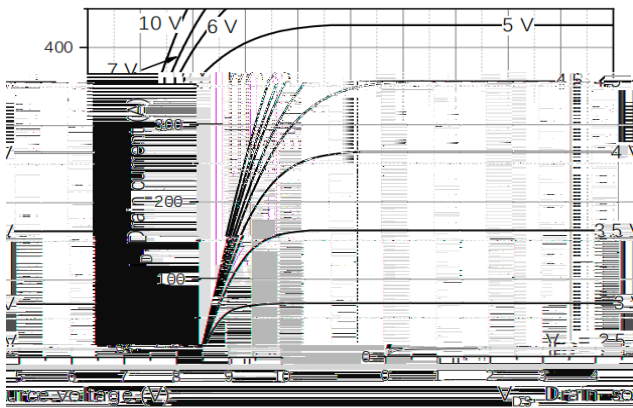


Figure1. Output Characteristics

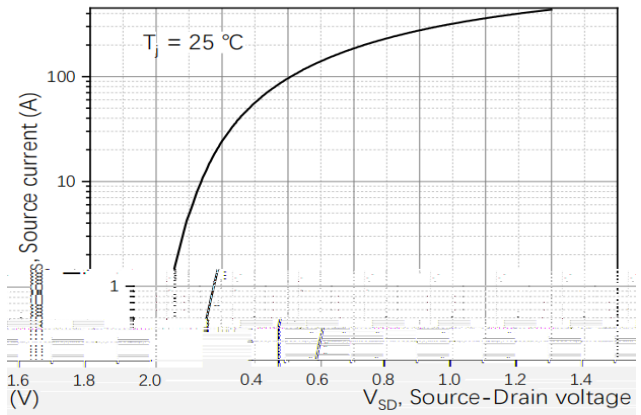


Figure2. Transfer Characteristics

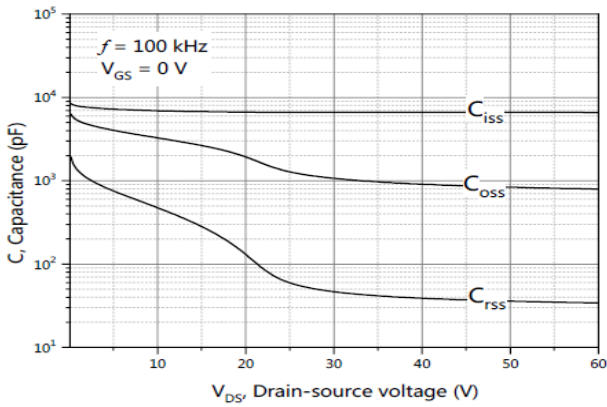


Figure3. Capacitance Characteristics

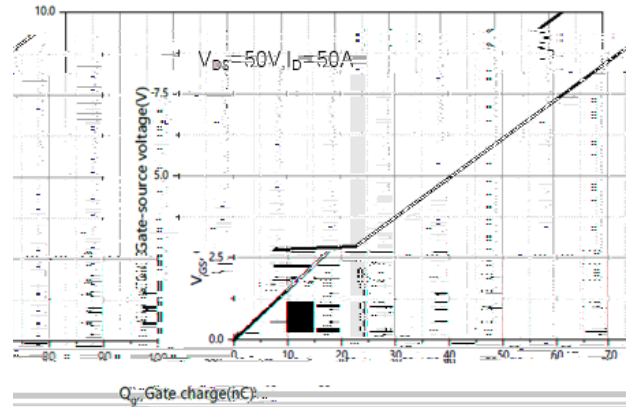


Figure4. Gate Charge

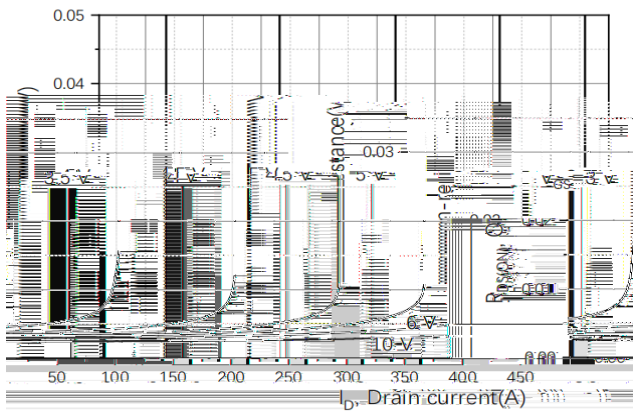


Figure5. Drain-Source on Resistance

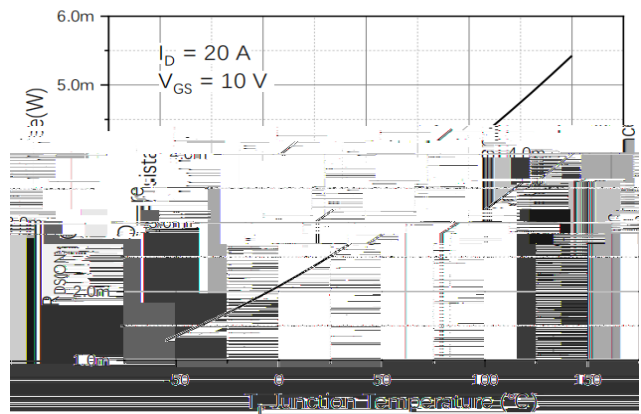


Figure6. Drain-Source on Resistance

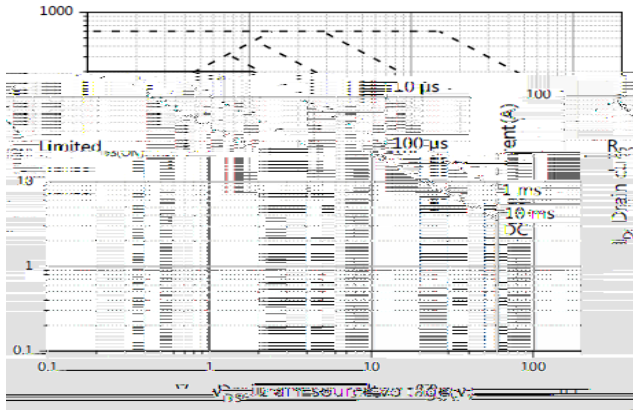


Figure7. Safe Operation Area

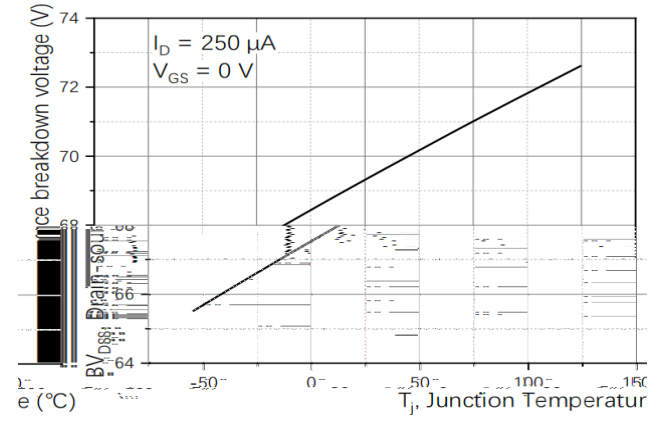


Figure8. Drain-source breakdown voltage

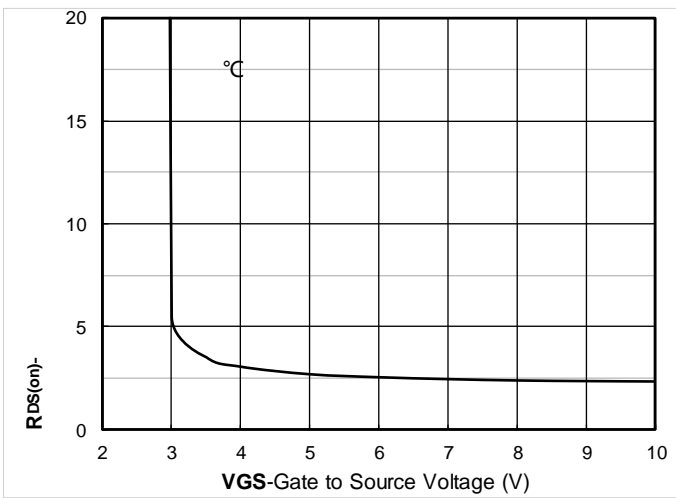


Figure9. On-Resistance vs Gate to Source Voltage

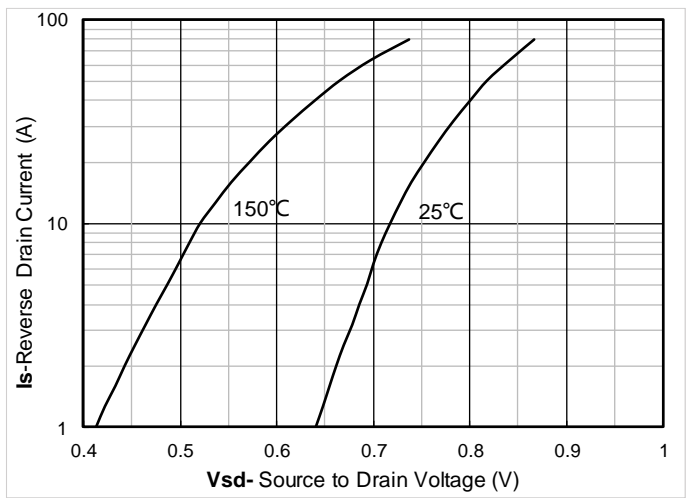


Figure10. Forward characteristics of reverse diode

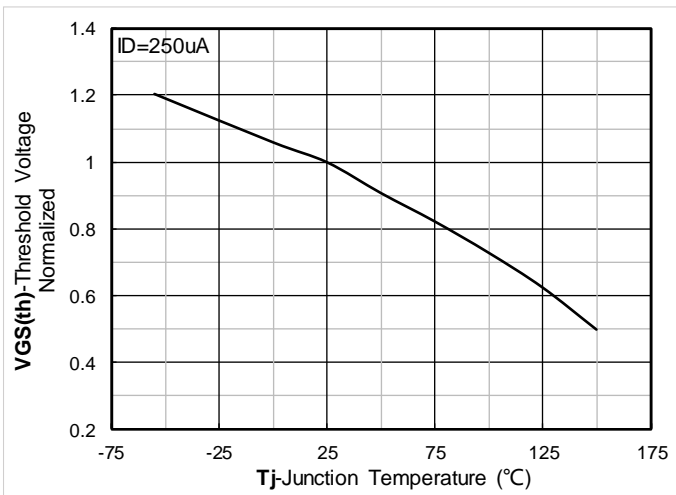


Figure11. Normalized Threshold voltage

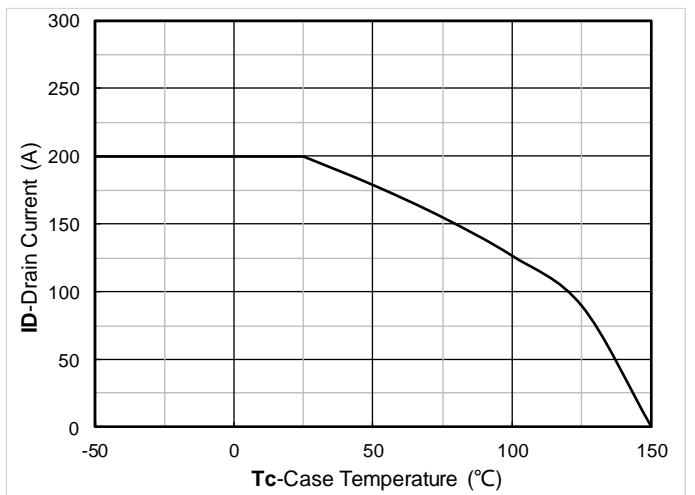


Figure12. Current dissipation

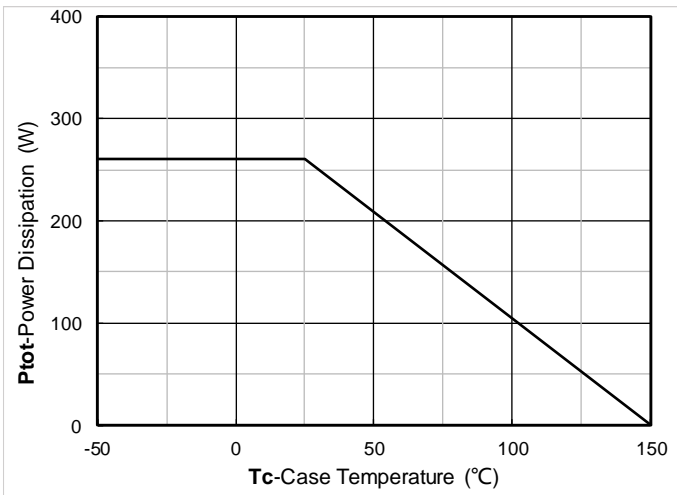


Figure13. Power dissipation

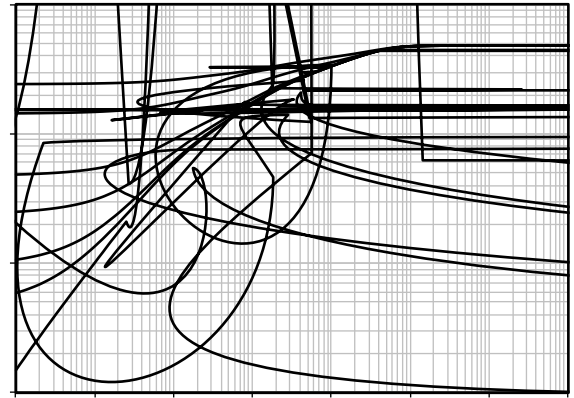


Figure14. Maximum Transient Thermal Impedance

Test circuits and waveforms

Figure A: Gate Charge Test Circuit & Waveforms

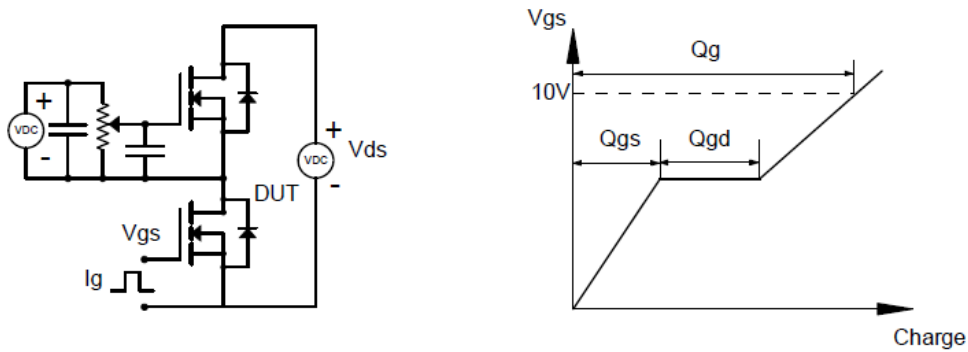
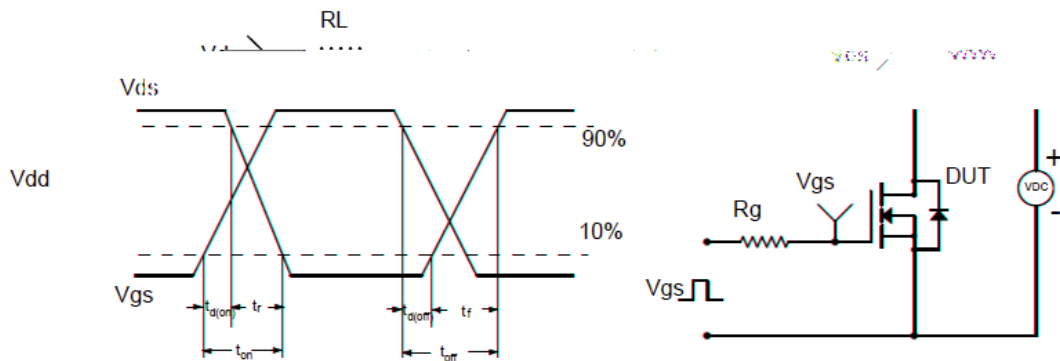
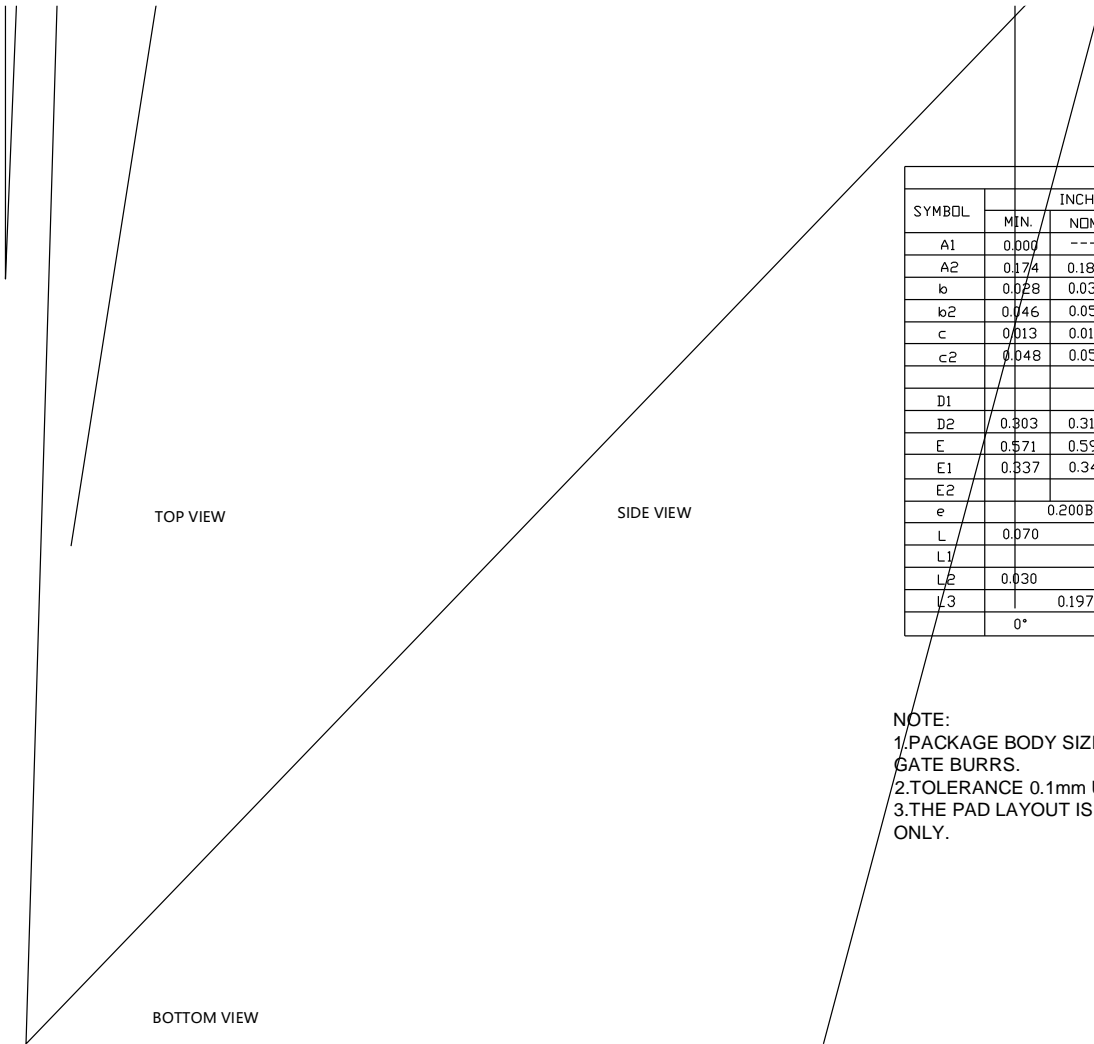


Figure B: Resistive Switching Test Circuit & Waveforms





TO-263-HY Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A1	0.000	---	0.010	0.000	---	0.250
A2	0.174	0.180	0.186	4.430	4.580	4.730
b	0.028	0.032	0.036	0.720	0.820	0.920
b2	0.046	0.050	0.054	1.180	1.280	1.380
c	0.013	0.015	0.018	0.330	0.390	0.450
c2	0.048	0.050	0.053	1.220	1	1.340
D1						
D2	0.303	0.315	0.327	7.700		8.300
E	0.571	0.591	0.610	14.500		15.500
E1	0.337	0.341	0.348	8.550		8.850
E2						
e		0.200BSC		5.080BSC		
L	0.070		0.110	1.790		2.790
L1						
L2	0.030		0.070	0.770		1.770
L3		0.197REF				
	0°		8°	0°		8°

NOTE:
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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