



# YJB2D7G10H

## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	100V
$I_D$	170A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	2.7m
100% EAS Tested	
100% $V_{DS}$ Tested	

### General Description

Split Gate Trench MOSFET technology  
Excellent package for heat dissipation  
High density cell design for low  $R_{DS(ON)}$   
Moisture Sensitivity Level 1  
Epoxy Meets UL 94 V-0 Flammability Rating  
Halogen Free

### Applications

Load switch  
Battery management  
Solar

### Absolute Maximum Ratings ( $T_J=25$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
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Drain-source Voltage



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## Electrical Characteristics ( $T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D$	100	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	
		$V_{DS}=100V, V_{GS}=0V, T_J=125^\circ C$	-	-	100	
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D$	2.2	3.0	3.8	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=50A$	-	2	2.7	
Diode Forward Voltage	$V_{SD}$	$I_S=50A, V_{GS}=0V$	-	-	1.2	V
Gate resistance	$R_G$	$f=1MHz$	-	0.8	-	
Maximum Body-Diode Continuous Current	$I_S$		-	-	170	A
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V, f=1MHz$	-	9440	-	pF
Output Capacitance	$C_{oss}$		-	3180	-	
Reverse Transfer Capacitance	$C_{rss}$		-	50	-	
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g$	$V_{GS}=10V, V_{DS}=50V, I_D=50A$	-	132.5	-	nC
Gate-Source Charge	$Q_{gs}$		-	55	-	
Gate-Drain Charge	$Q_{gd}$		-	17	-	
Reverse Recovery Charge	$Q_{rr}$	$I_F=50A, di/dt=100A/us$	-	157	-	nC
Reverse Recovery Time	$t_{rr}$		-	93	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=50V, I_D=50A$ $R_{GEN}=3$	-	30	-	ns
Turn-on Rise Time	$t_r$		-	48	-	
Turn-off Delay Time	$t_{D(off)}$		-	59	-	
Turn-off fall Time	$t_f$		-	34	-	

### Note

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of  $R_{\theta}$  is measured with the device mounted on the 40mm\*40mm\*1.1mm single layer FR-4 PCB board with 1 in<sup>2</sup> pad of 2oz. Copper, in the still air environment with  $T_A=25$ . The maximum allowed junction temperature of 175. The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).



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## Typical Electrical and Thermal Characteristics Diagrams

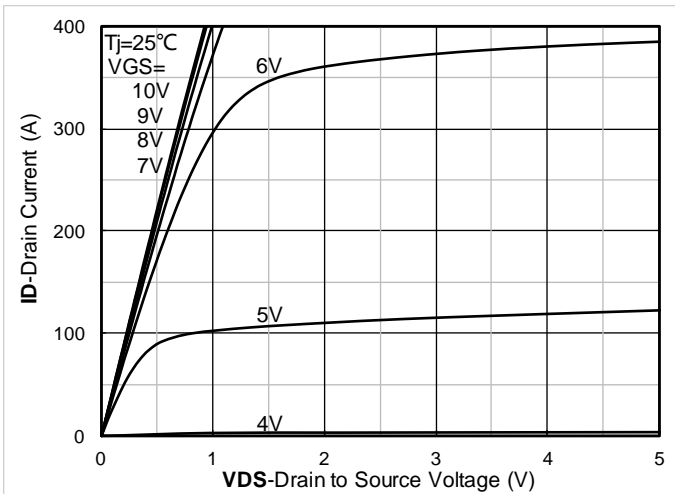


Figure 1. Output Characteristics

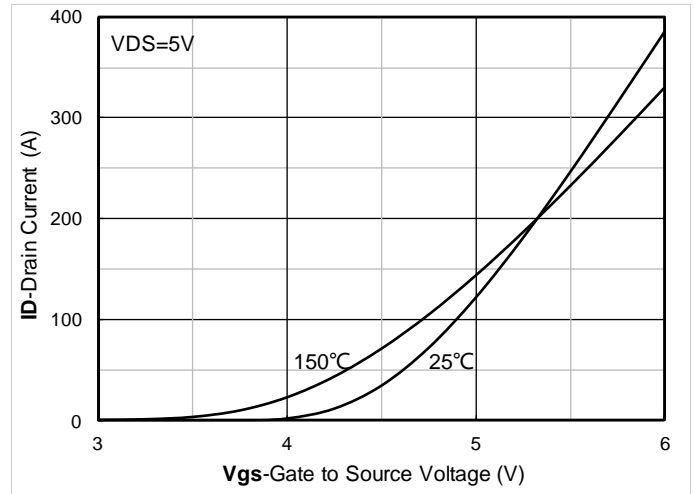


Figure 2. Transfer Characteristics

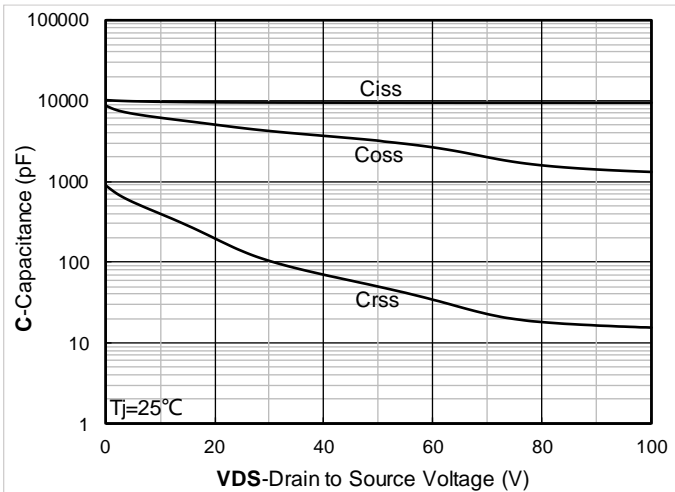


Figure 3. Capacitance Characteristics

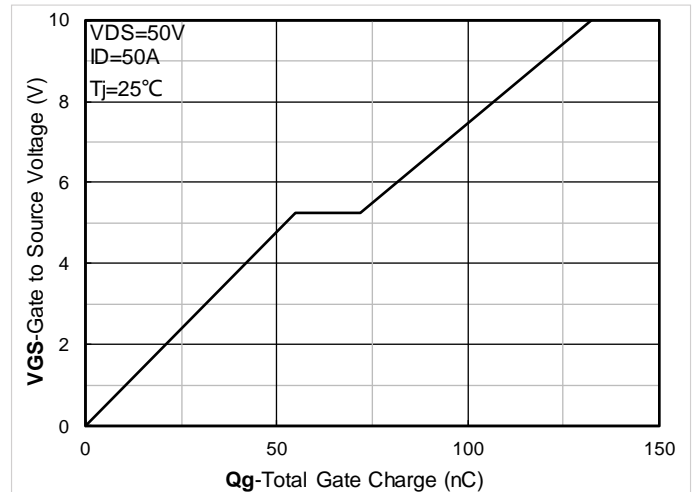


Figure 4. Gate Charge

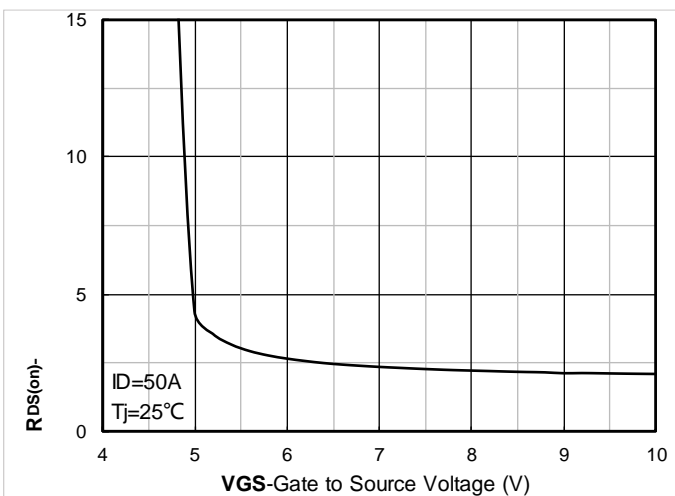


Figure 5. On-Resistance vs Gate to Source Voltage

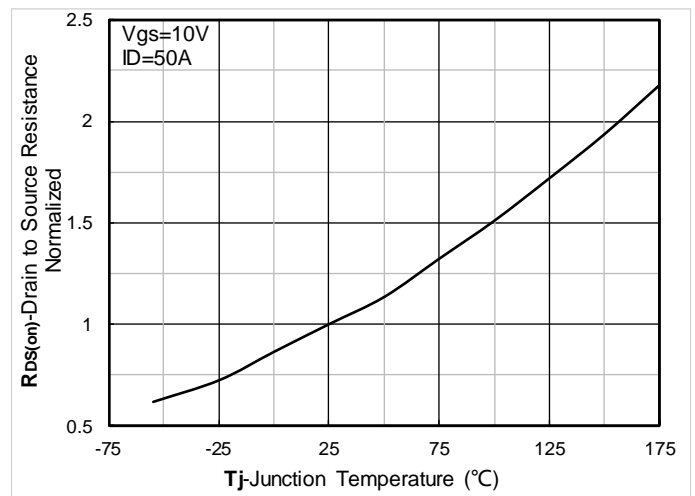


Figure 6. Normalized On-Resistance



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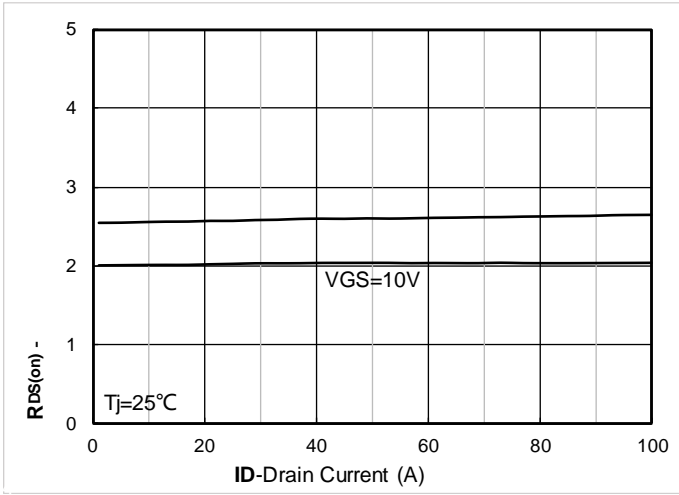


Figure 7.  $R_{DS(on)}$  VS Drain Current

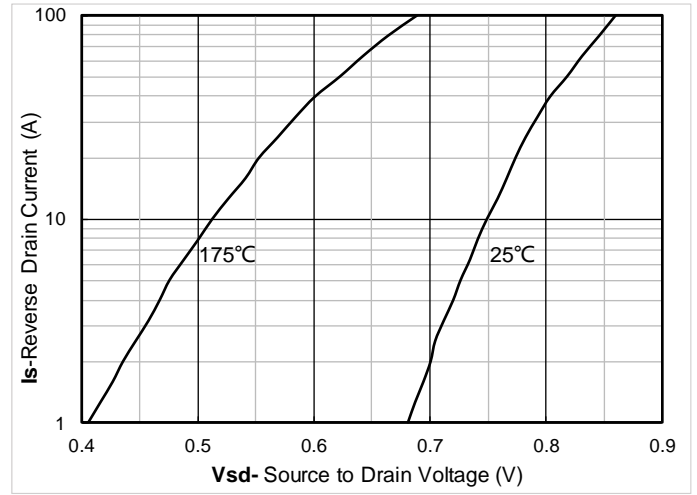


Figure 8. Forward characteristics of reverse diode

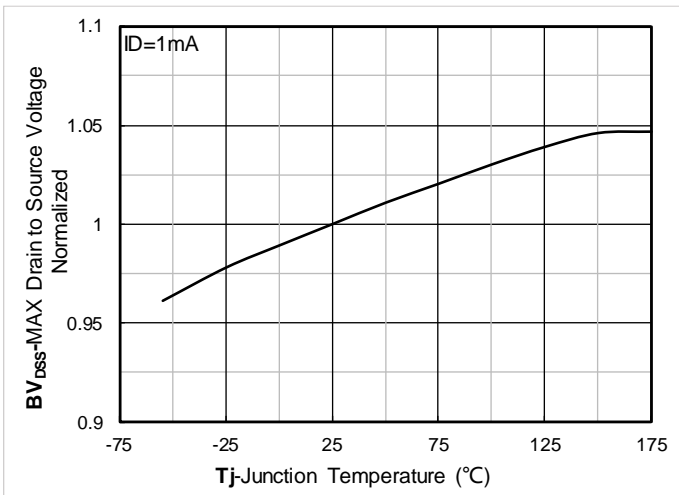


Figure 9. Normalized breakdown voltage

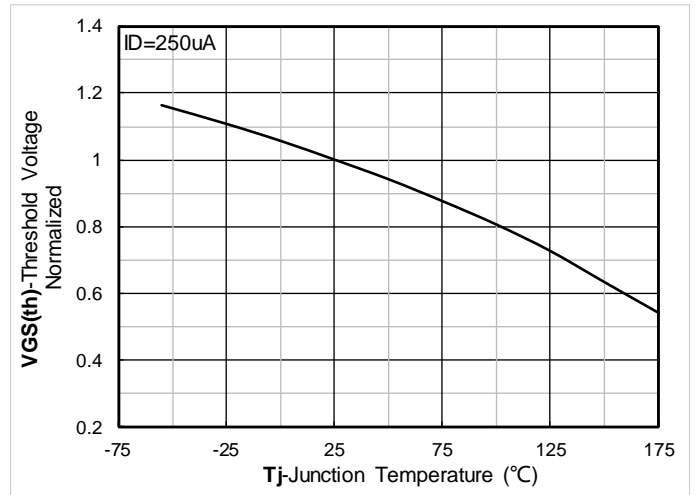


Figure 10. Normalized Threshold voltage

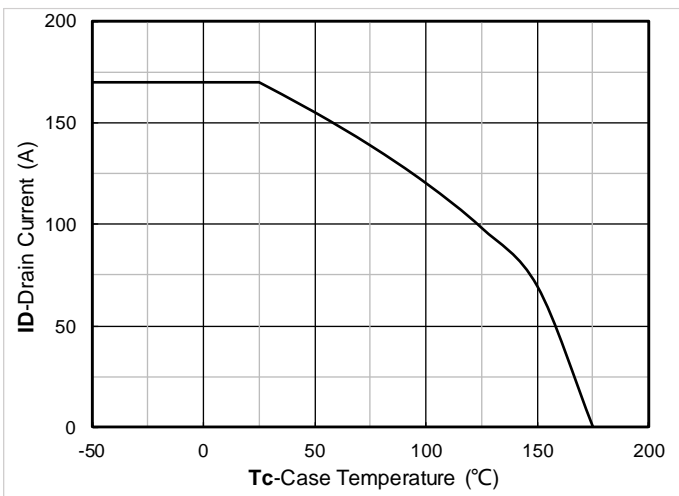


Figure 11. Current dissipation

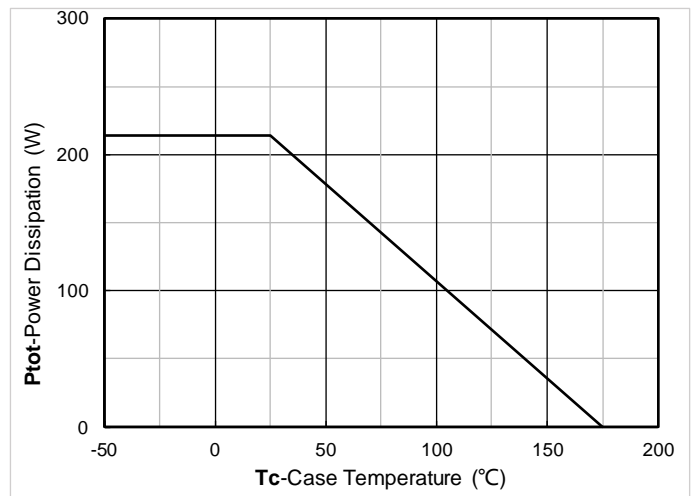


Figure 12. Power dissipation



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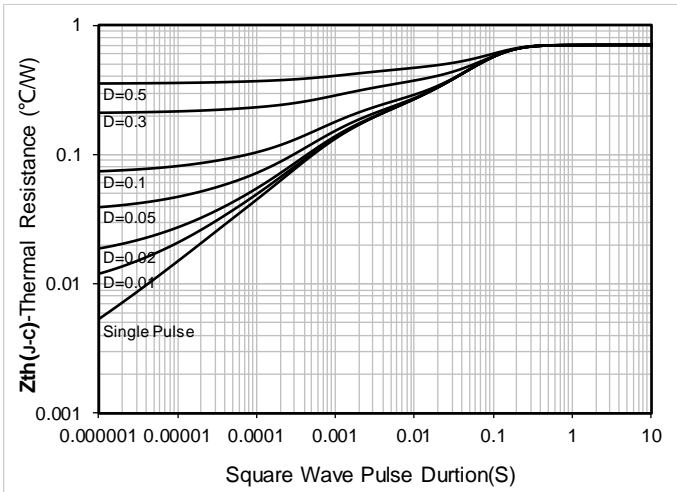


Figure 13. Maximum Transient Thermal Impedance

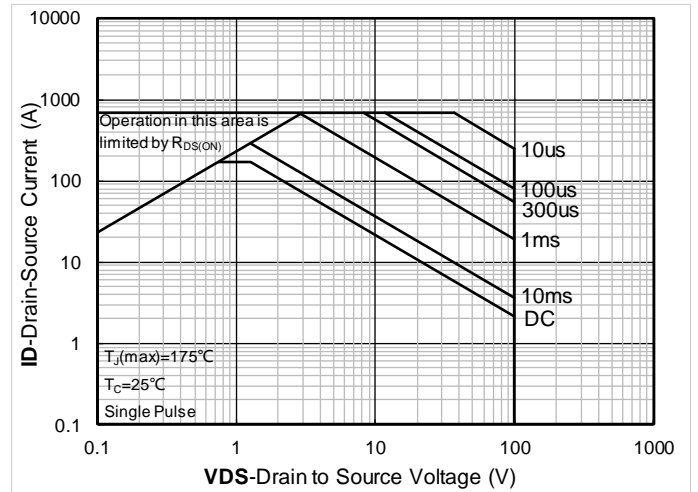


Figure 14. Safe Operation Area

## Test Circuits & Waveforms

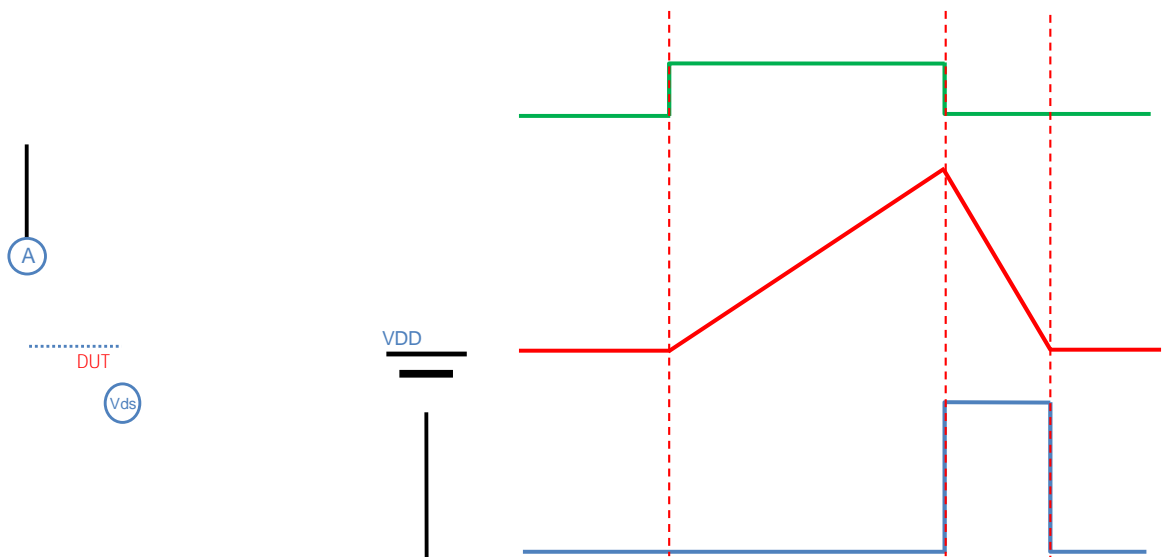


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

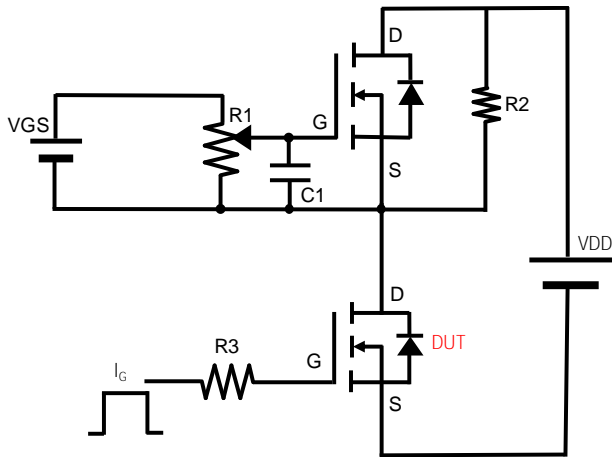


Figure B. Gate Charge Test Circuit & Waveform

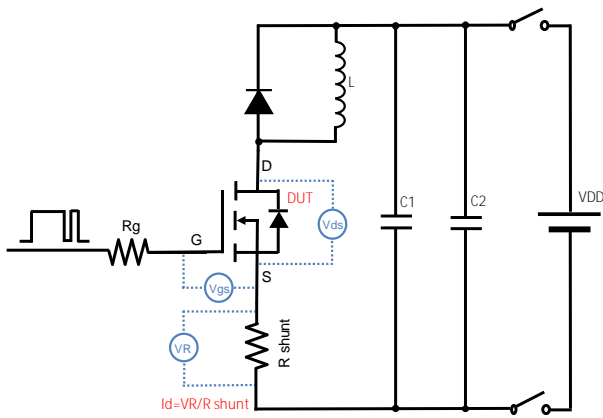


Figure C. Resistive Switching Test Circuit & Waveform

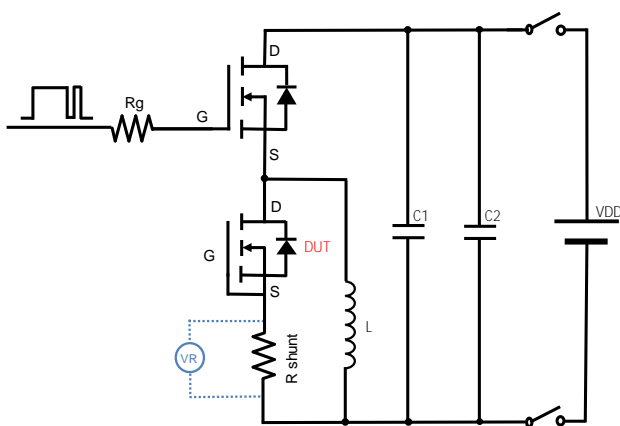
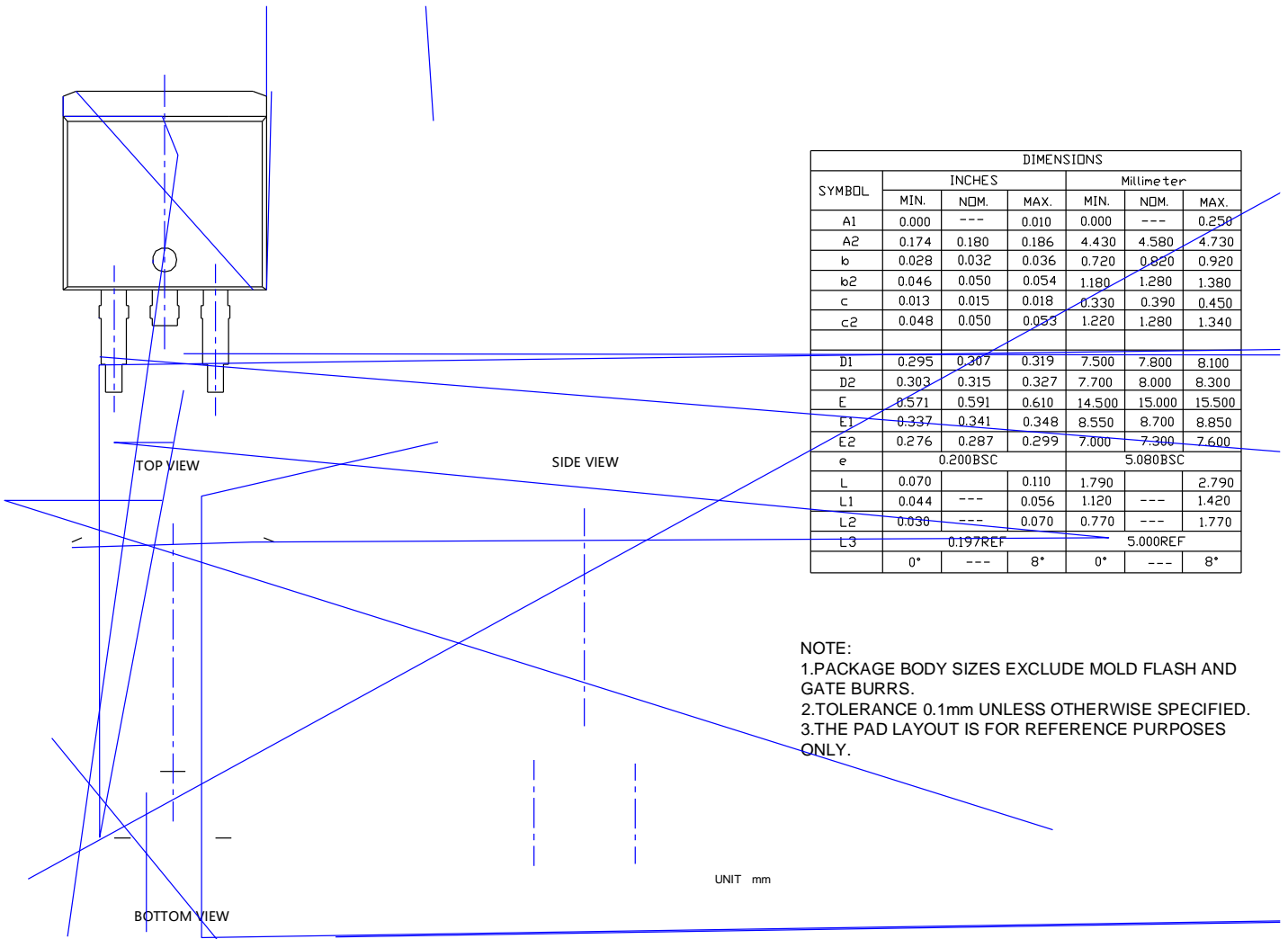


Figure D. Diode Recovery Test Circuit & Waveform



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## TO-263-HY Package information





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