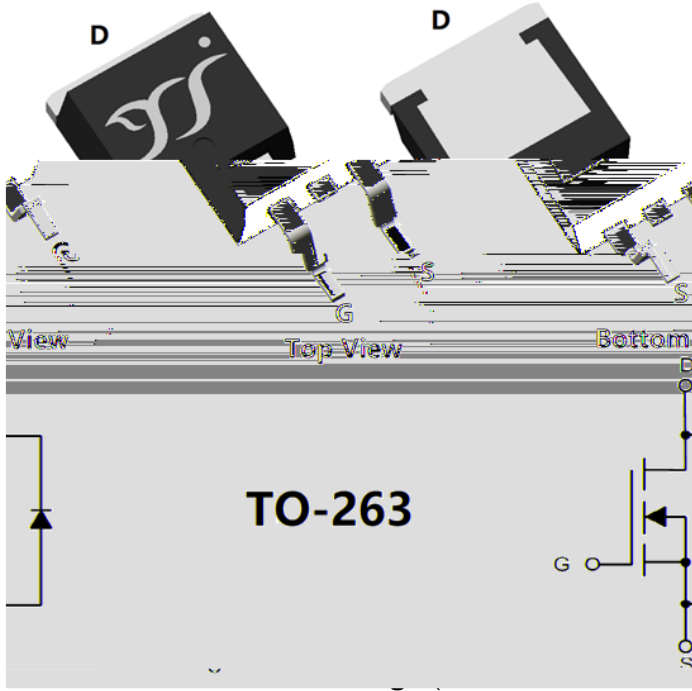




# N-Channel Enhancement Mode Field Effect Transistor



## Product Summary

$V_{DS}$	60V
$I_D$	90A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	5.0m
100% EAS Tested	
100% $V_{DS}$ Tested	

## General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

## Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

(otherwise noted)

Parameter			Symbol	Limit	Unit		
Drain-source Voltage			$V_{DS}$	60	V		
Gate-source Voltage			$V_{GS}$	±20	V		
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^{\circ}C$	$I_D$	18.5	A		
		$T_A=100^{\circ}C$		13			
Continuous Drain Current (Note 1,3)	Steady-State	$T_C=25^{\circ}C$		90			
		$T_C=100^{\circ}C$		63			
Pulsed Drain Current	$T_C=25^{\circ}C, t_p=100\mu s$			$I_{DM}$		350	A
Avalanche energy				$E_{AS}$		132.25	mJ
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^{\circ}C$	$P_D$	3.7	W		
		$T_A=100^{\circ}C$		1.8			
Total Power Dissipation (Note 1,3)	Steady-State	$T_C=25^{\circ}C$		93			
		$T_C=100^{\circ}C$		46			
Junction and Storage Temperature Range				$T_J, T_{STG}$		-55 +175	$^{\circ}C$

## Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	R	33	40	$^{\circ}C/W$
Thermal Resistance Junction-to-Case	Steady-State	R	1.3	1.6	

## Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJB5D0G06H	F2	YJB5D0G06H	800	/	8000	13 reel





# YJB5D0G06H

## Typical Electrical and Thermal Characteristics Diagrams

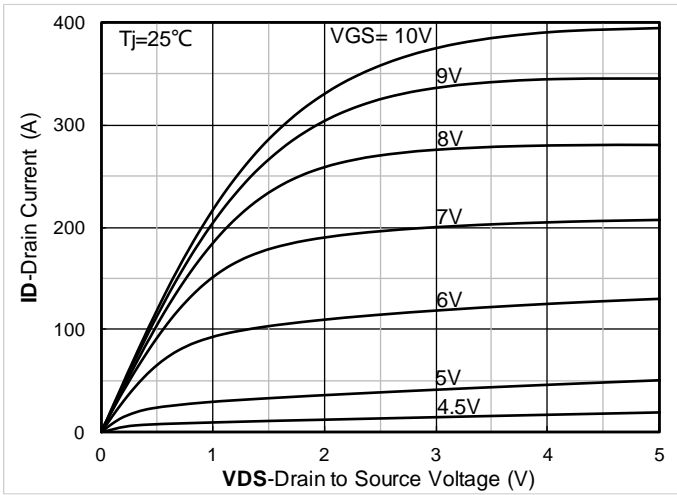


Figure 1. Output Characteristics

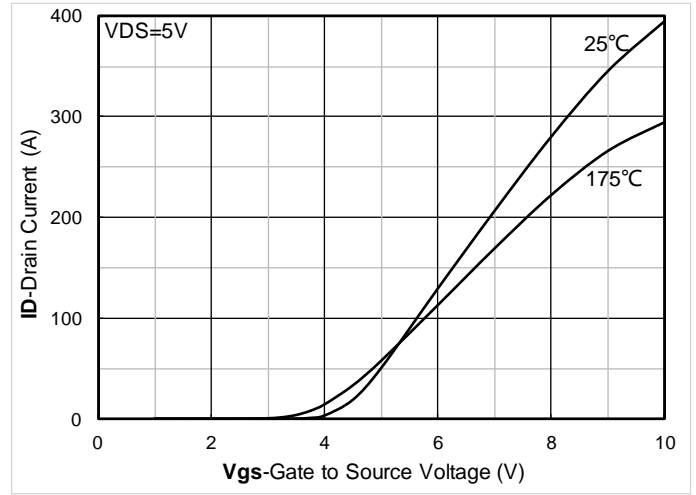


Figure 2. Transfer Characteristics

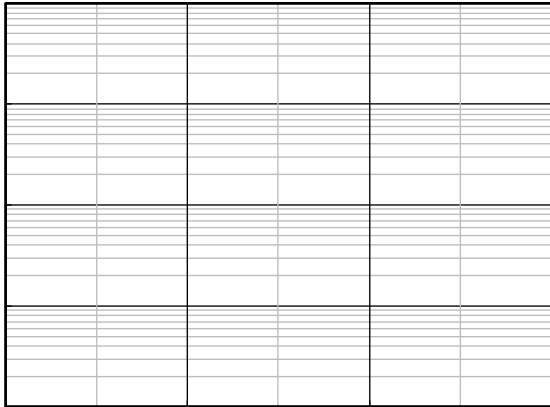


Figure 3. Capacitance Characteristics

Figure 4. Gate Charge

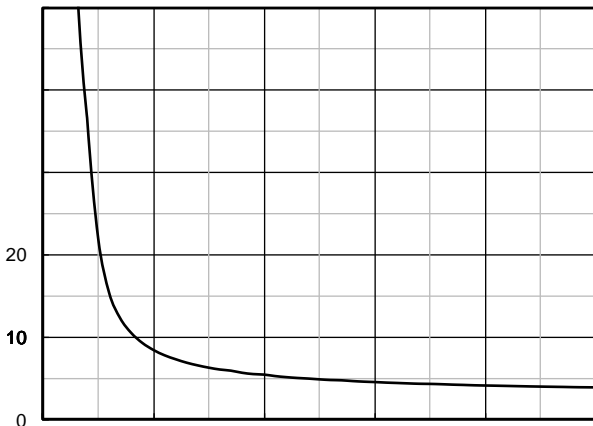


Figure 5. On-Resistance vs Gate to Source Voltage

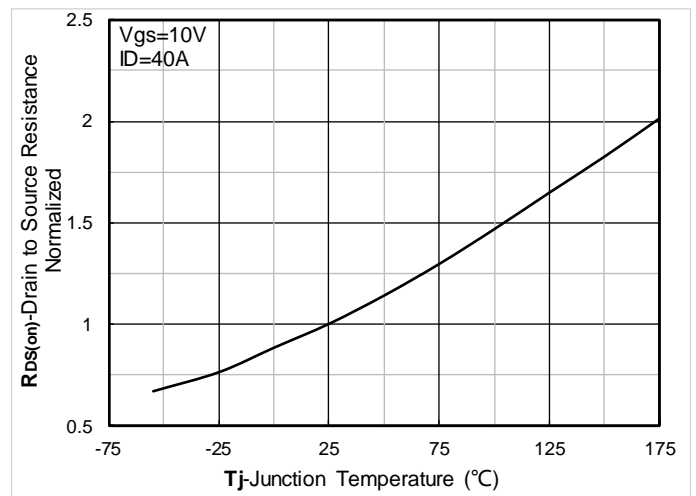


Figure 6. Normalized On-Resistance



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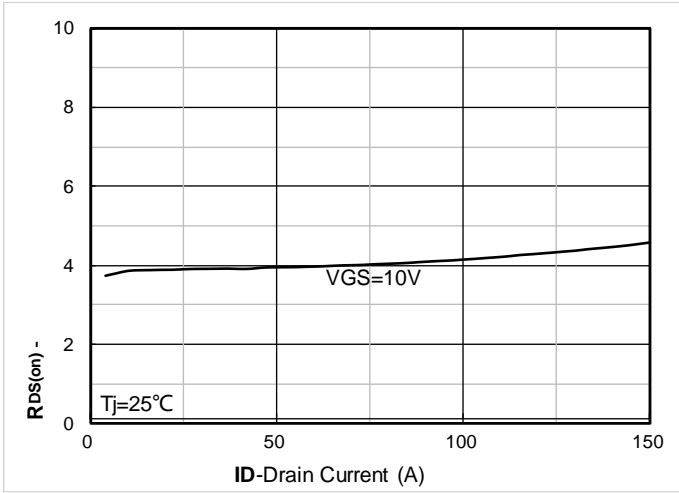


Figure 7.  $R_{DS(on)}$  VS Drain Current

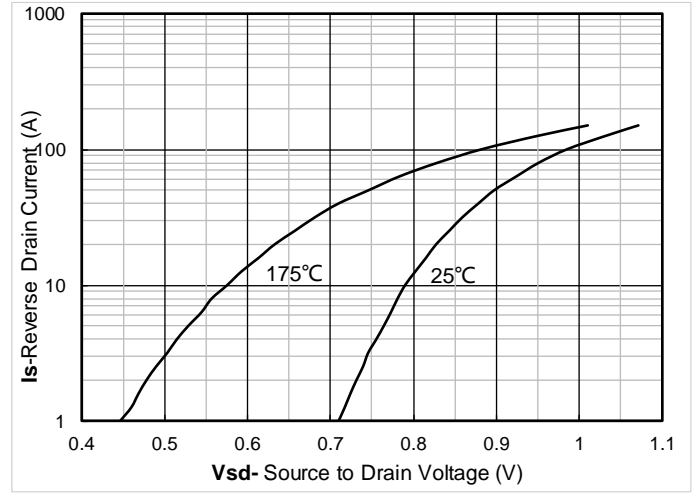


Figure 8. Forward characteristics of reverse diode

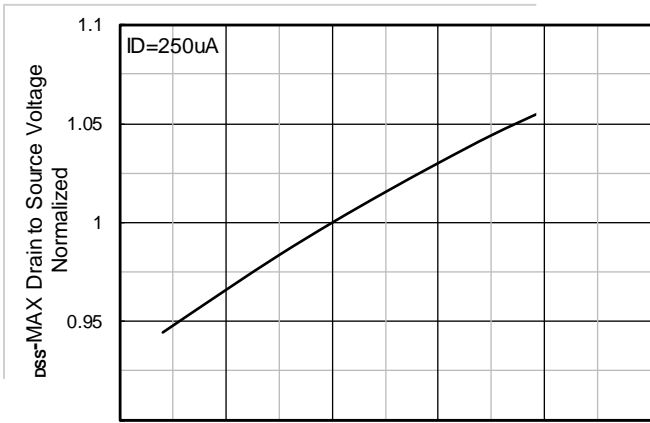


Figure 9. Normalized breakdown voltage

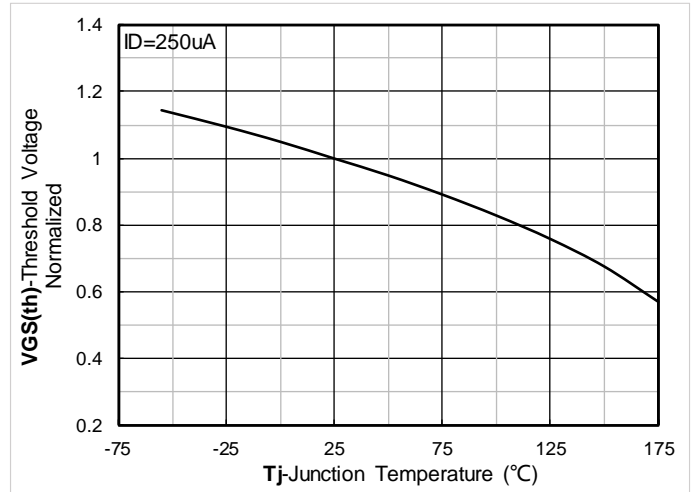


Figure 10. Normalized Threshold voltage

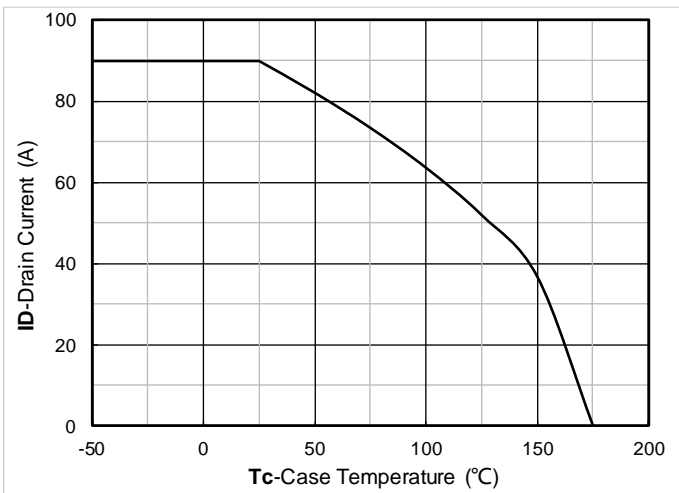


Figure 11. Current dissipation

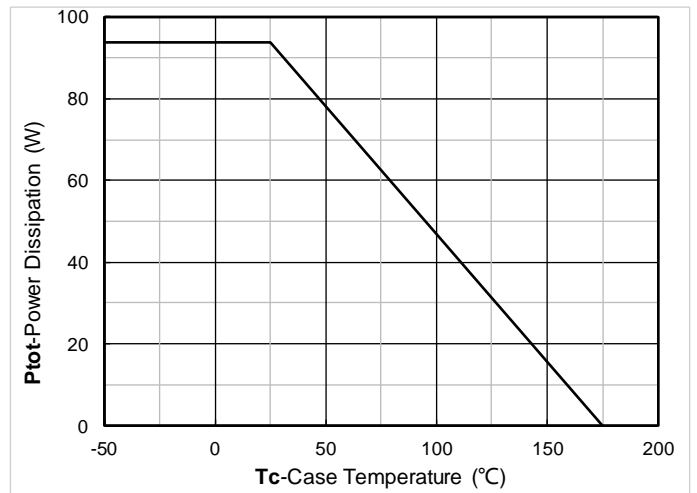


Figure 12. Power dissipation

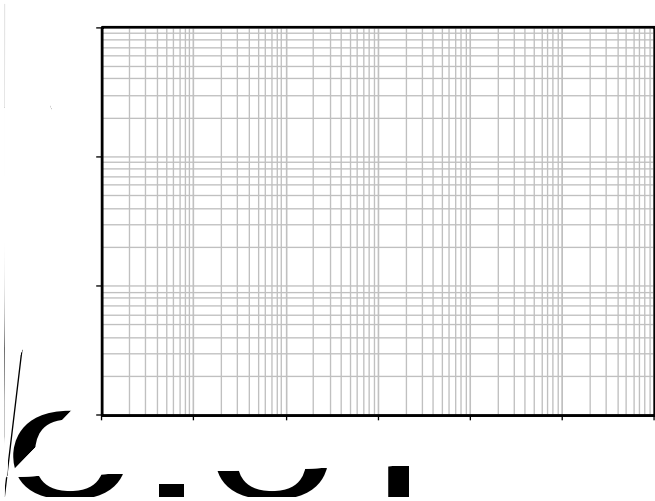


Figure 13. Maximum Transient Thermal Impedance

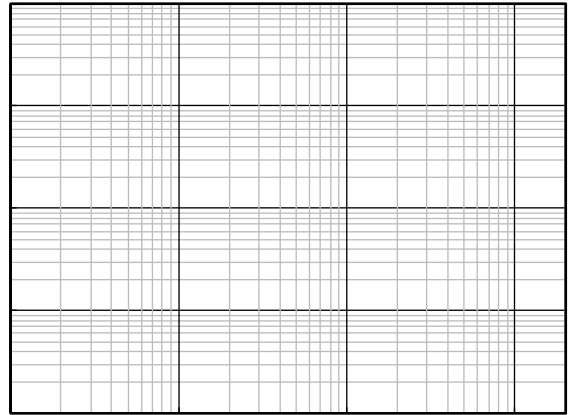
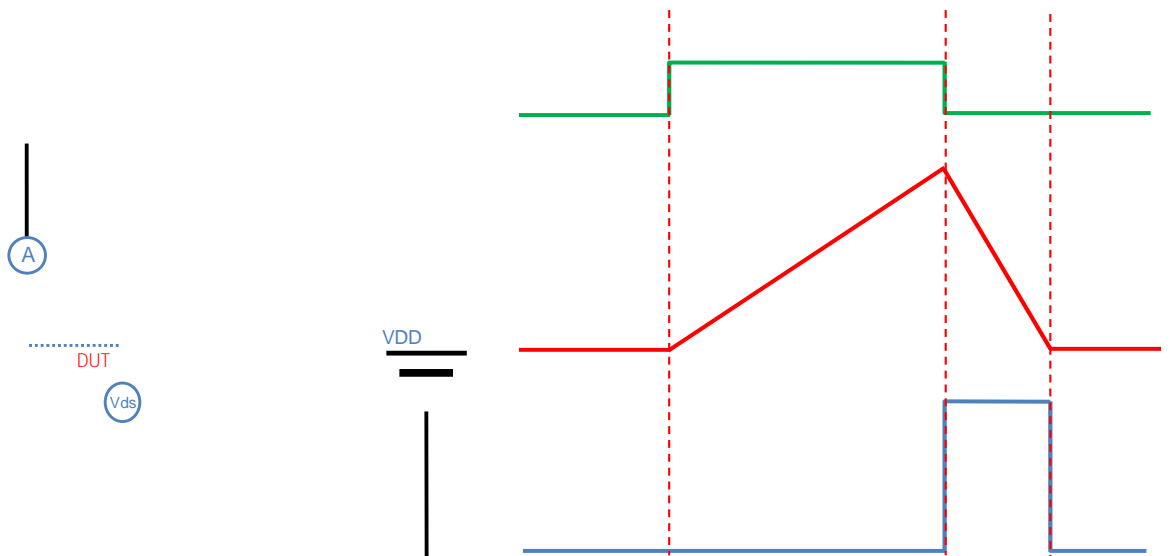


Figure 14. Safe Operation Area

## Test Circuits & Waveforms





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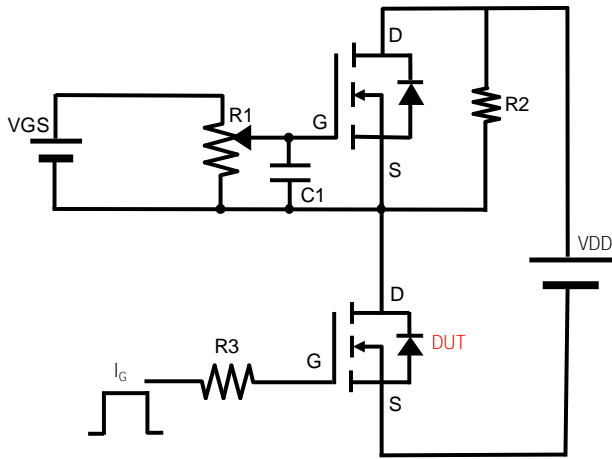


Figure B. Gate Charge Test Circuit & Waveform

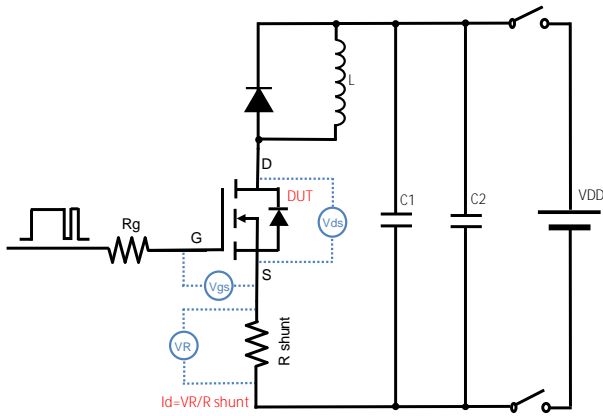


Figure C. Resistive Switching Test Circuit & Waveform

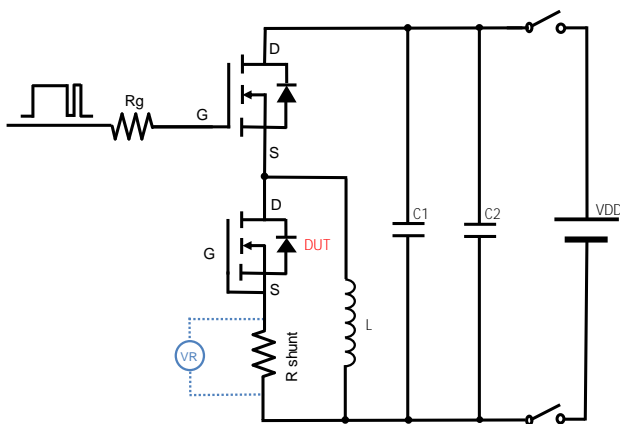


Figure D. Diode Recovery Test Circuit & Waveform





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