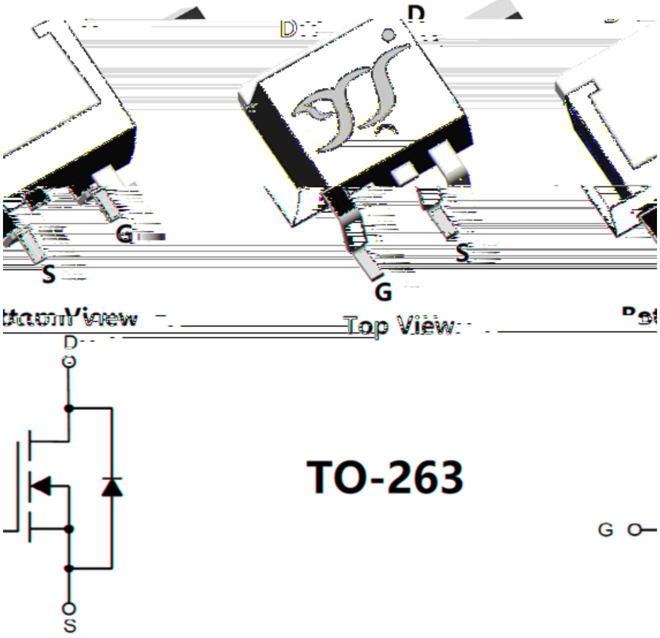
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

” V_{DS}	150V
” I_D	90A
” $R_{DS(ON)}$(at V_{GS}=10V)	11.8m

” 100% EAS Tested

” 100% V_{DS} Tested

General Description

” Split gate trench MOSFET technology

” Excellent package for heat dissipation

” High density cell design for low $R_{DS(ON)}$

” 0RLVWXUH 6HQVLWLYLW\ /HYHO

” Epoxy Meets UL 94 V-0 Flammability Rating

” Halogen Free

Applications

” Power switching application

” Uninterruptible power supply

” DC-DC convertor

v Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	150	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25	I_D	12	A
	T_A=100		7	
	T_C=25		90	
	T_C =100		56	
Pulsed Drain Current [A]		I_{DM}	250	A
Avalanche energy [B]		EAS	400	mJ
Total Power Dissipation [C]	T_A=25	P_D	3	W
	T_A=100		1.2	
	T_C=25		178	
	T_C =100		71	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +150	

vThermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	Steady-State	R -$	30	40	/W
Thermal Resistance Junction-to-Case	Steady-State	R -&	0.6	0.7	

v Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJB90G15H	F2	YJB90G15H	800	/	8000	1 ³ UHH

Typical Electrical and Thermal Characteristics Diagrams

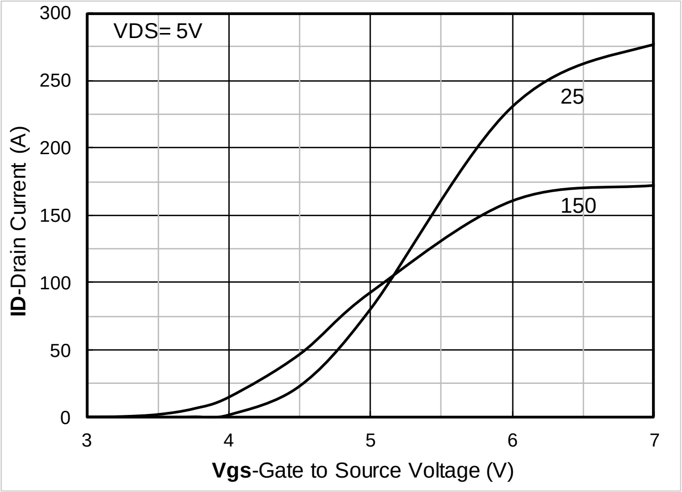
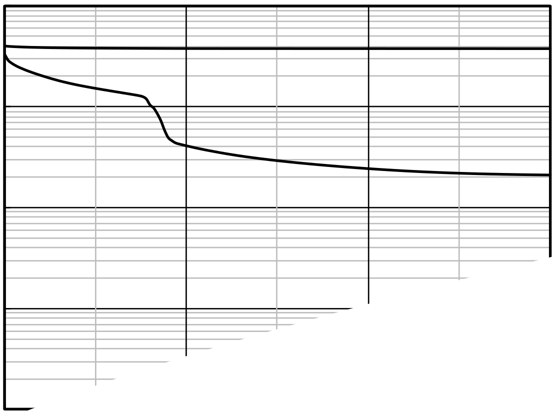


Figure 1. Output Characteristics

Figure 2. Transfer Characteristics



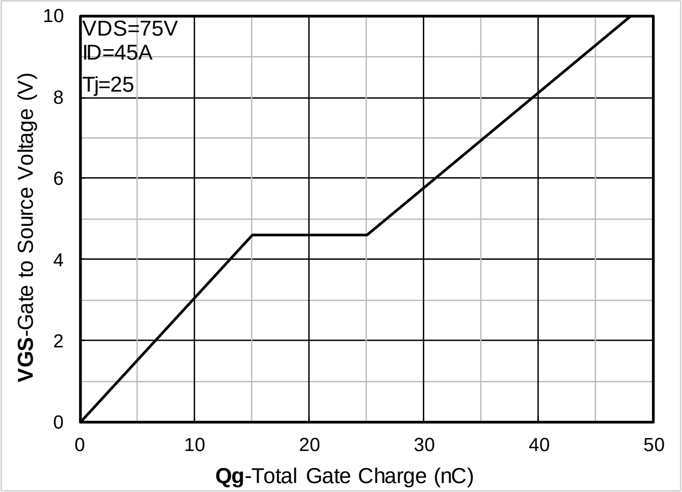


Figure 3. Capacitance Characteristics

Figure 4. Gate Charge

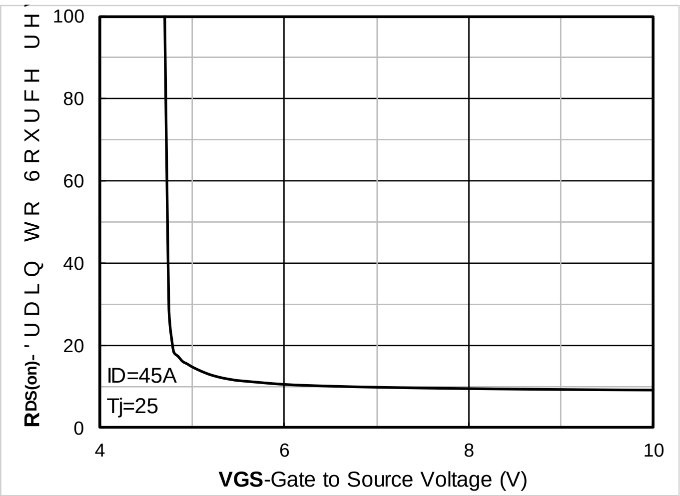
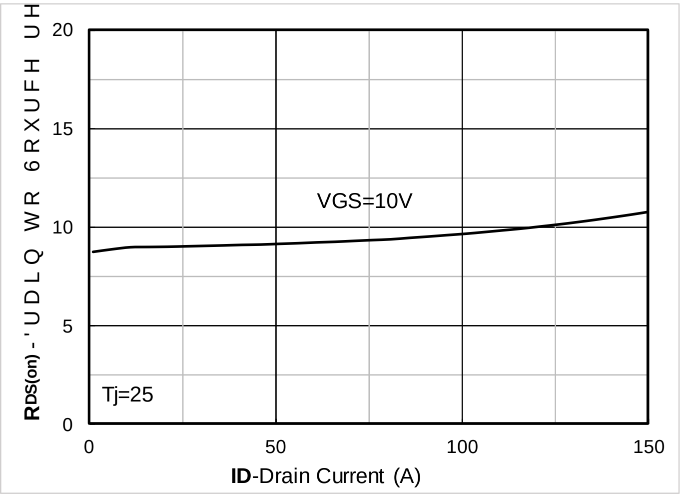


Figure 5. On-Resistance vs Gate to Source Voltage

Figure 6. Normalized On-Resistance



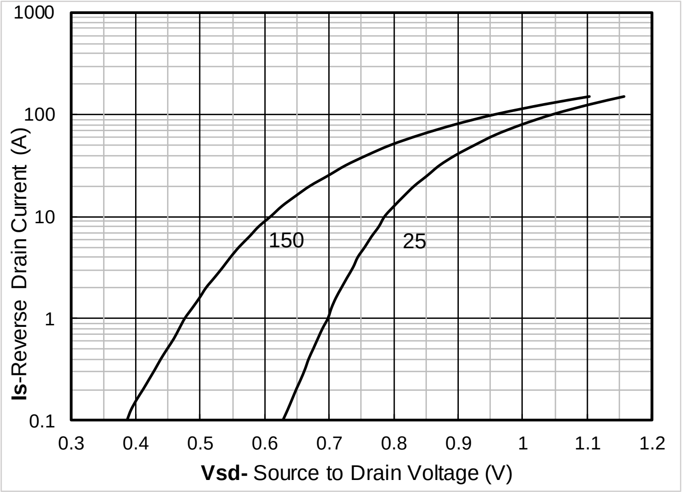
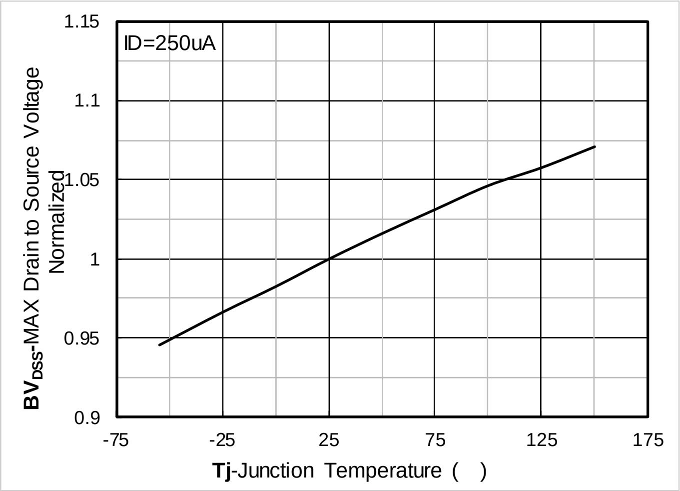


Figure 7. RDS(on) VS Drain Current

Figure 8. Forward characteristics of reverse diode



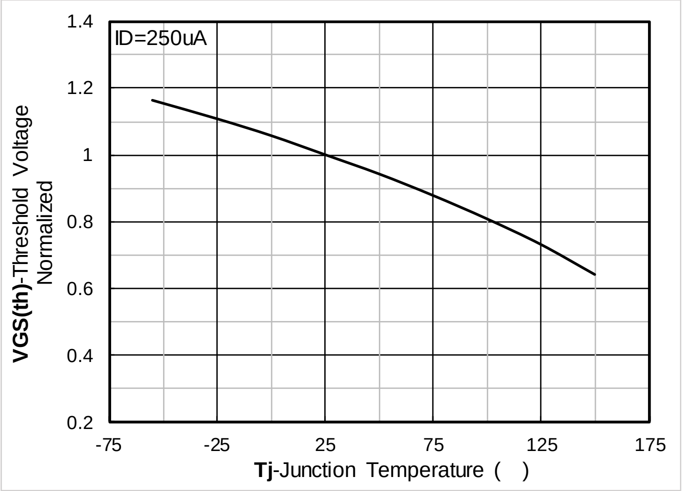
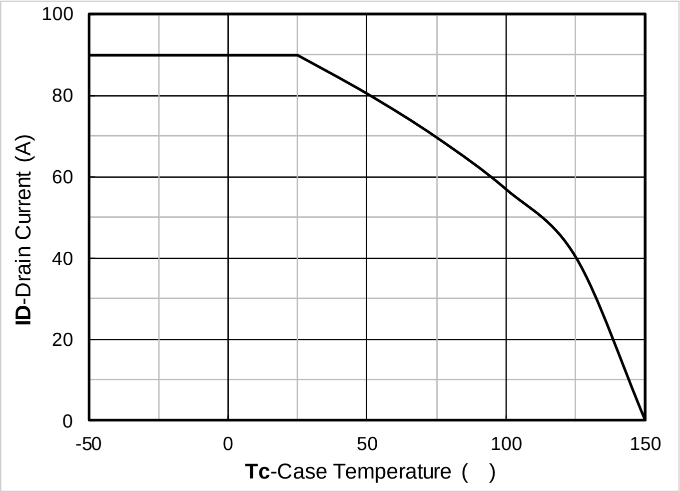


Figure 9. Normalized breakdown voltage

Figure 10. Normalized Threshold voltage



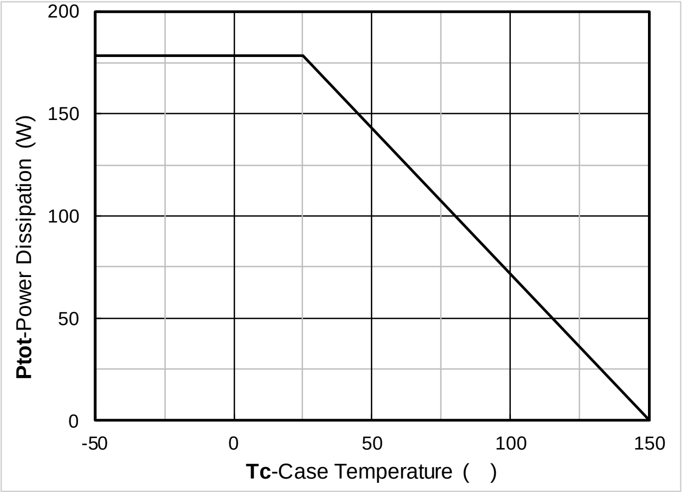
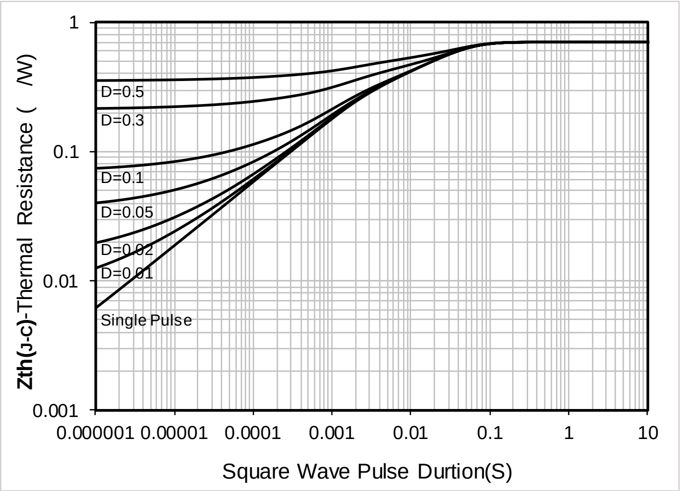


Figure 11. Current dissipation

Figure 12. Power dissipation



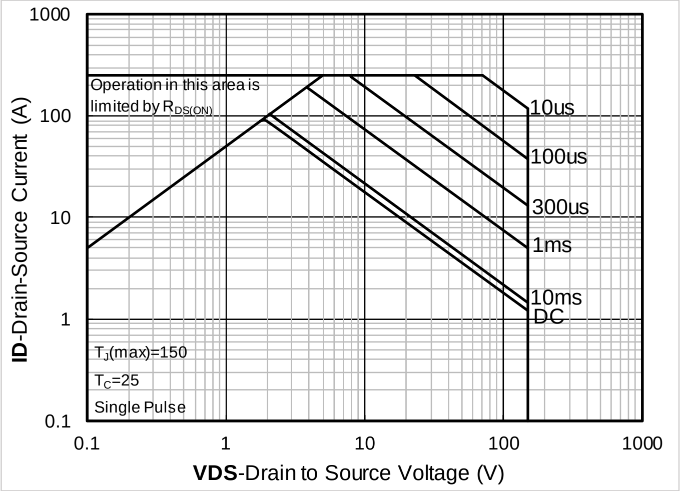


Figure 13. Maximum Transient Thermal Impedance

Figure 14. Safe Operation Area

vTest Circuits & Waveforms

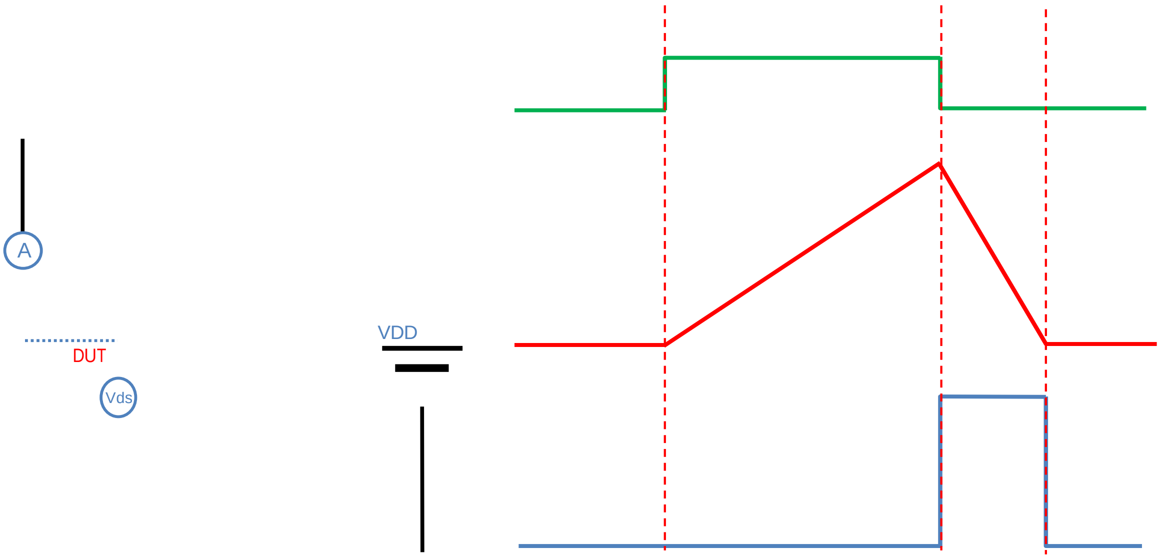


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

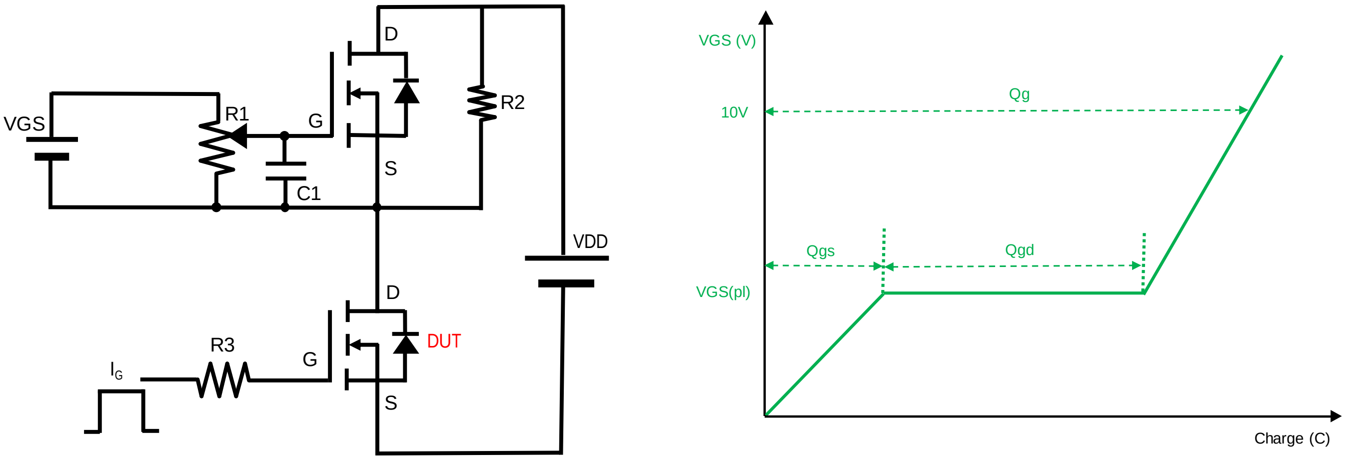


Figure B. Gate Charge Test Circuit & Waveform

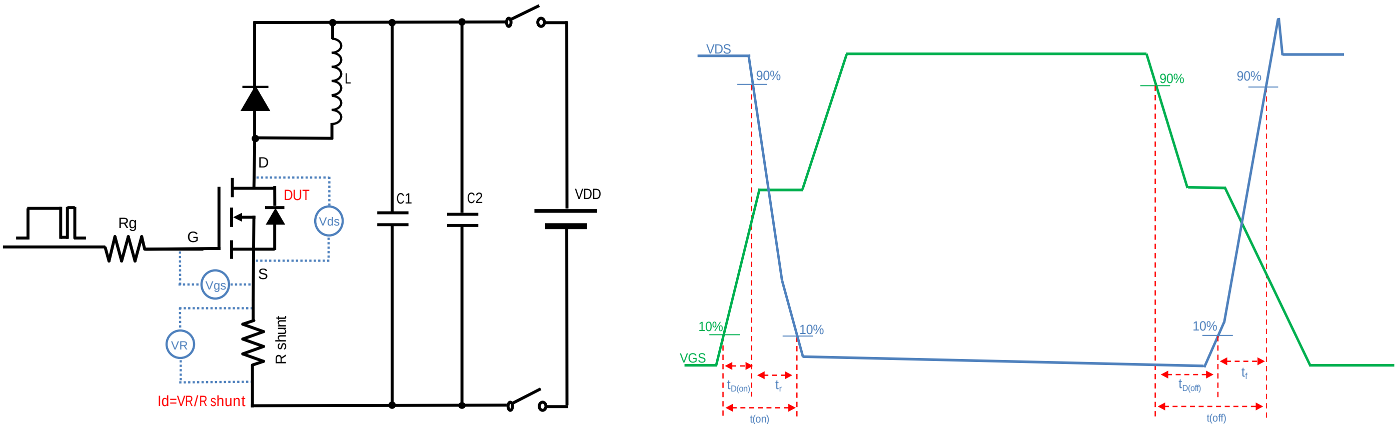


Figure C. Resistive Switching Test Circuit & Waveform

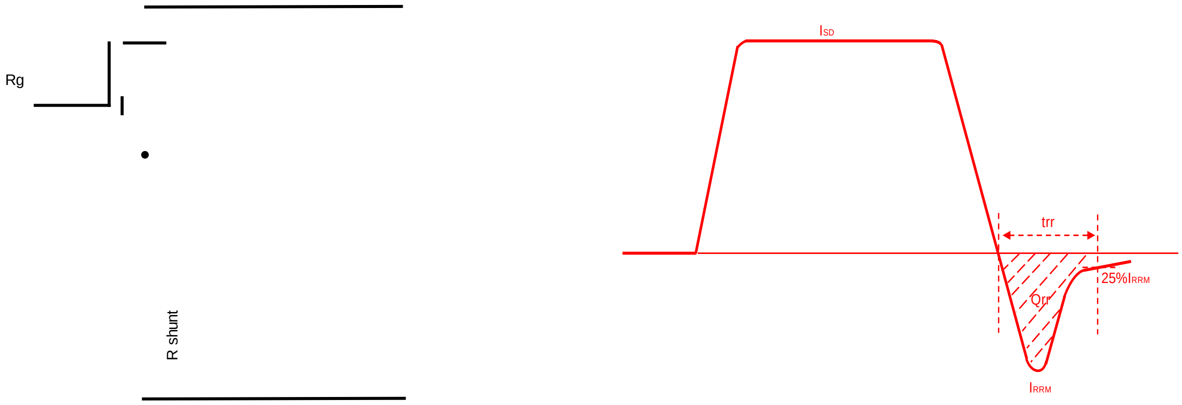
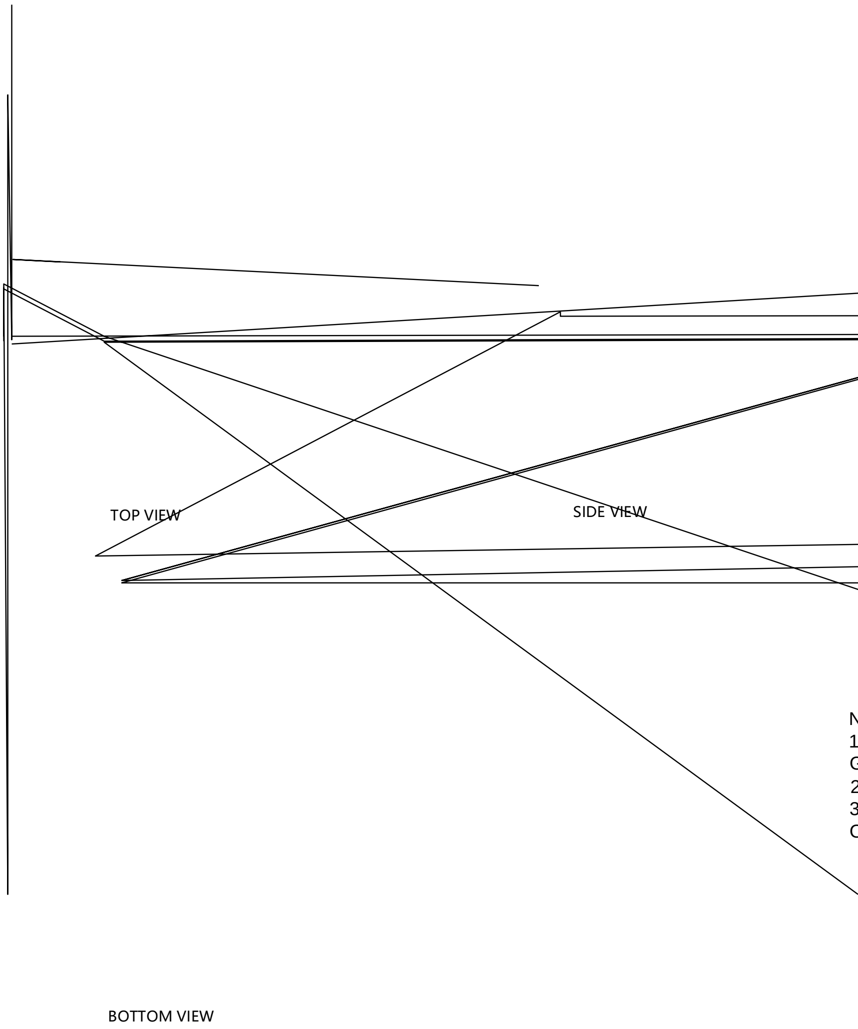


Figure D. Diode Recovery Test Circuit & Waveform

∨TO-263-HY Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.010	0.000	---	0.250
A2	0.174	0.180	0.186	4.430	4.580	4.730
b	0.028	0.032	0.036	0.720	0.820	0.920
b2	0.046	0.050	0.054	1.180	1.280	1.380
c	0.013	0.015	0.018	0.330	0.390	0.450
c2	0.048	0.050	0.053	1.220	1	1.340
D1						
D2	0.303	0.315	0.327	7.700		8.300
E	0.571	0.591	0.610	14.500		15.500
E1	0.337	0.341	0.348	8.550		8.850
E2						
e	0.200BSC			5.080BSC		
L	0.070		0.110	1.790		2.790
L1						
L2	0.030		0.070	0.770		1.770
L3	0.197REF					
θ	0°		8°	0°		8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.