



YJD12N10B

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	100V
I_D	12A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	120m
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	135m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Trench Power MV MOSFET technology
 Excellent package for heat dissipation
 High density cell design for low $R_{DS(ON)}$
 Moisture Sensitivity Level 1
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

Power management functions
 DC-DC convertor

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	3	A
	$T_A=100^\circ C$		2	
	$T_C=25^\circ C$		12	
	$T_C=100^\circ C$		8.5	
Pulsed Drain Current ^A		I_{DM}	25	A
Avalanche energy ^B		EAS	12	mJ
Total Power Dissipation ^C	$T_A=25^\circ C$	P_D	3	W
	$T_A=100^\circ C$		1.5	
	$T_C=25^\circ C$		50	
	$T_C=100^\circ C$		25	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +175	$^\circ C$

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	R	40	50	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	R	2.5	3	



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Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D$	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	
		$V_{DS}=100V, V_{GS}=0V, T_J=175^\circ C$	-	-	100	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D$	1.1	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=10A$	-	93	120	
		$V_{GS}=4.5V, I_D=10A$	-	97	135	
Diode Forward Voltage	V_{SD}	$I_S=12A, V_{GS}=0V$	-	-	1.2	V
Gate resistance	R_G	$f=1MHz$	-	4	-	
Maximum Body-Diode Continuous Current	I_S		-	-	12	A



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Typical Electrical and Thermal Characteristics Diagrams

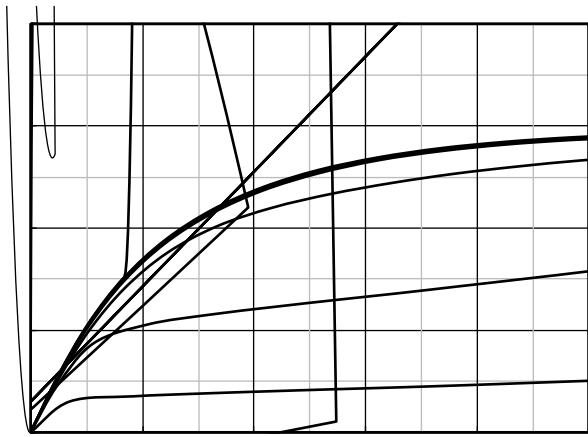


Figure 1. Output Characteristics

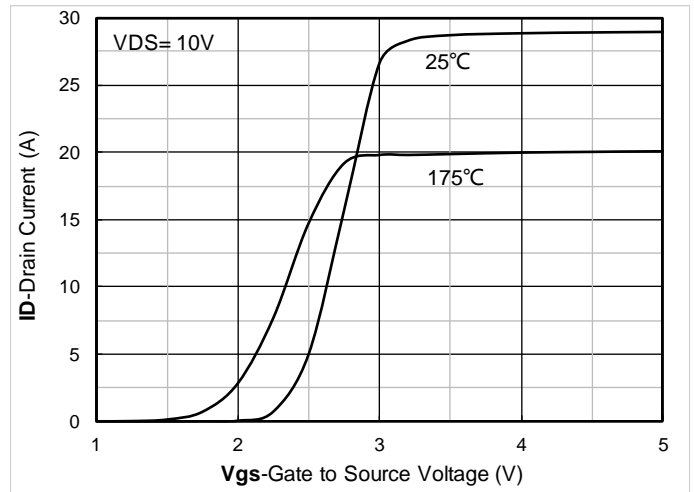


Figure 2. Transfer Characteristics

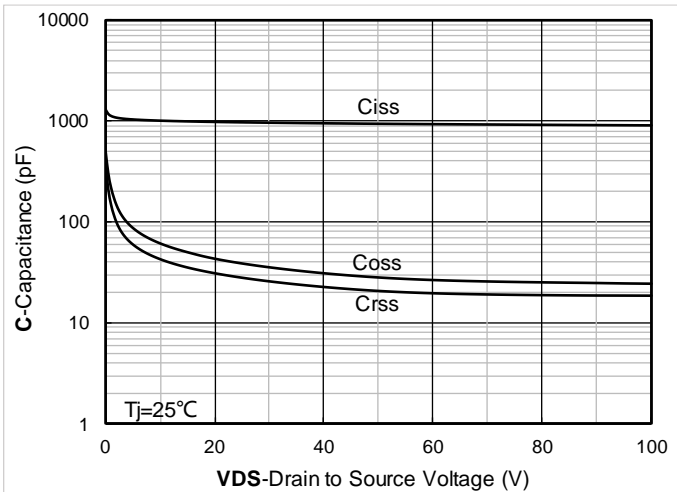


Figure 3. Capacitance Characteristics

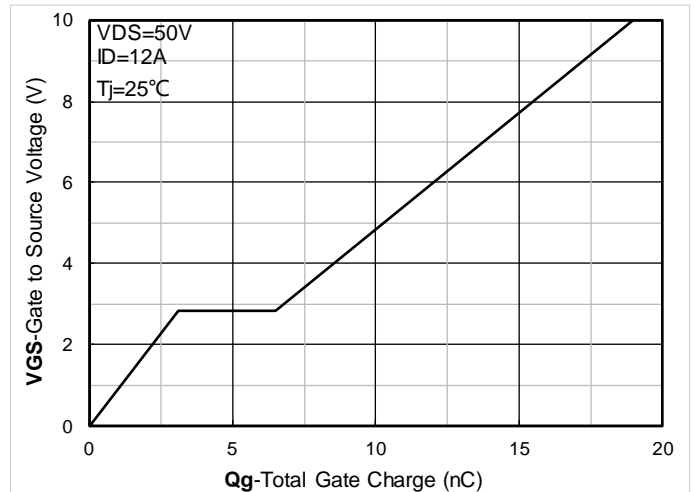


Figure 4. Gate Charge

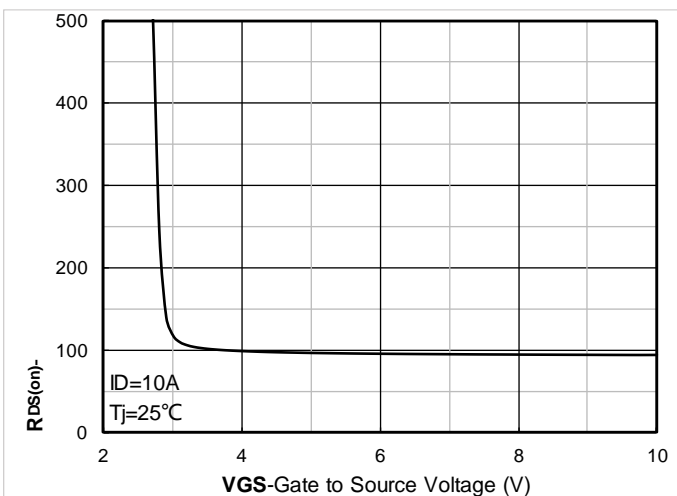


Figure 5. On-Resistance vs Gate to Source Voltage

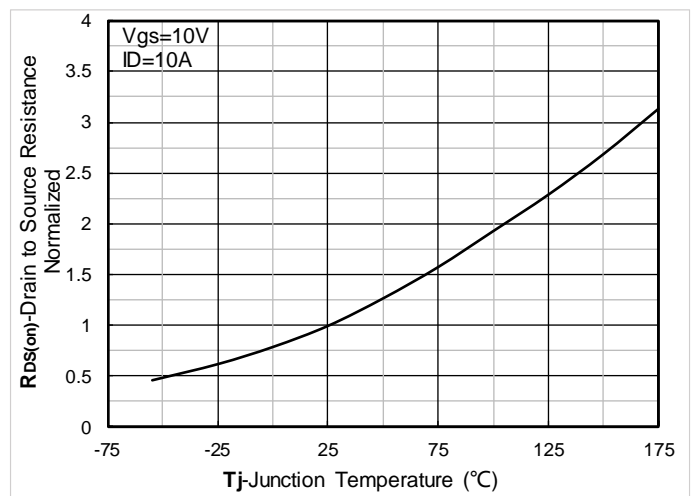


Figure 6. Normalized On-Resistance



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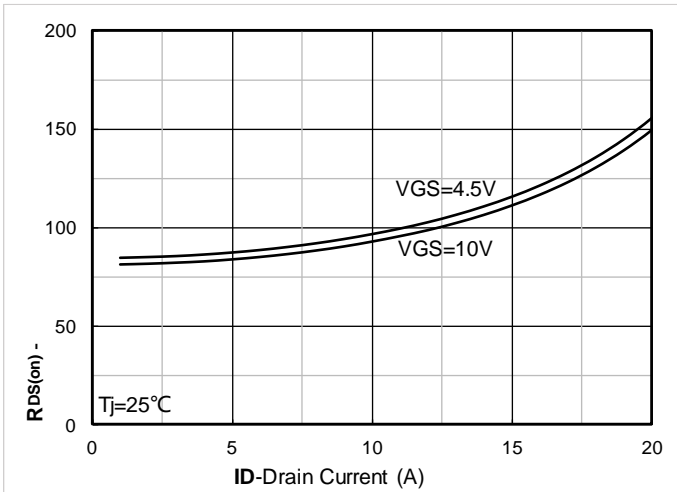


Figure 7. RDS(on) VS Drain Current

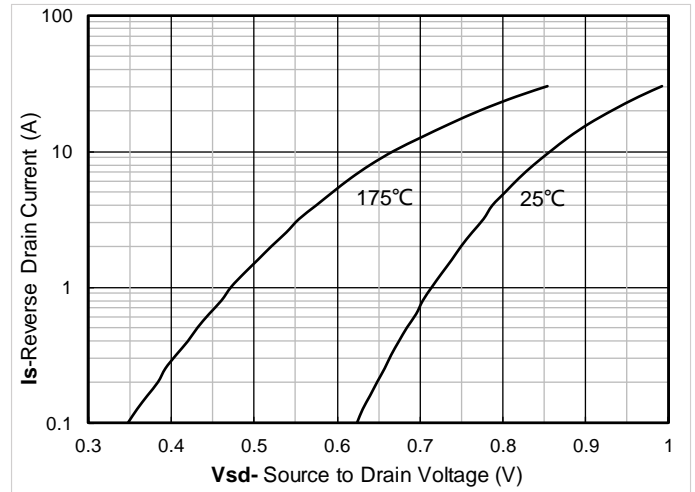


Figure 8. Forward characteristics of reverse diode

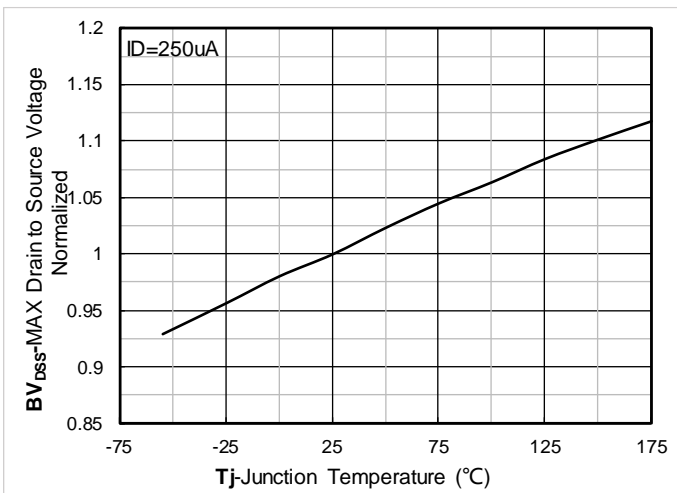


Figure 9. Normalized breakdown voltage

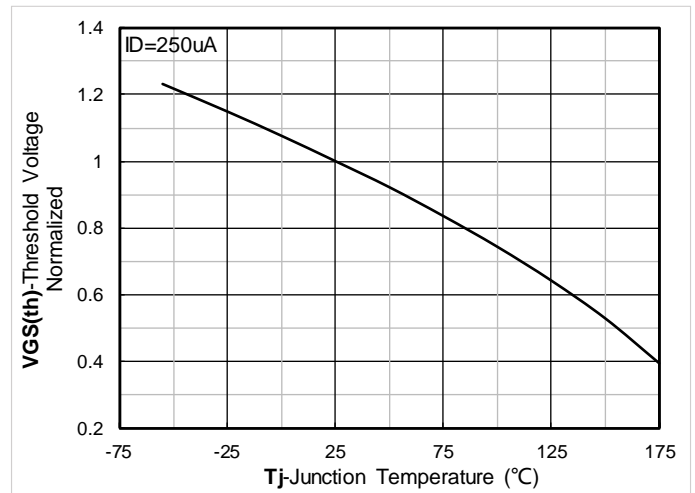


Figure 10. Normalized Threshold voltage

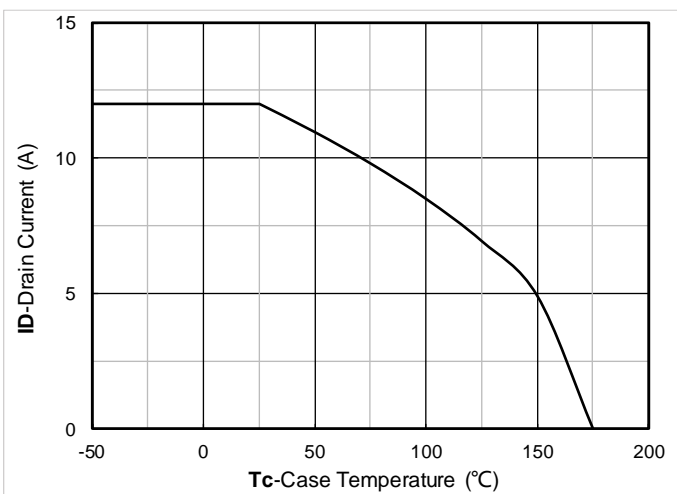


Figure 11. Current dissipation

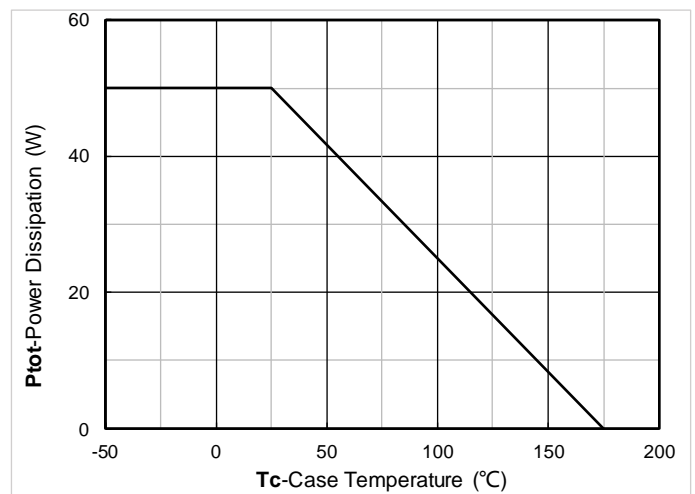


Figure 12. Power dissipation

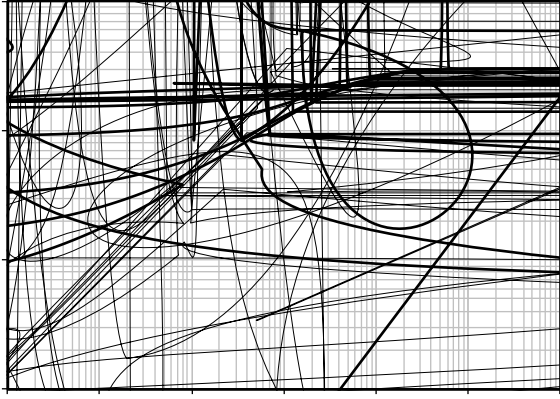


Figure 13. Maximum Transient Thermal Impedance

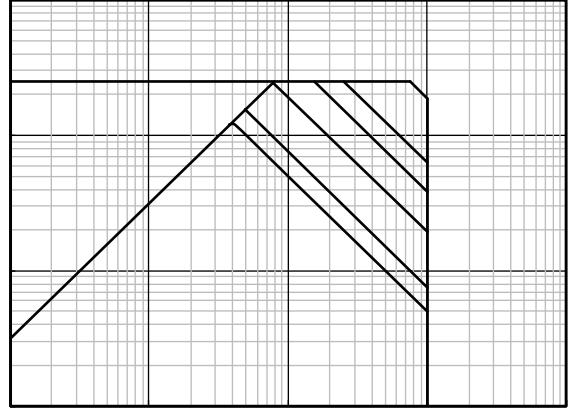


Figure 14. Safe Operation Area

Test Circuits & Waveforms

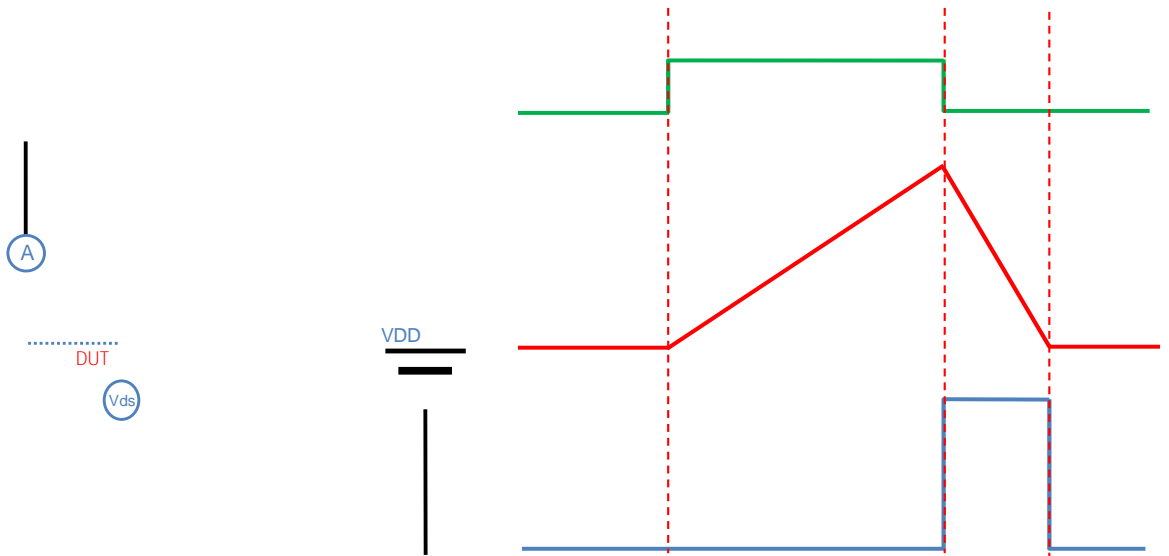
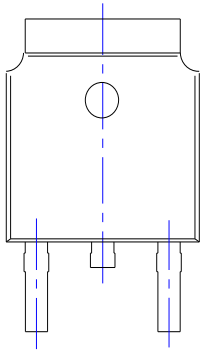


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



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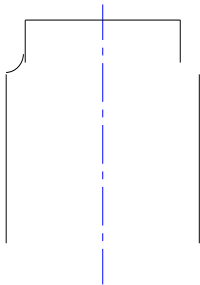
TO-252-B Package information



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES			
	MIN.	NOM.		
A1	0.000			
A2	0.087	0.091		
A3	0.035	0.039		
b	0.026	0.030		
c	0.018	0.020		
D	0.256	0.260		
D1				
D2	0.181	0.189		
E	0.390	0.398		
E1	0.236	0.240		

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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