



YJD28GP10A

P-Channel Enhancement Mode Field Effect Transistor

Product Summary

| | |
|------------------------------------|---------|
| V_{DS} | -100V |
| I_D | -28A |
| $R_{DS(ON)}$ (at $V_{GS}=-10V$) | 58 mohm |
| $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) | 65 mohm |
| 100% EAS Tested | |
| 100% V_{DS} Tested | |

General Description

Split gate trench MOSFET technology

" Excellent package for heat dissipation

High density cell(d)-5(e)9(i)9(ty)5(c)-8(e)-9 Tf1 0 0 1 352.87 664.9 ce



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Electrical Characteristics ($T_J=25$ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|-----------------------------------|--------------|---------------------------|----------|------|------|-------|
| Static Parameter | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS}=0V, I_D=-250$ | -100 | | | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS}=-100V, V_{GS}=0V$ | $T_J=25$ | | -1 | |
| | | | $T_J=55$ | | -5 | |
| Gate-Body Leakage Current | I_{GSS} | $V_{GS}=20V, V_{DS}=0V$ | | | 100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=$ | -1.0 | -1.8 | -2.5 | V |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}=-10V, I_D=-15A$ | | 42 | 58 | m |
| | | $V_{GS}=-4.5V, I_D=-7A$ | | 46 | 65 | |
| Diode Forward Voltage | V_{SD} | $I_S=-20A, V_{GS}=0V$ | | | | |



Typical Performance Characteristics

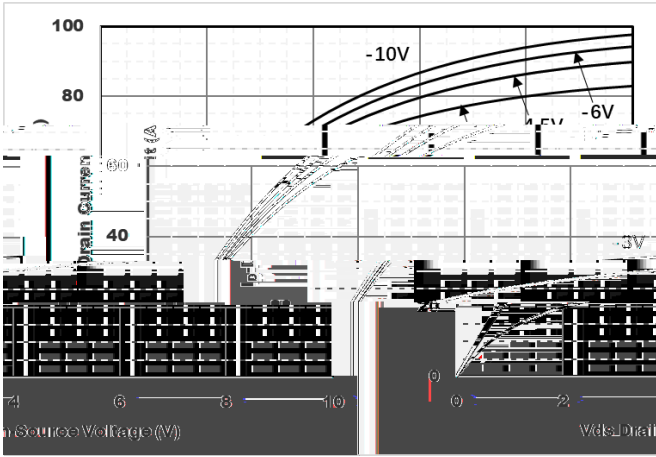


Figure1. Output Characteristics

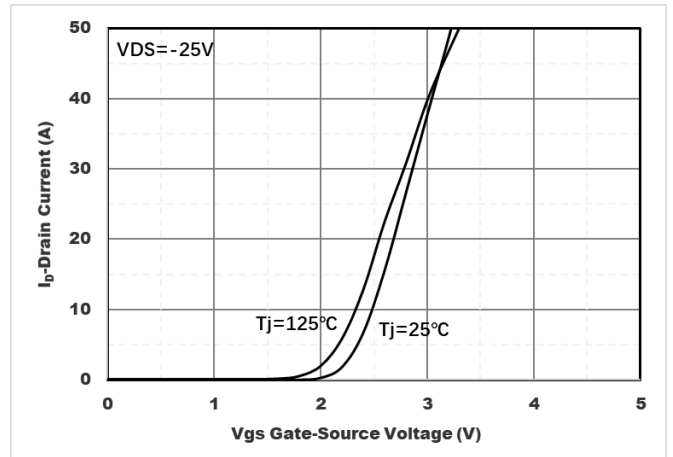


Figure2. Transfer Characteristics

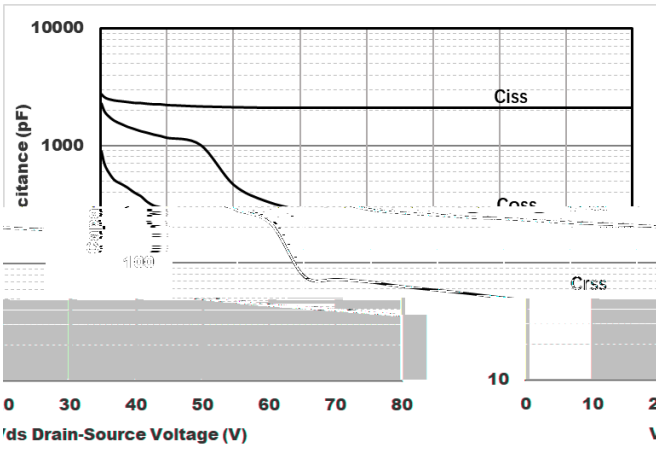


Figure3. Capacitance Characteristics

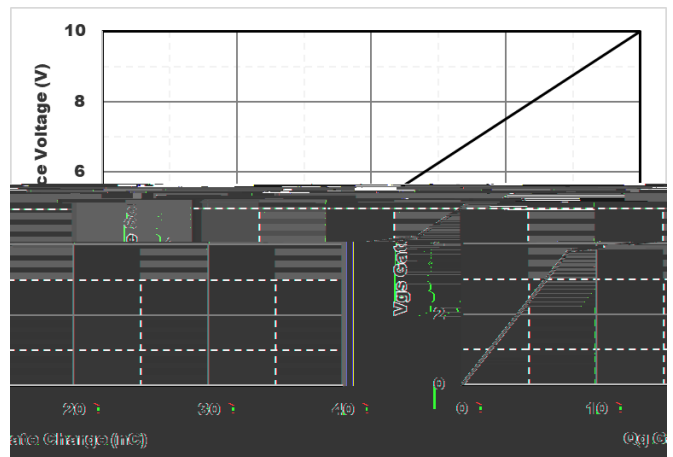


Figure4. Gate Charge

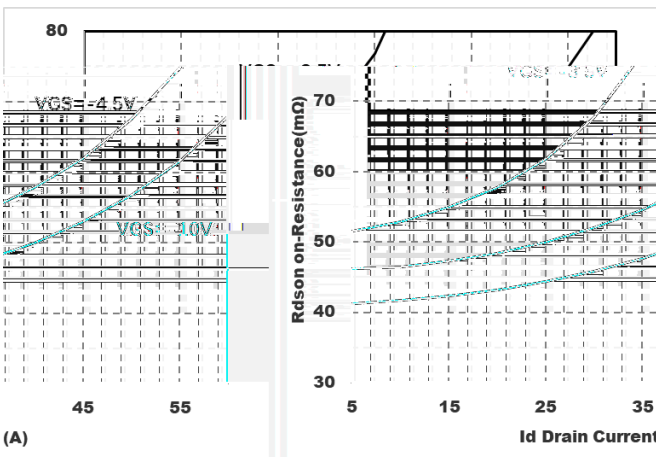


Figure5. : On-Resistance vs. Drain Current and Gate Voltage

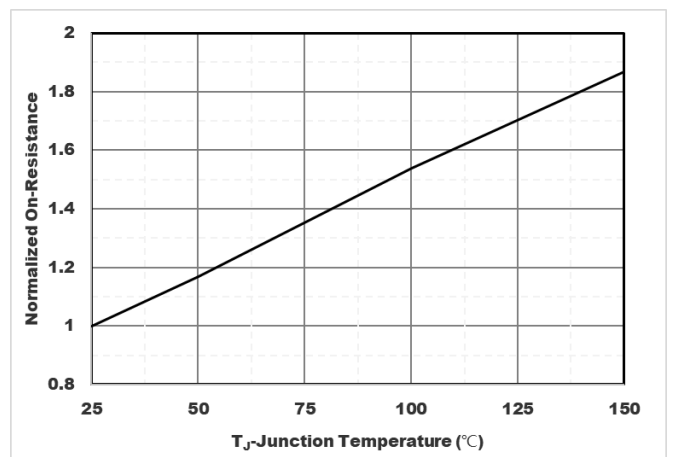


Figure6. Normalized On-Resistance



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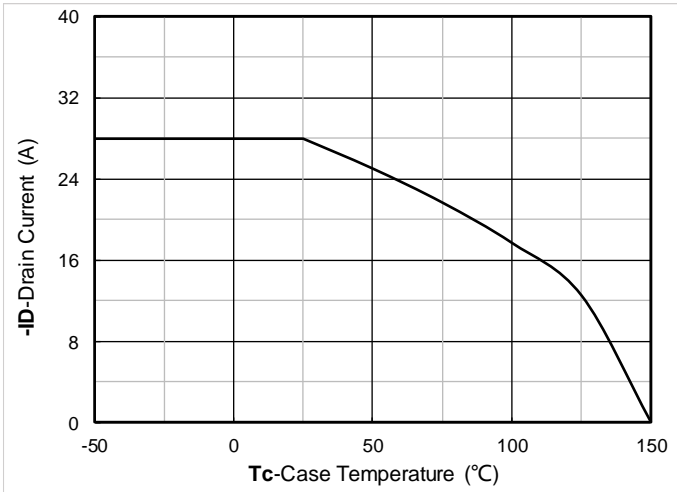


Figure7. Drain current

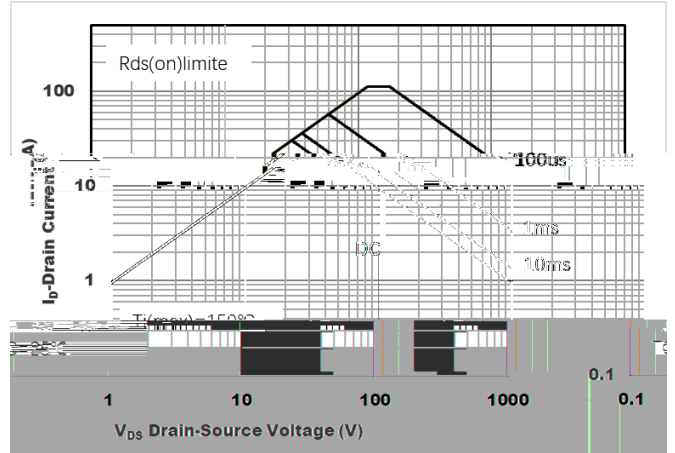


Figure8.Safe Operation Area

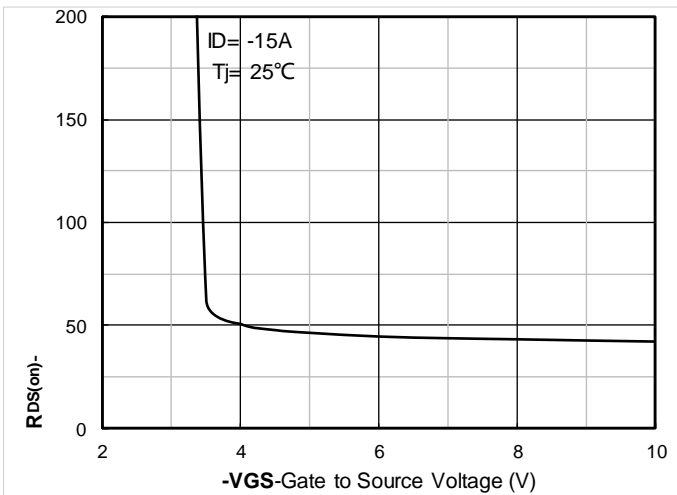


Figure 9. On-Resistance vs Gate to Source Voltage

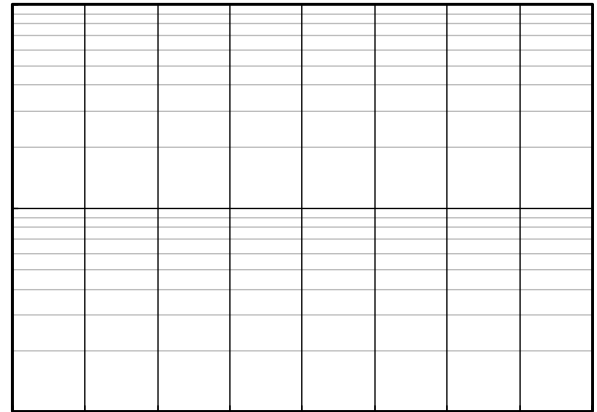


Figure 10. Forward characteristics of reverse diode

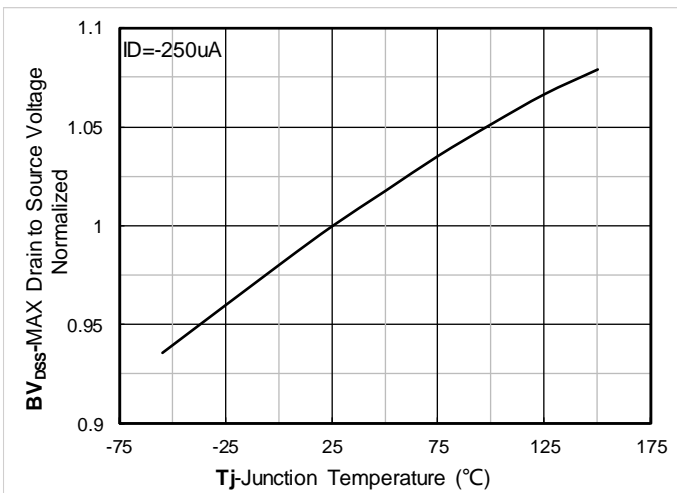


Figure 11. Normalized breakdown voltage

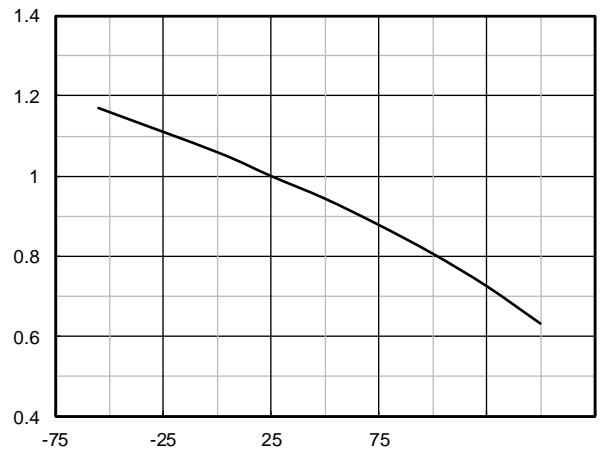


Figure 12. Normalized Threshold voltage



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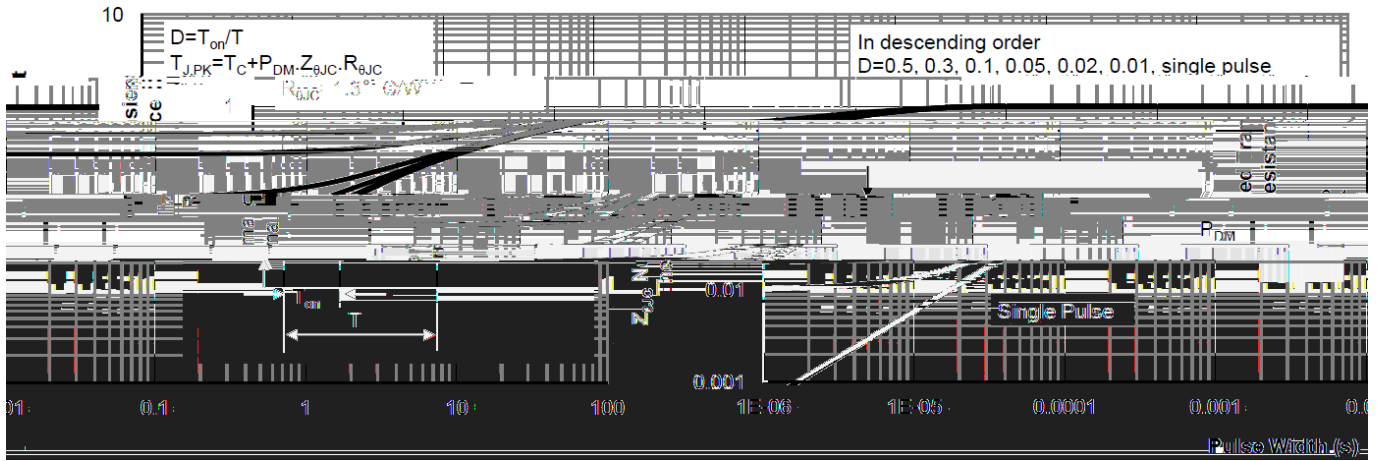
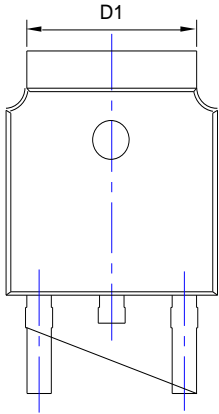


Figure13.Normalized Maximum Transient thermal impedance

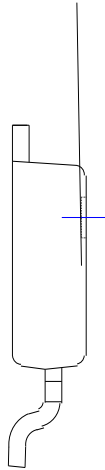


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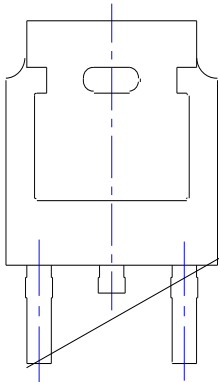
TO-252-B Package Information



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SUGGESTED SOLDER PAD LAYOUT

| SYMBOL | DIMENSIONS | | | | |
|--------|------------|-------|--|--|--|
| | MIN. | NOM. | | | |
| A1 | 0.000 | | | | |
| A2 | 0.087 | 0.091 | | | |
| A3 | 0.035 | 0.039 | | | |
| b | 0.026 | 0.030 | | | |
| c | 0.018 | 0.020 | | | |
| D | 0.256 | 0.260 | | | |
| D1 | | | | | |
| D2 | 0.181 | 0.189 | | | |
| E | 0.390 | 0.398 | | | |
| E1 | 0.236 | 0.240 | | | |

NOTE:
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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