



N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	250V
I_D	8A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	470m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$



YJD470N25H

Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D$	250	-		



Typical Electrical and Thermal Characteristics Diagrams

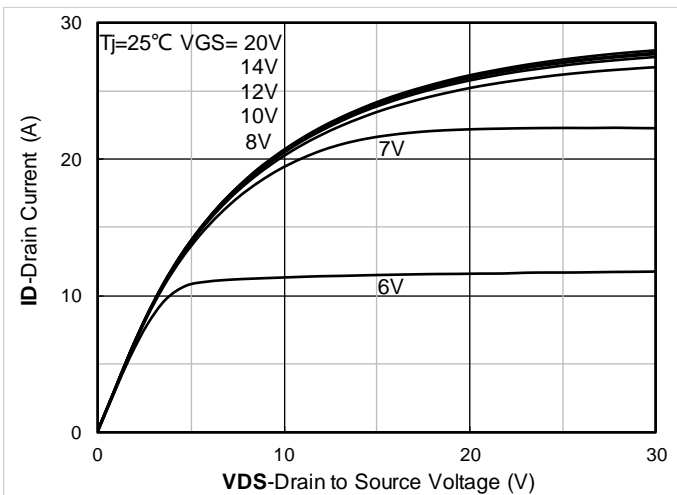


Figure 1. Output Characteristics

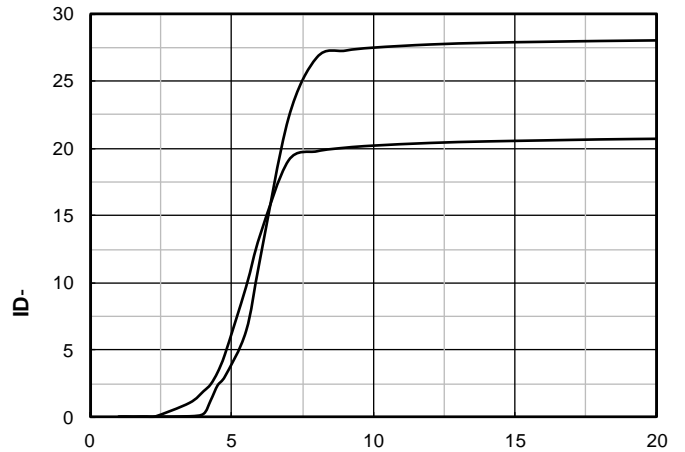


Figure 2. Transfer Characteristics

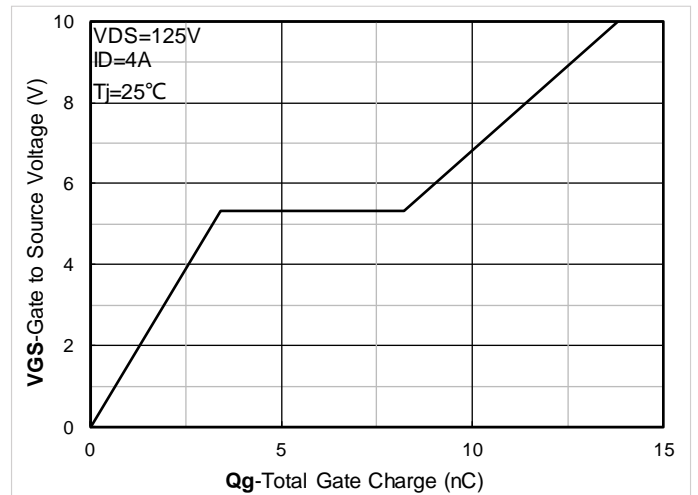


Figure 3. Capacitance Characteristics

Figure 4. Gate Charge

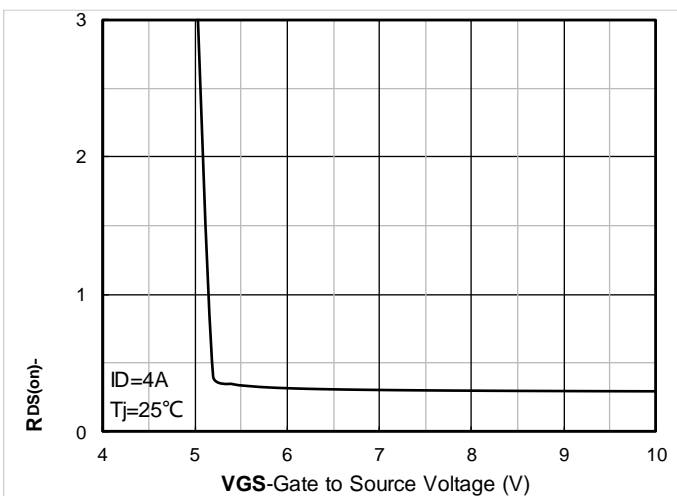


Figure 5. On-Resistance vs Gate to Source Voltage

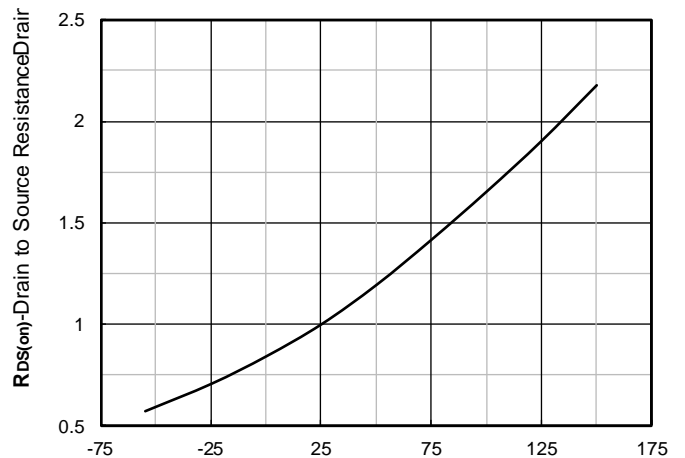


Figure 6. Normalized On-Resistance



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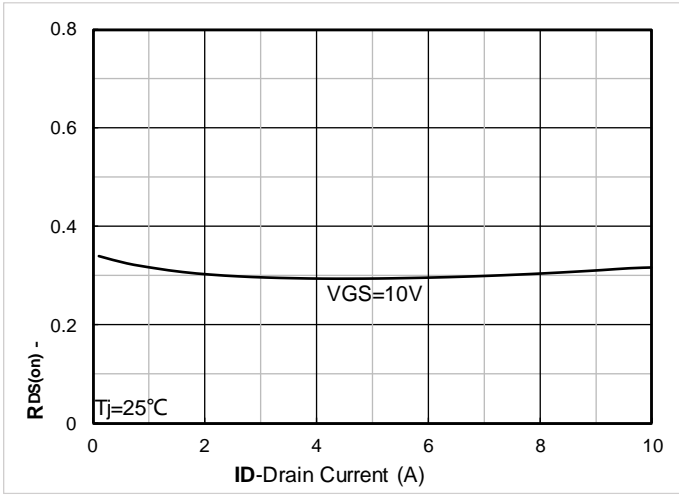


Figure 7. RDS(on) VS Drain Current

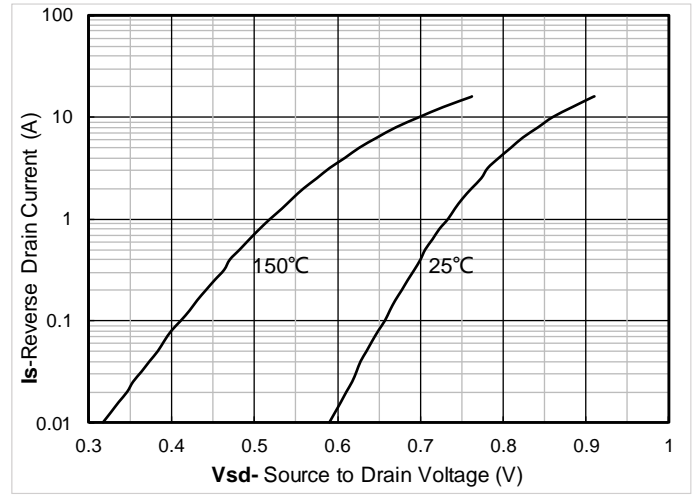


Figure 8. Forward characteristics of reverse diode

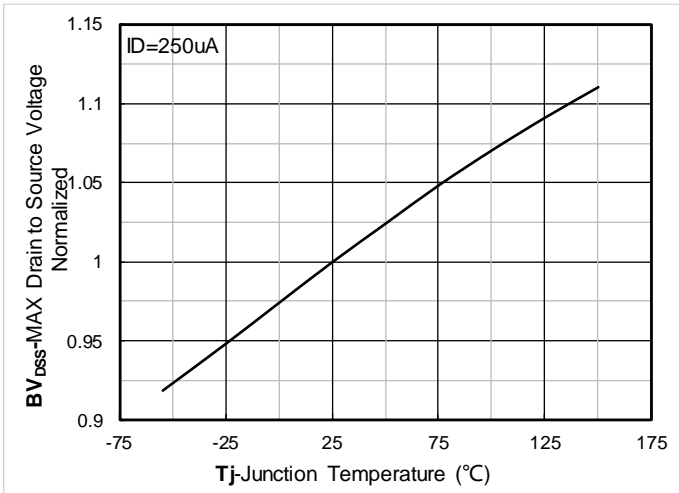


Figure 9. Normalized breakdown voltage

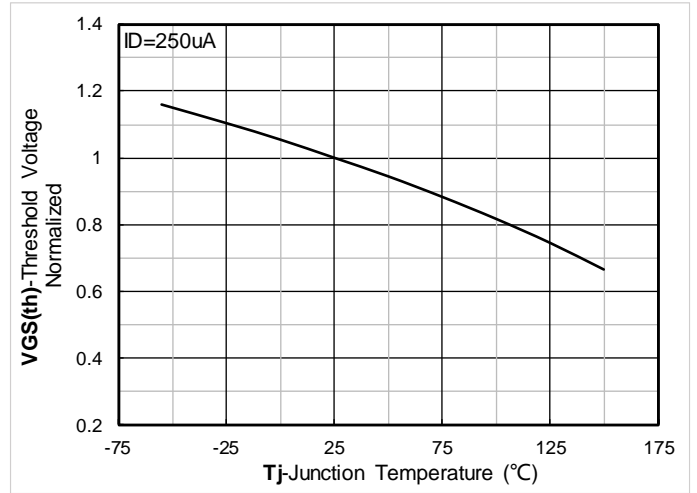


Figure 10. Normalized Threshold voltage

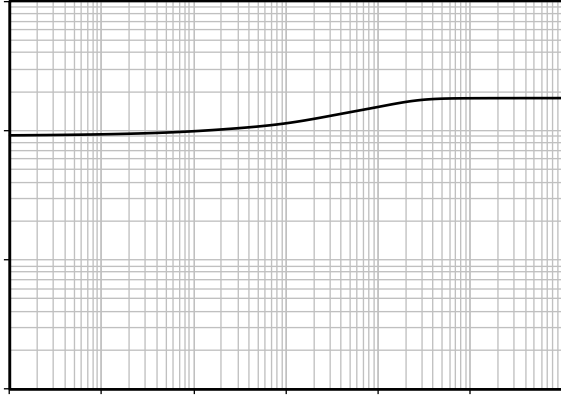


Figure 13. Maximum Transient Thermal Impedance

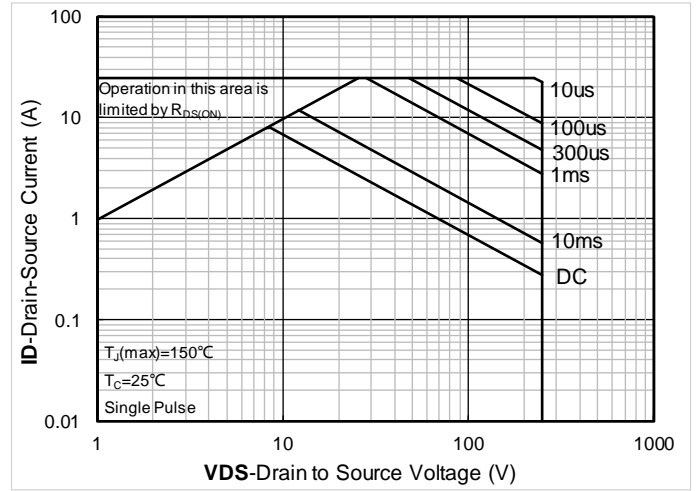


Figure 14. Safe Operation Area

Test Circuits & Waveforms

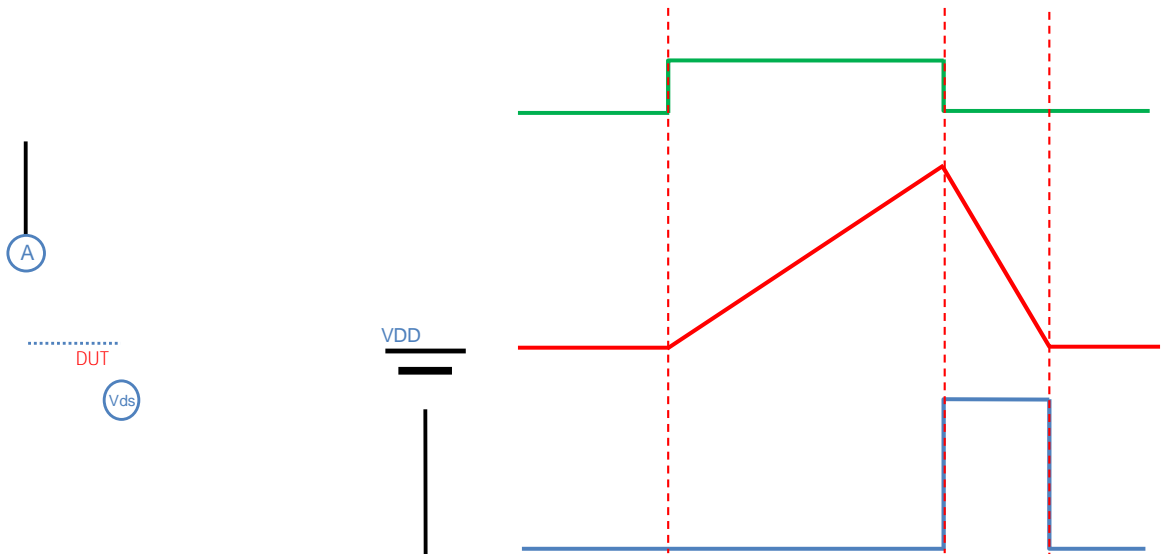


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

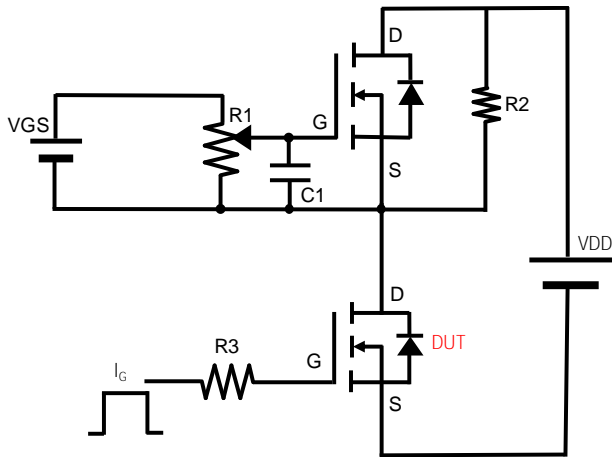


Figure B. Gate Charge Test Circuit & Waveform

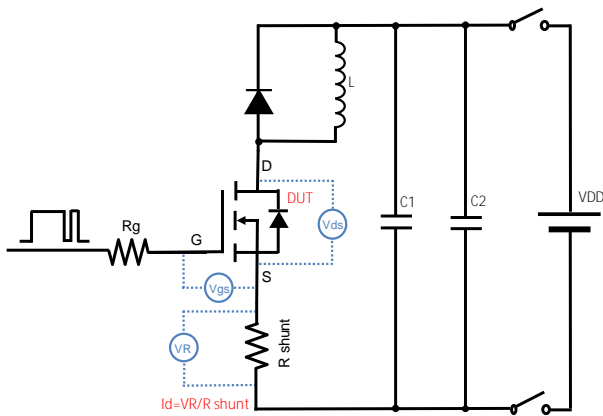


Figure C. Resistive Switching Test Circuit & Waveform

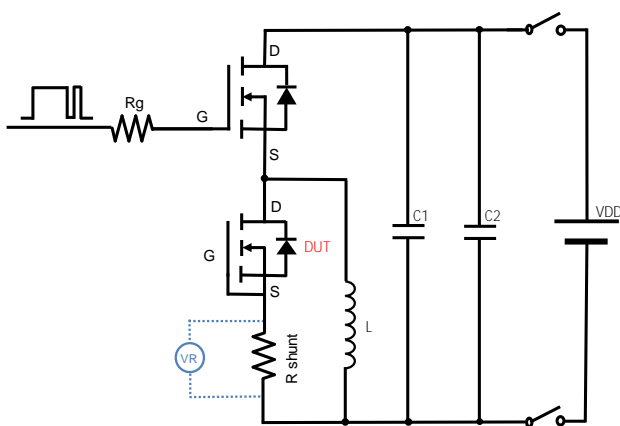
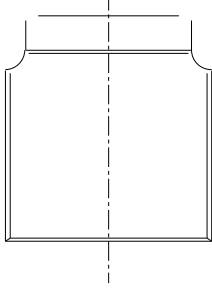


Figure D. Diode Recovery Test Circuit & Waveform



TO-252-C Package information



TOP VIEW



SIDE VIEW

BOTTOM VIEW

SUGGESTED SOLDER PAD LAYOUT



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