



N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	30V
D	50A
$R_{DS(ON)}$ (at $V_{GS}= 10V$)	7.3mohm
$R_{DS(ON)}$ (at $V_{GS}= 4.5V$)	11.5mohm
100% EAS Tested	
100% V_{DS} Tested	

General Description

J F B CEI J
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Moisture Sensitivity Level 1
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free



YJD50N03A

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250 7	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	7
		V _{DS} =30V, V _{GS} =0V, T _J =150°C			100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = 20V, V _{DS} =0V			100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250 7	1.0	1.5	2.2	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =15A		5.4	7.3	m
		V _{GS} = 4.5V, I _D =15A		9.5	11.5	
Diode Forward Voltage	V _{SD}	I _S =15A, V _{GS} =0V		0.85	1.2	V
Maximum Body-Diode Continuous Current	I _S				50	A
Gate resistance	R _G	f=1MHz		4		
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ		1015		pF
Output Capacitance	C _{oss}			201		
Reverse Transfer Capacitance	C _{rss}			164		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =20V, I _D =20A		23.6		nC
Gate-Source Charge	Q _{gs}			3.9		
Gate-Drain Charge	Q _{gd}			7		
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=100A/us		0.2		
Reverse Recovery Time	t _{rr}			5		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =20V, I _D =2A, R _{GEN} =3		7		ns
Turn-on Rise Time	t _r			19		
Turn-off Delay Time	t _{D(off)}			24		
Turn-off fall Time	t _f			24		

A. Pulse Test: Pulse Width 300us, Duty cycle 2%.

B. T_J=25, V_{DD}=25V, V_G=10V, L=0.5mH, I_{AS}=14.5A

C. R_{JA} is the sum of the junction-to-Case and Case-to-ambient thermal resistance, where the Case thermal reference is defined as the solder mounting surface of the drain pins. R_{JC} is guaranteed by design, while R_{JA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



Typical Performance Characteristics

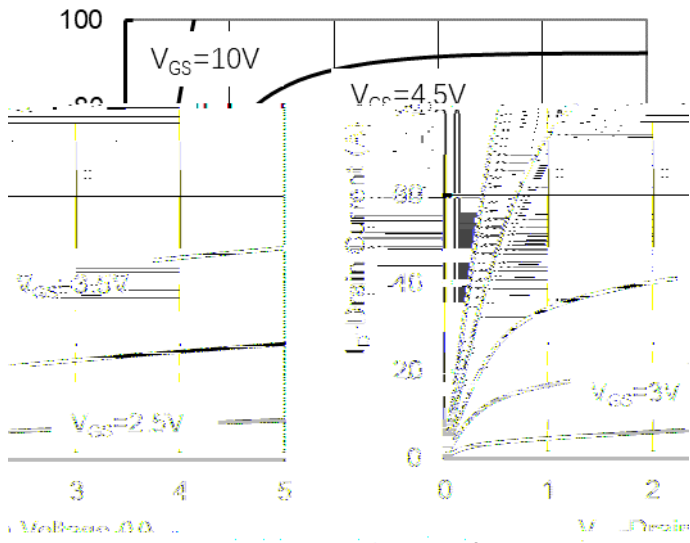


Figure 1. Output Characteristics

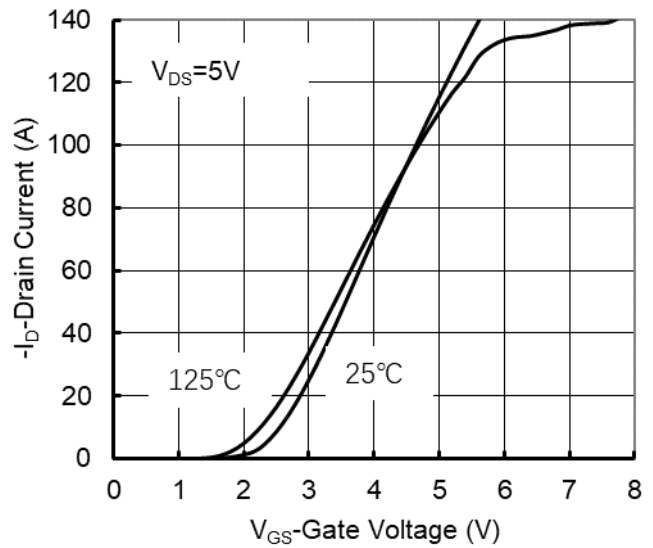


Figure 2. Transfer Characteristics

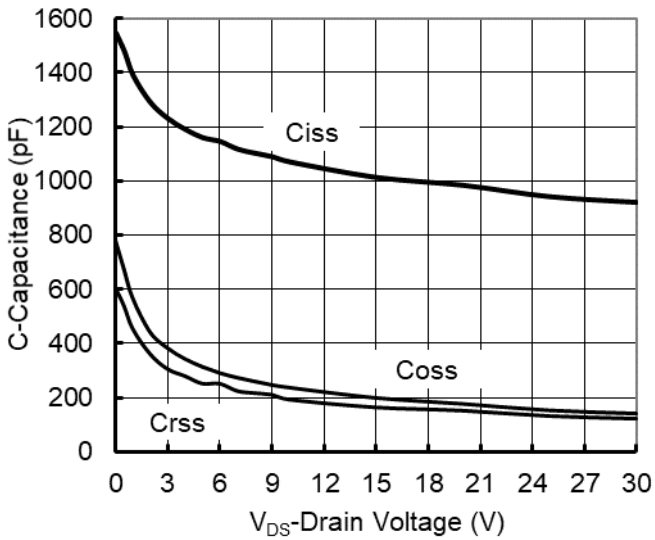


Figure 3. Capacitance Characteristics

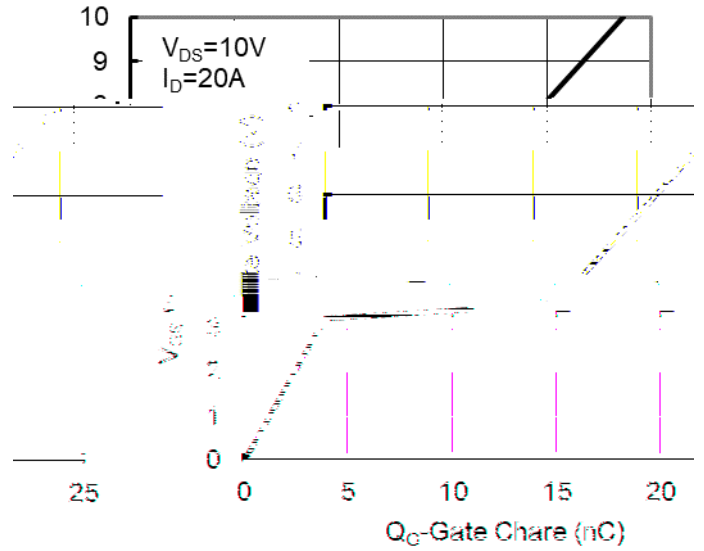


Figure 4. Gate Charge

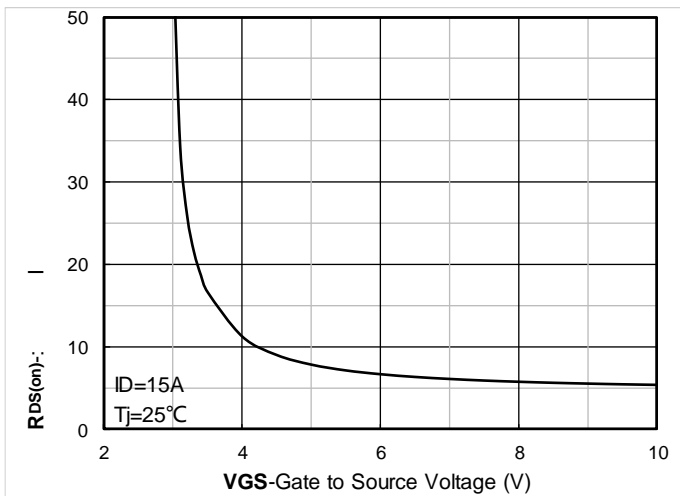


Figure 5. On-Resistance vs Gate to Source Voltage

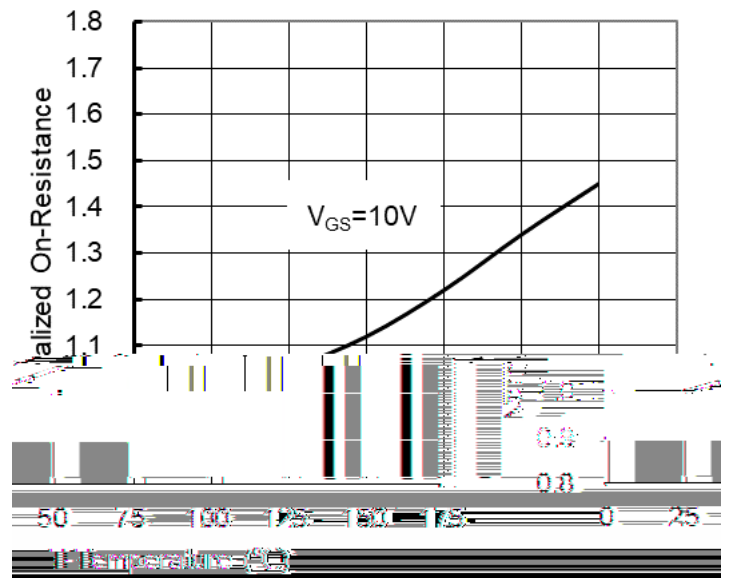


Figure 6. On-Resistance vs. Junction Temperature



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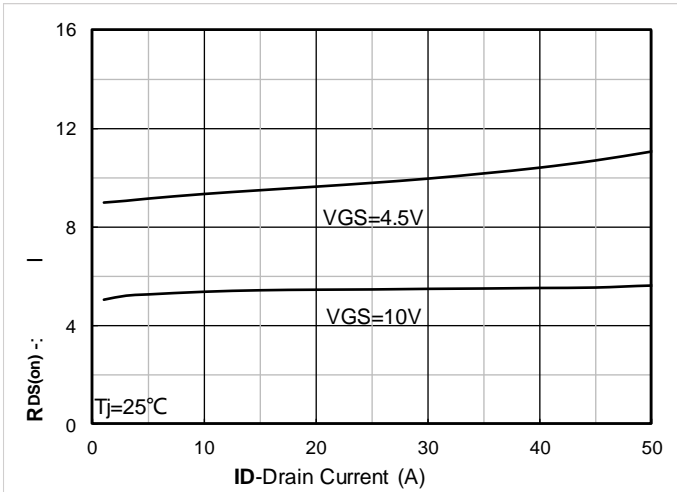


Figure 7. RDS(on) VS Drain Current

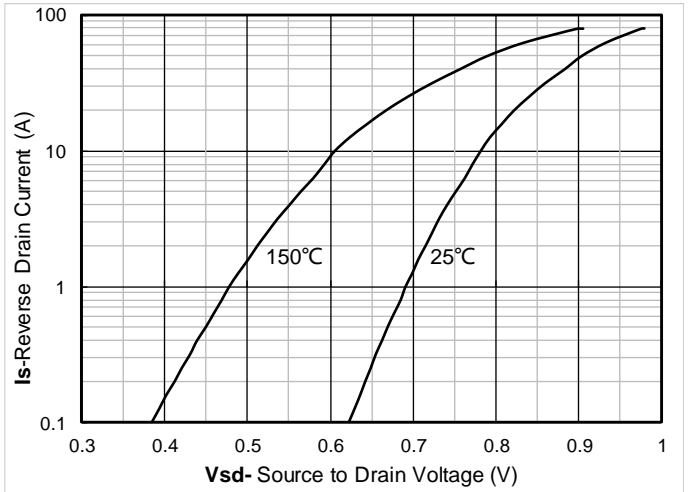


Figure 8. Forward characteristics of reverse diode

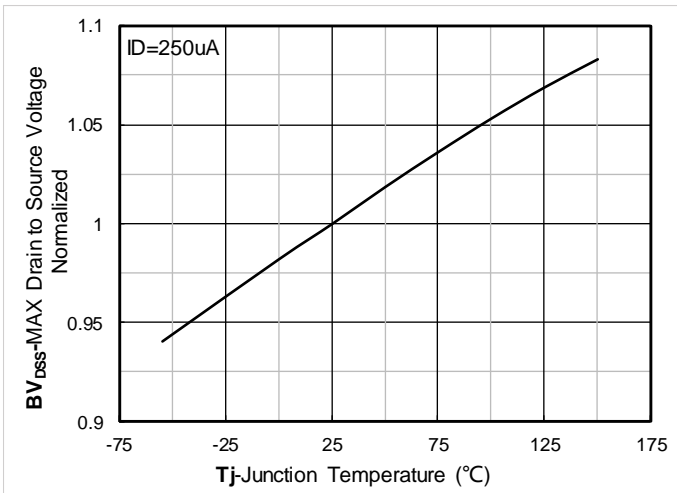


Figure 9. Normalized breakdown voltage

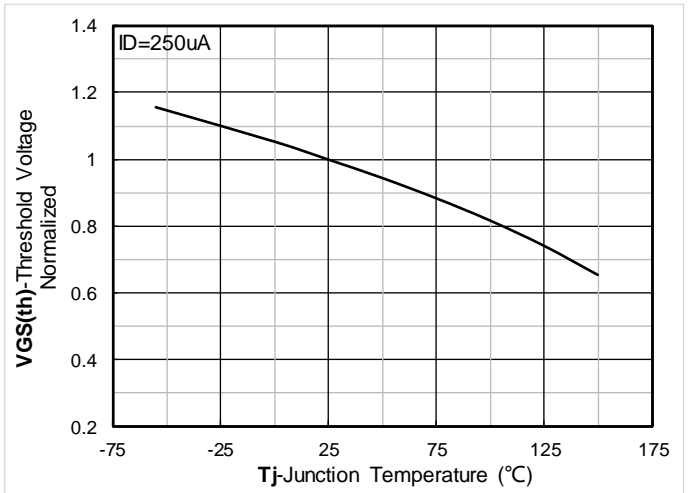


Figure 10. Normalized Threshold voltage

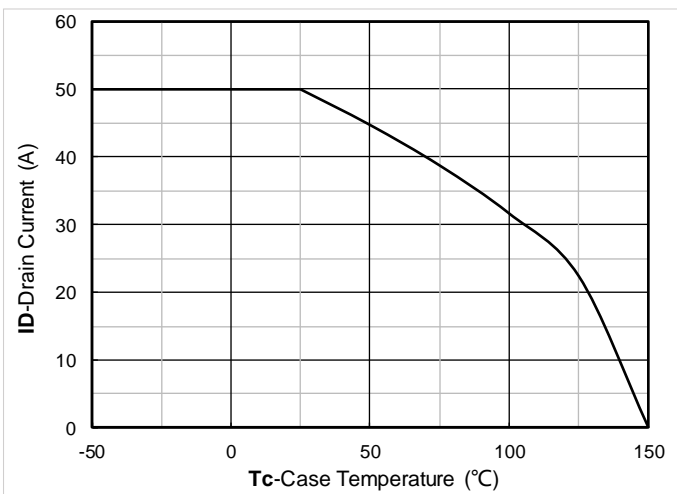


Figure 11. Current dissipation

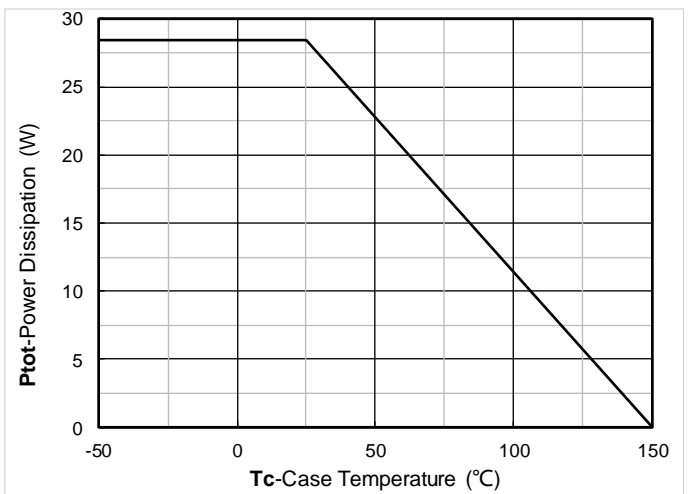


Figure 12. Power dissipation

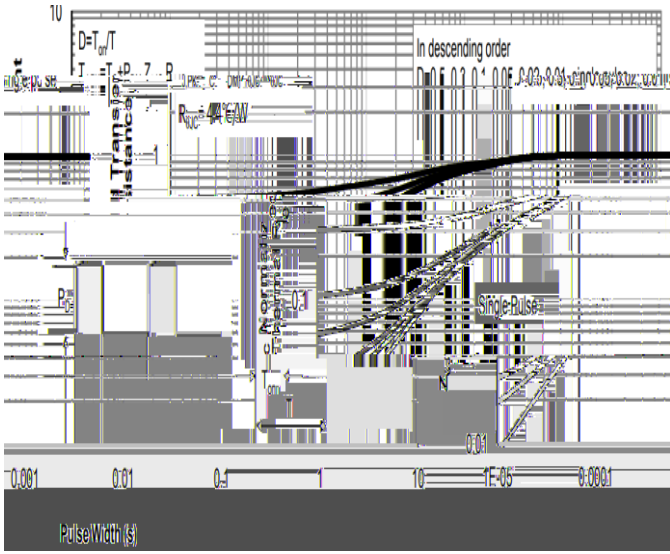


Figure 13. Normalized Maximum Transient Thermal Impedance

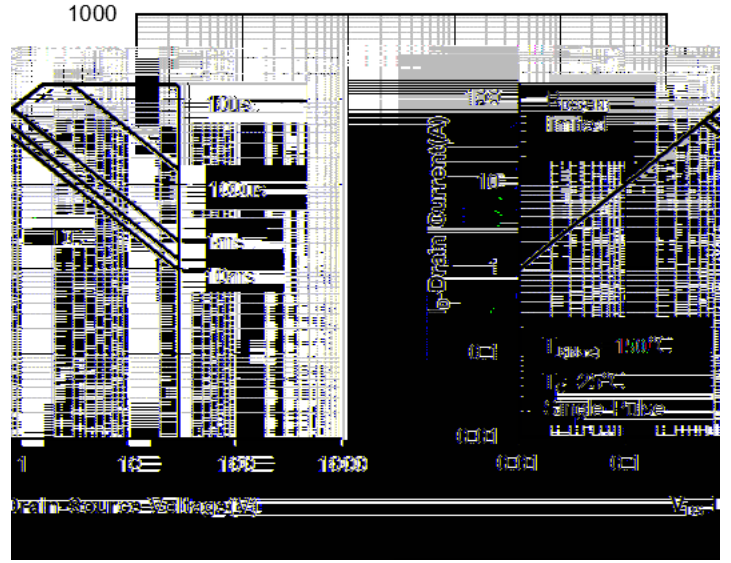
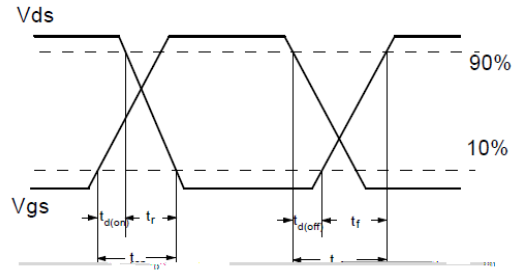
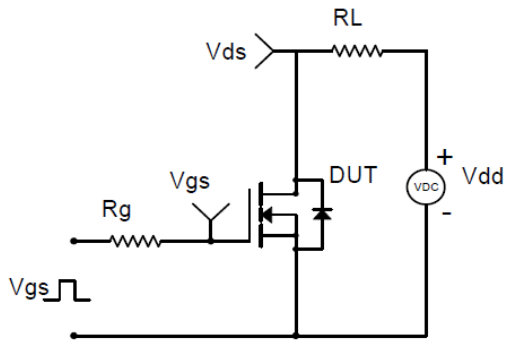
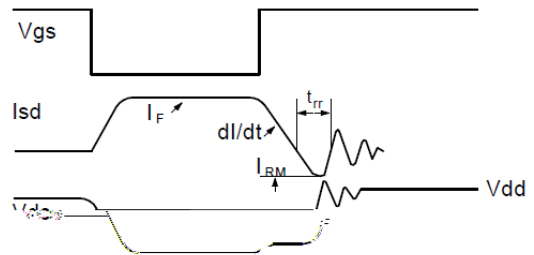
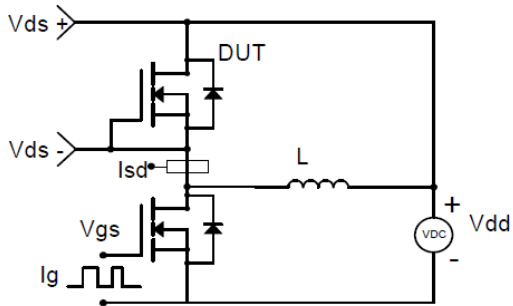


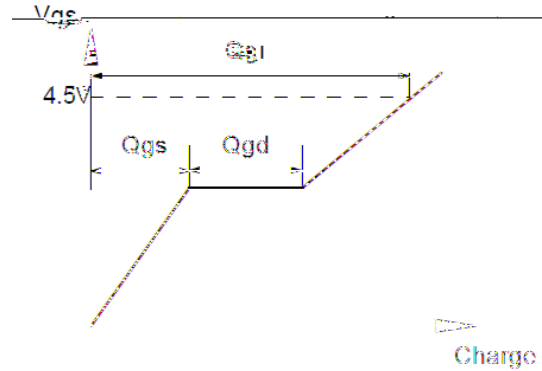
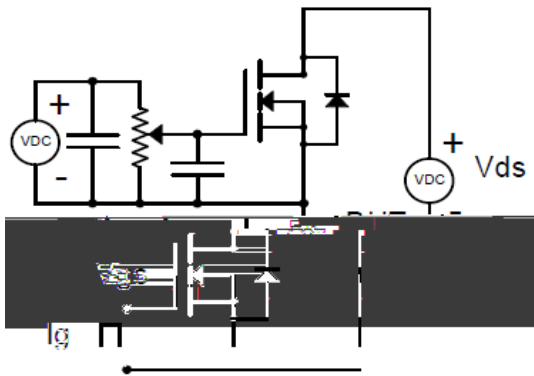
Figure 14. Safe Operation Area



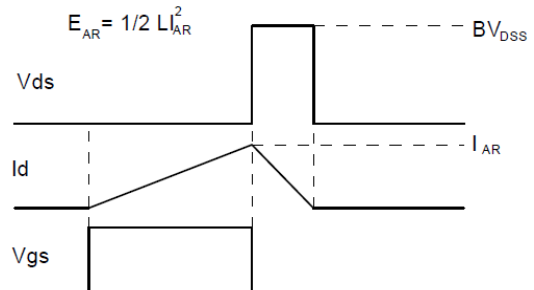
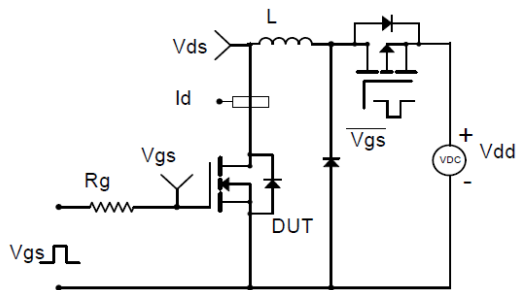
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

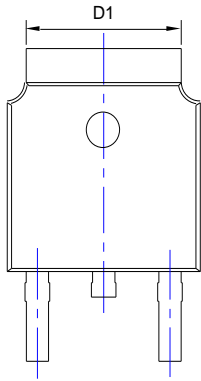


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

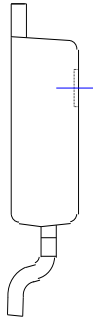


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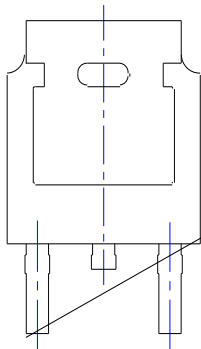
TO-252-B Package information



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES			
	MIN.	NOM.		
A1	0.000			
A2	0.087	0.091		
A3	0.035	0.039		
b	0.026	0.030		
c	0.018	0.020		
D	0.256	0.260		
D1				
D2	0.181	0.189		
E	0.390	0.398		
E1	0.236	0.240		

NOTE:

- 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



Disclaimer

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