



YJD50N03B

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	30V
I_D	50A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	9m
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	10m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Trench Power LV MOSFET technology
Extremely low switching loss
Excellent stability and uniformity
Moisture Sensitivity Level 1
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

Power management
Portable equipment

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 12	V
Drain Current	$T_A=25^{\circ}C$	I_D	11	A
	$T_A=100^{\circ}C$		7	
	$T_C=25^{\circ}C$		50	
	$T_C=100^{\circ}C$		31	
Pulsed Drain Current ^A		I_{DM}	120	A
Avalanche energy ^B		EAS	49	mJ
Total Power Dissipation ^C	$T_A=25^{\circ}C$	P_D	2.5	W
			1	
	$T_C=25^{\circ}C$		104	



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Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$ $V_{DS}=30V, V_{GS}=0V, T_J=150$	-	-	1	μA



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Typical Electrical and Thermal Characteristics Diagrams

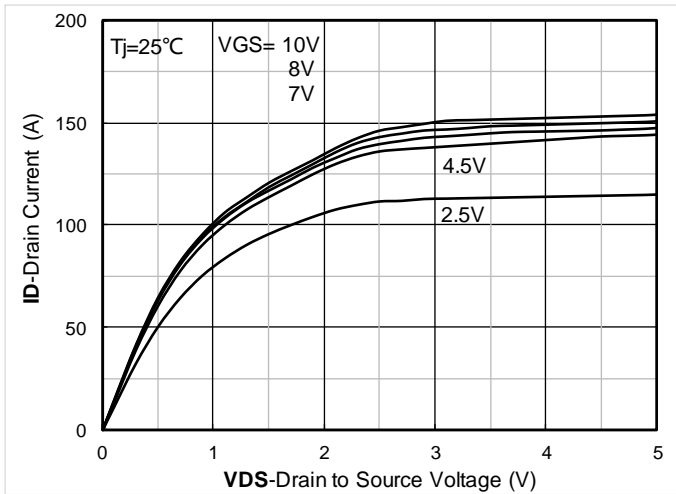


Figure 1. Output Characteristics

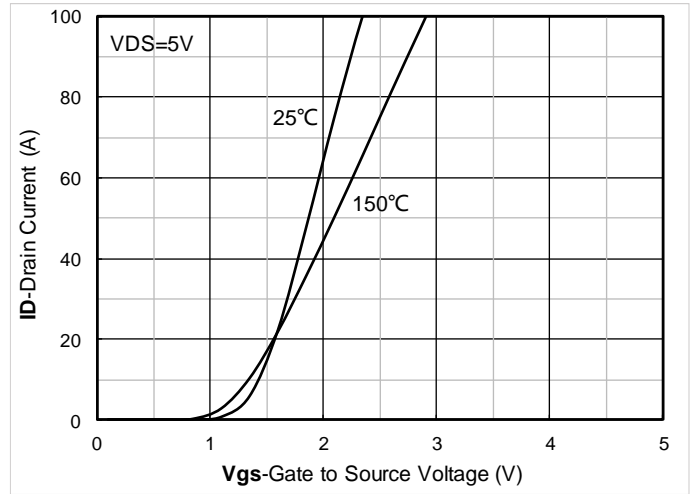


Figure 2. Transfer Characteristics

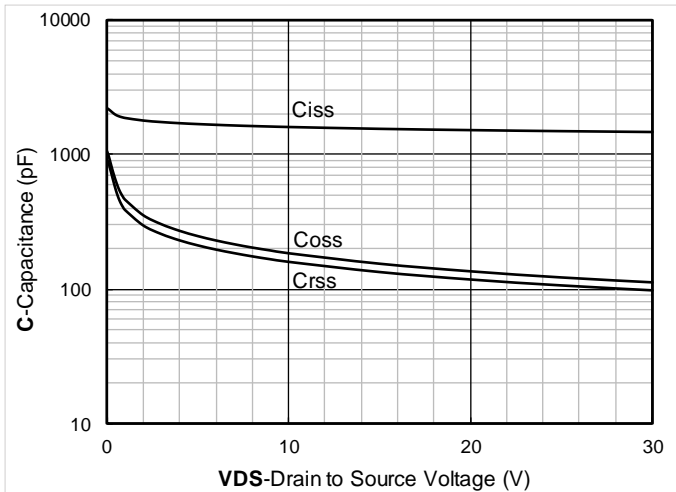


Figure 3. Capacitance Characteristics

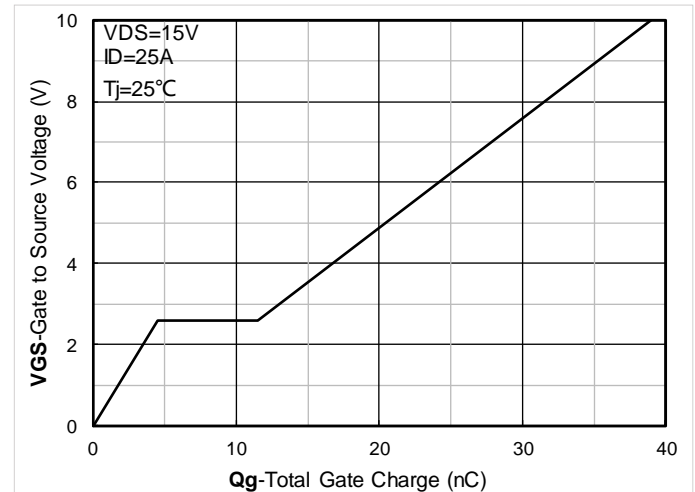


Figure 4. Gate Charge

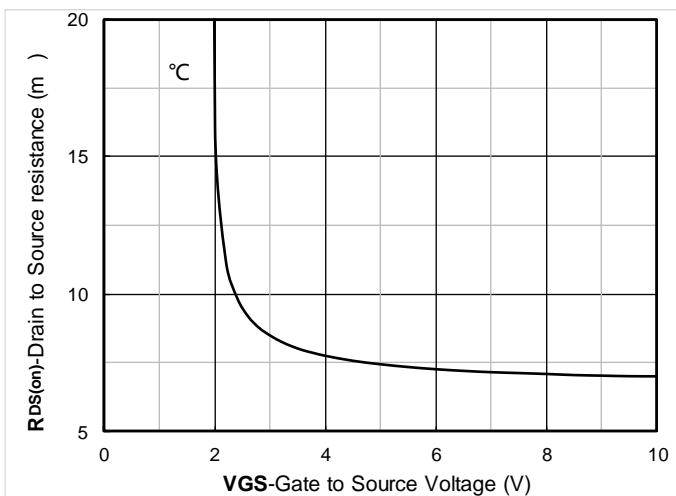


Figure 5. On-Resistance vs Gate to Source Voltage

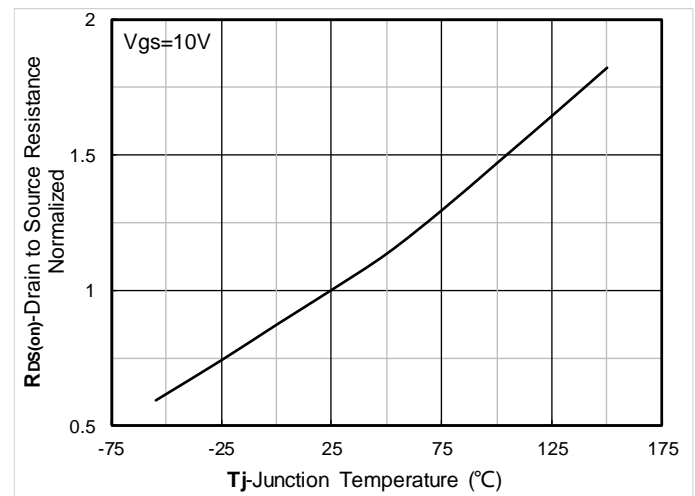


Figure 6. Normalized On-Resistance



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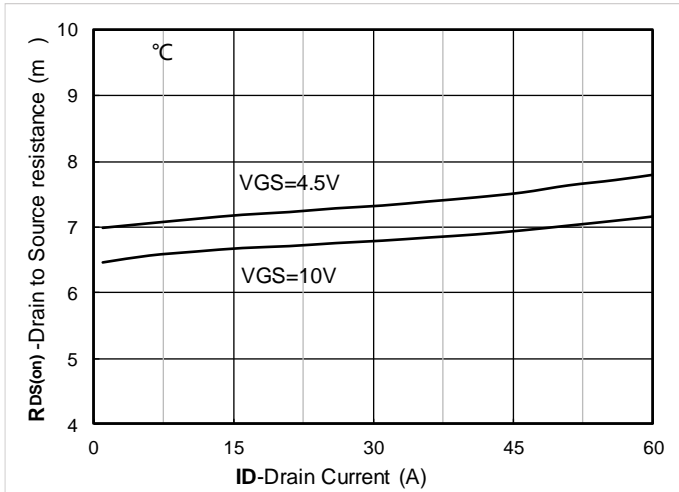


Figure 7. RDS(on) VS Drain Current

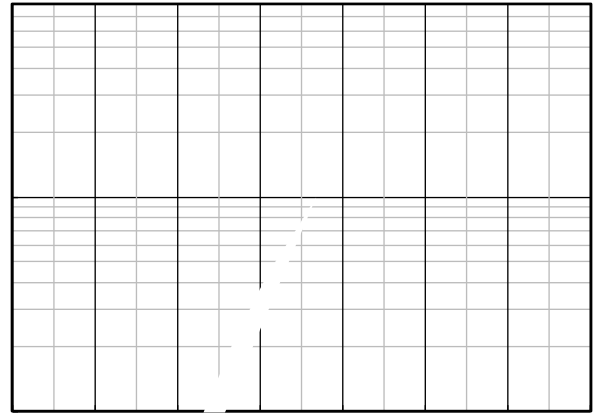


Figure 8. Forward characteristics of reverse diode

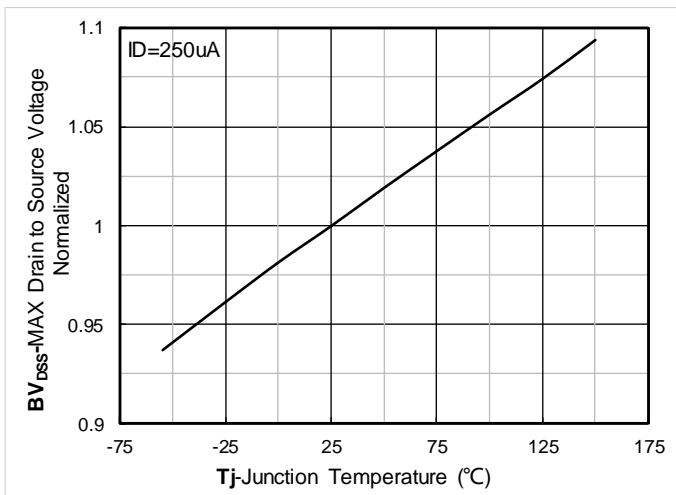


Figure 9. Normalized breakdown voltage

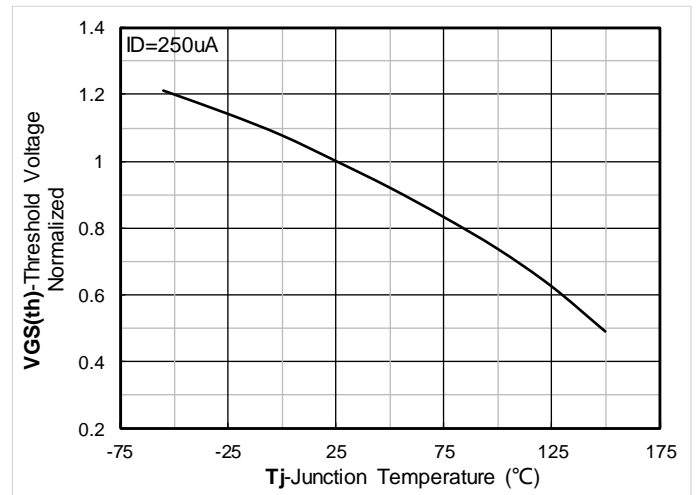


Figure 10. Normalized Threshold voltage

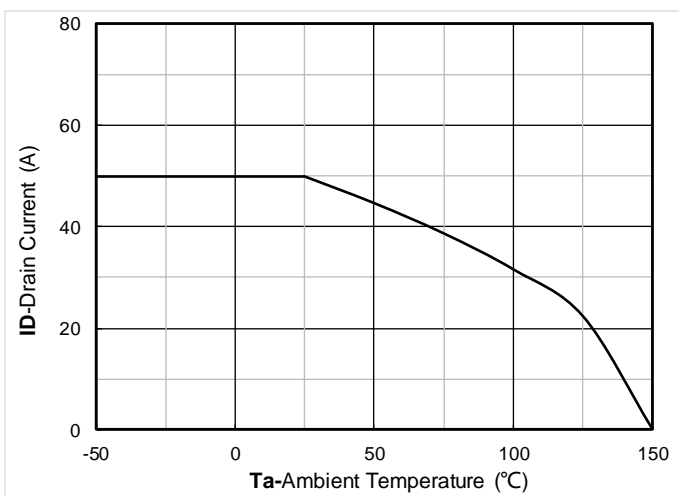


Figure 11. Current dissipation

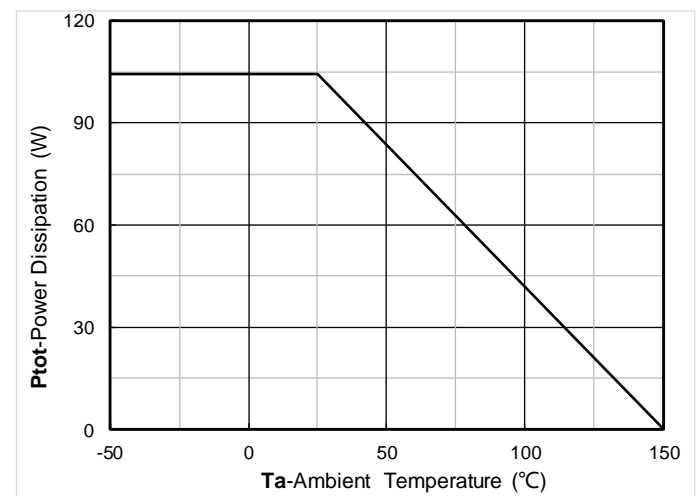


Figure 12. Power dissipation

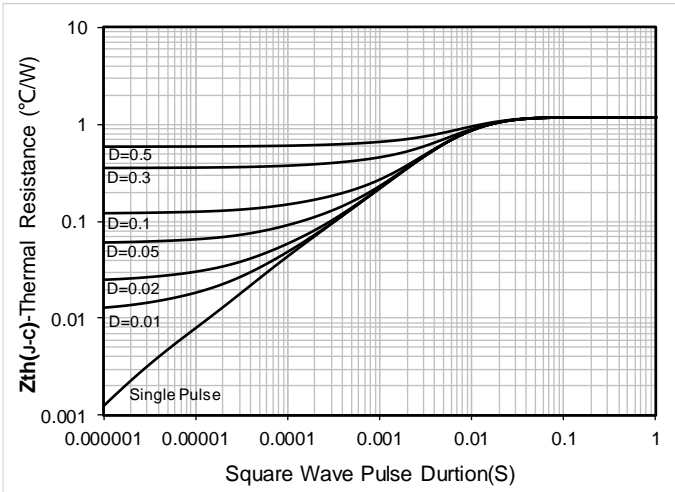


Figure 13. Maximum Transient Thermal Impedance

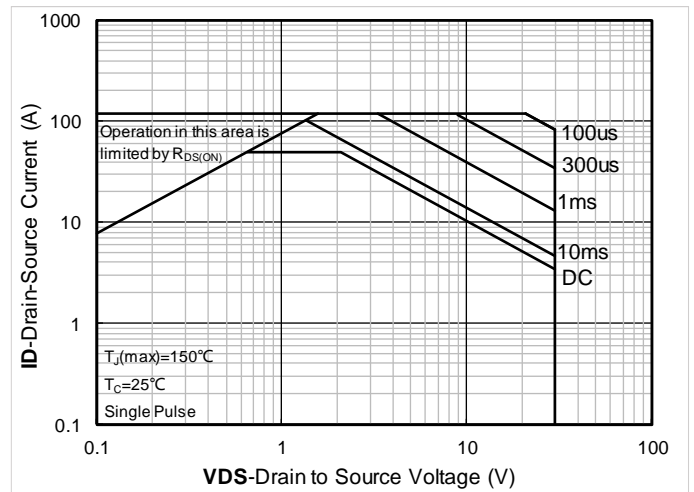


Figure 14. Safe Operation Area

Test Circuits & Waveforms

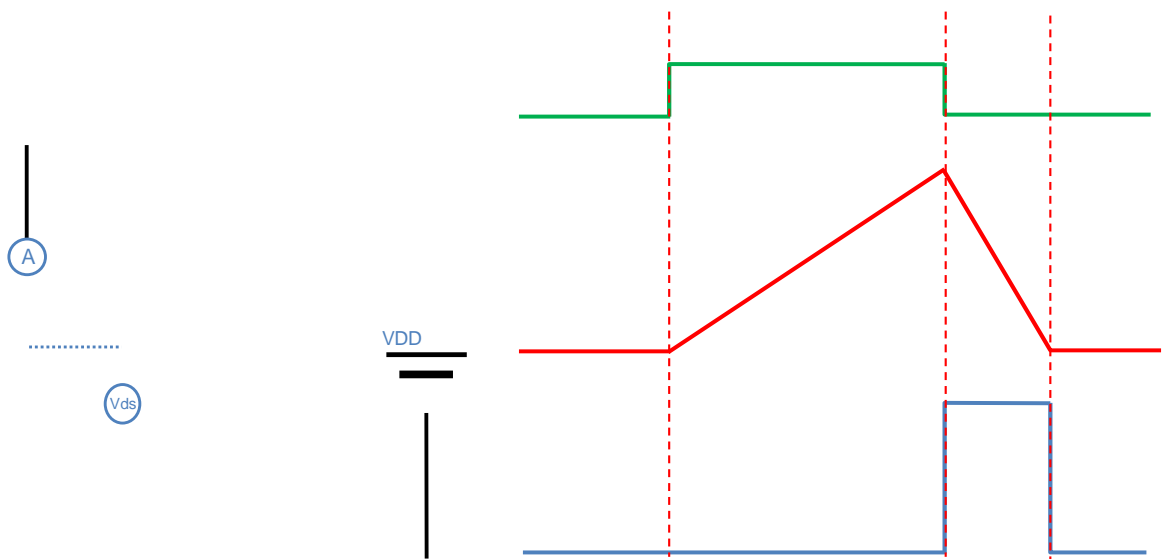


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

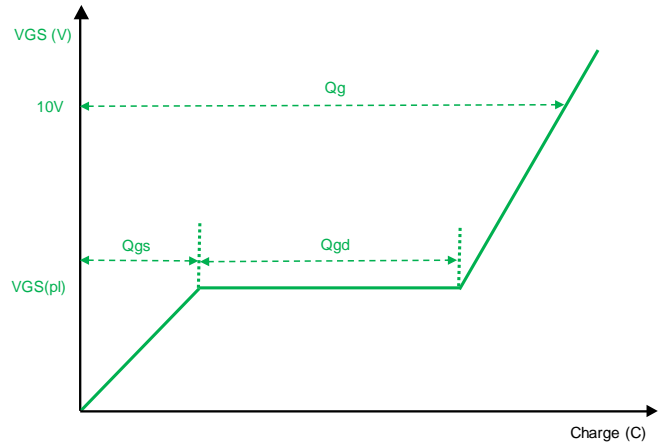
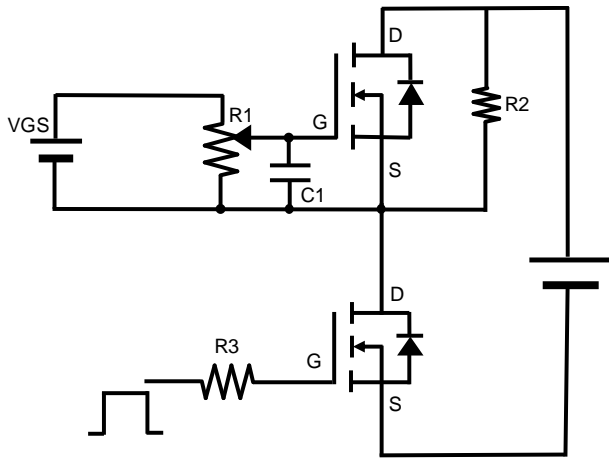


Figure B. Gate Charge Test Circuit & Waveform

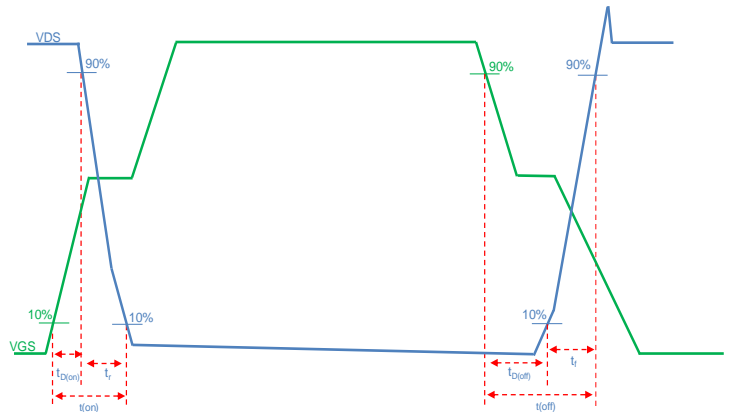
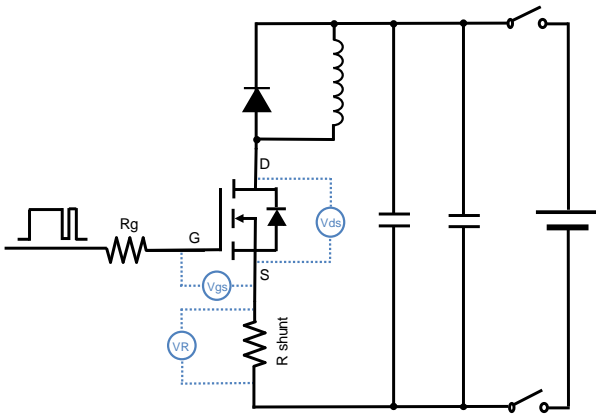


Figure C. Resistive Switching Test Circuit & Waveform

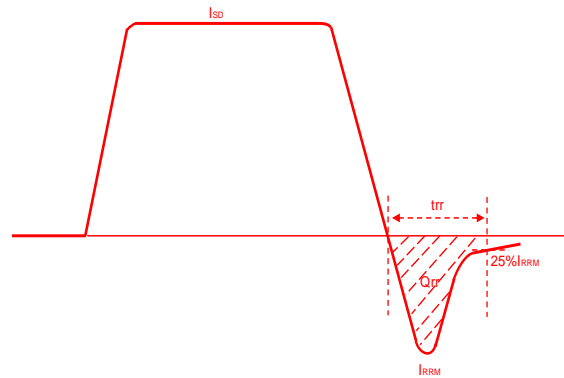
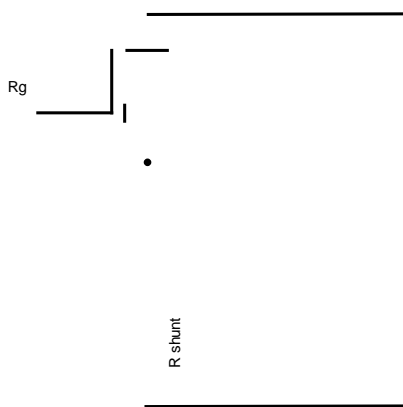
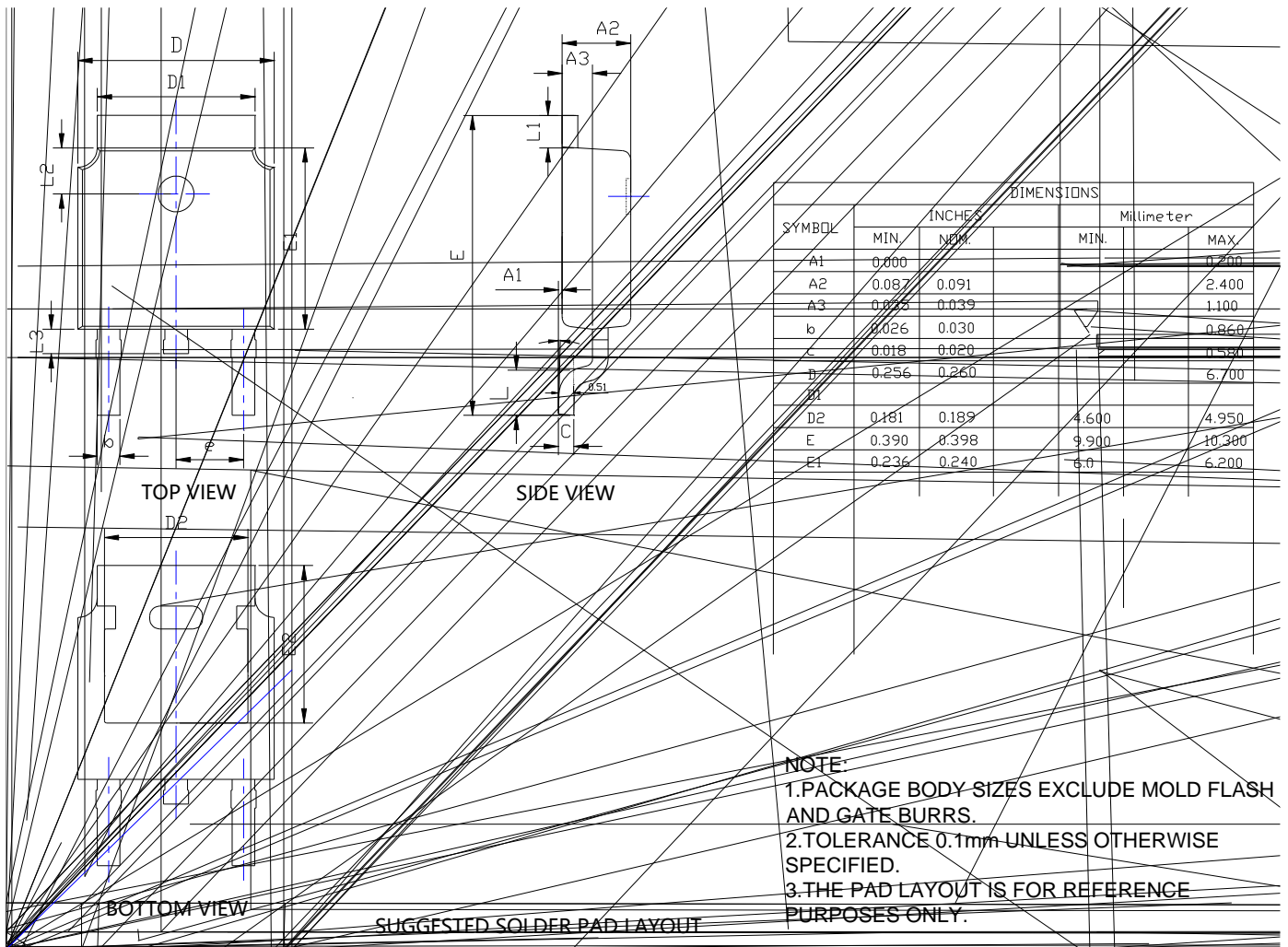


Figure D. Diode Recovery Test Circuit & Waveform



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TO-252-B Package information





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