



YJD80N03A

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

| | |
|----------------------------------|---------|
| V_{DS} | 30V |
| I_D | 80A |
| $R_{DS(ON)}$ (at $V_{GS}=10V$) | 4.5mohm |
| $R_{DS(ON)}$ (at $V_{GS}=4.5V$) | 6.0mohm |
| 100% EAS Tested | |
| ∇V_{DS} Tested | |

General Description

Excellent package for heat dissipation
 High density cell design for low $R_{DS(ON)}$
 Moisture Sensitivity Level 1
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

High current load applications
 Load switching
 Hard switched and high frequency circuits
 Uninterruptible power supply

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

| Parameter | | Symbol | Limit | Unit |
|--|-----------|----------------|----------|------|
| Drain-source Voltage | | V_{DS} | 30 | V |
| Gate-source Voltage | | V_{GS} | 20 | V |
| Drain Current | $T_C=25$ | I_D | 80 | A |
| | $T_C=100$ | | 50 | |
| Pulsed Drain Current ^A | | I_{DM} | 190 | A |
| Total Power Dissipation | $T_C=25$ | P_D | 44 | W |
| | $T_C=100$ | | 17 | W |
| Single Pulse Avalanche Energy ^B | | E_{AS} | 132 | mJ |
| Thermal Resistance Junction-to-Case ^C | | R_{JC} | 2.8 | /W |
| Junction and Storage Temperature Range | | T_J, T_{STG} | -55 +150 | |

Ordering Information (Example)

| PREFERRED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---------------|--------------|---------|----------------------|-------------------------|----------------------------|---------------|
|---------------|--------------|---------|----------------------|-------------------------|----------------------------|---------------|

YJD80N03A

F1/F2



YJD80N03A

Electrical Characteristics ($T_J=25$ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------------|--------------|--|-----|-----|-----|-------|
| Static Parameter | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS}=0V, I_D=250$ | 30 | | | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS}=30V, V_{GS}=0V$ | | | 1 | |
| | | $V_{DS}=30V, V_{GS}=0V, T_J=150^\circ C$ | | | 100 | |
| Gate-Body Leakage Current | I_{GSS} | $V_{GS}=20V, V_{DS}=0V$ | | | 100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=250$ | 1.0 | 1.5 | 2.5 | V |

Static Drain-Source On-Resistance

$R_{DS(on)}$

$V_{GS}=\dots$



Typical Performance Characteristics

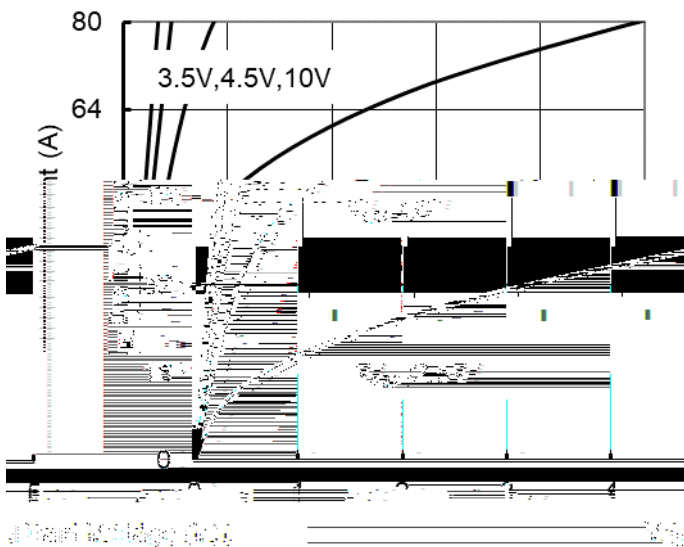


Figure 1. Output Characteristics

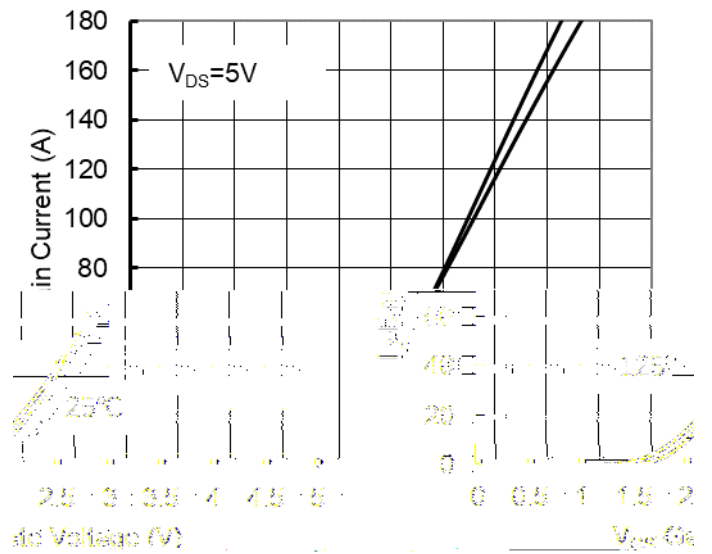


Figure 2. Transfer Characteristics

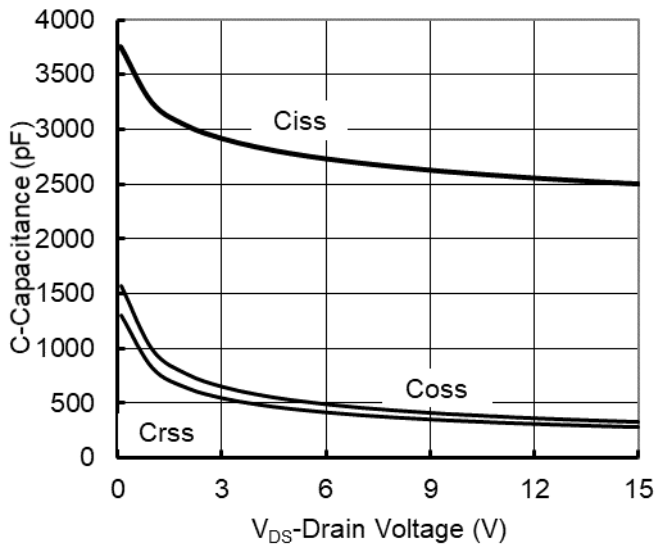


Figure 3. Capacitance Characteristics

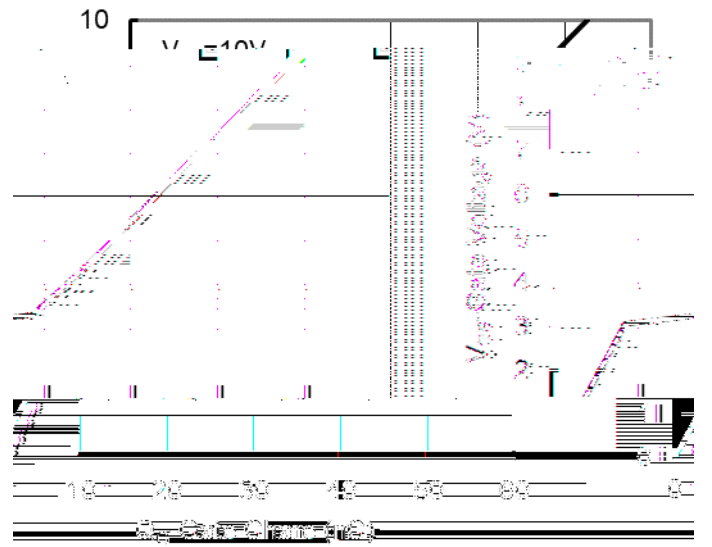
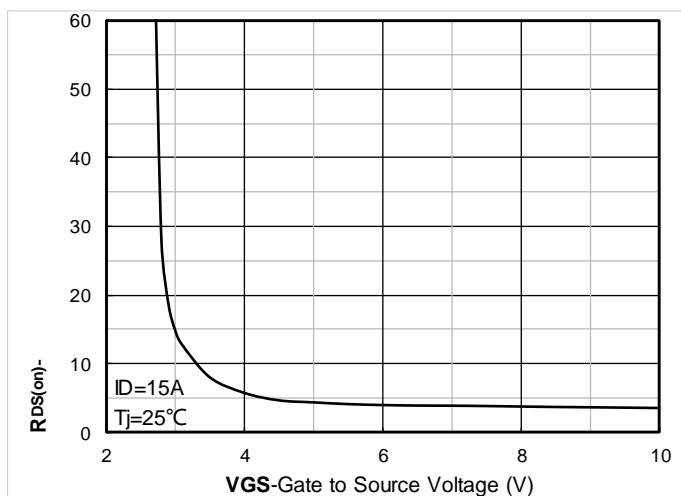


Figure 4. Gate Charge





YJD80N03A

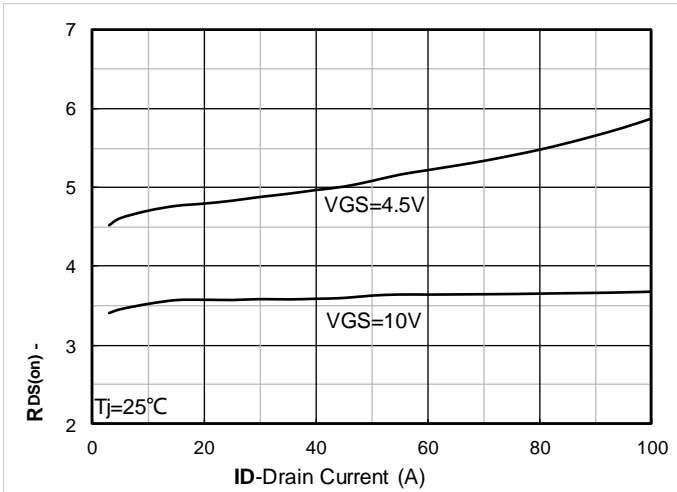


Figure 7. RDS(on) VS Drain Current

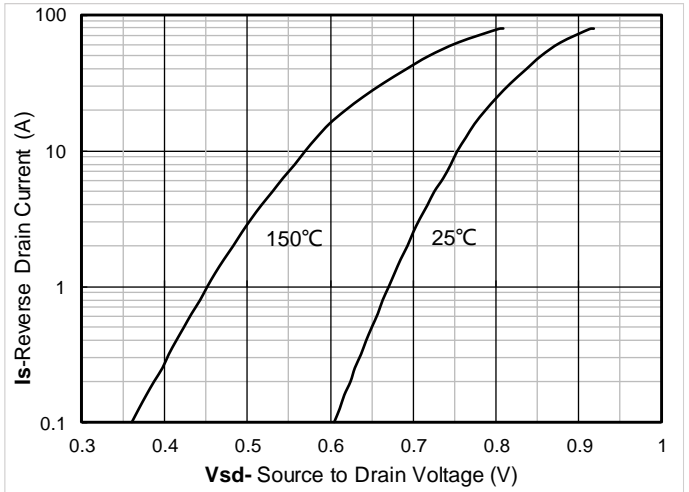


Figure 8. Forward characteristics of reverse diode

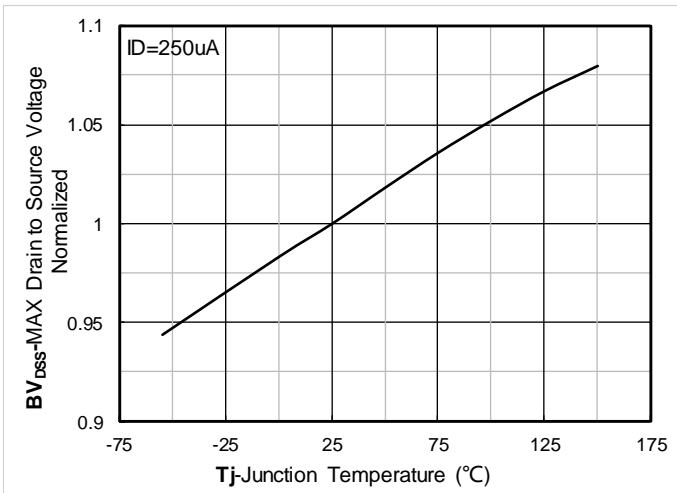


Figure 9. Normalized breakdown voltage

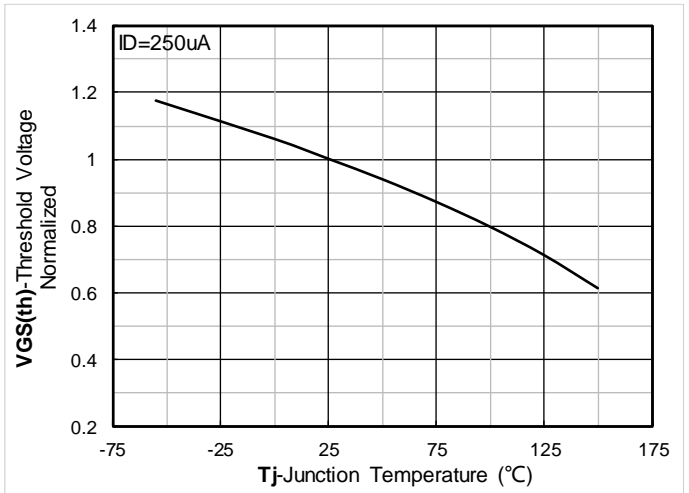


Figure 10. Normalized Threshold voltage

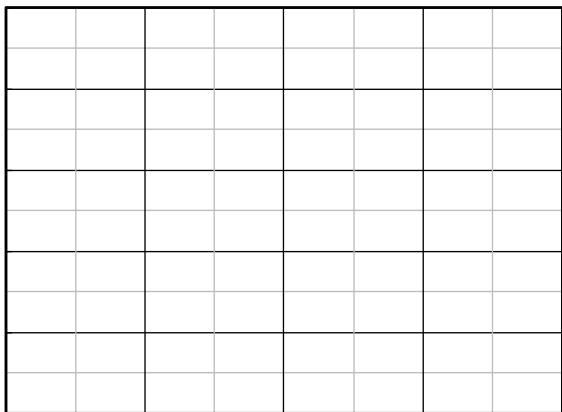


Figure 11. Current dissipation

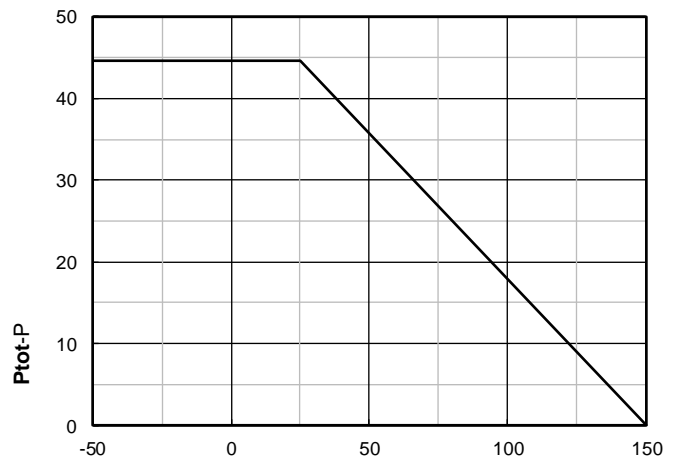


Figure 12. Power dissipation

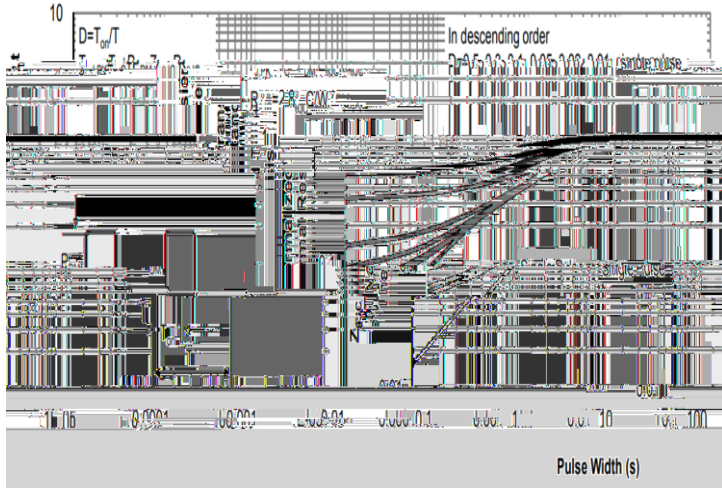


Figure 13. Normalized Maximum Transient Thermal Impedance

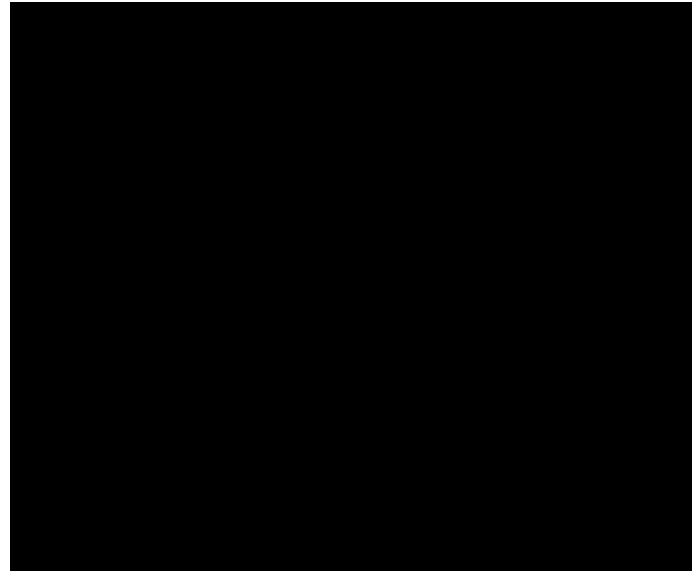
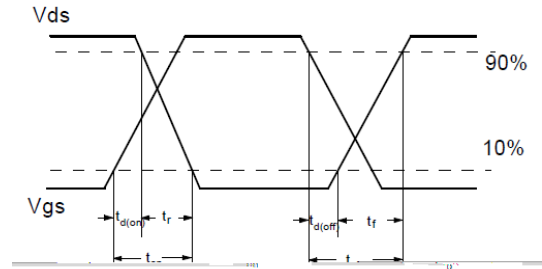
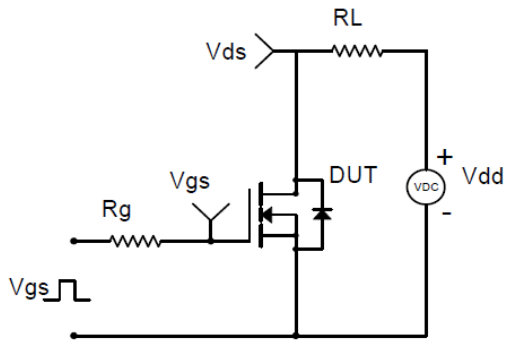
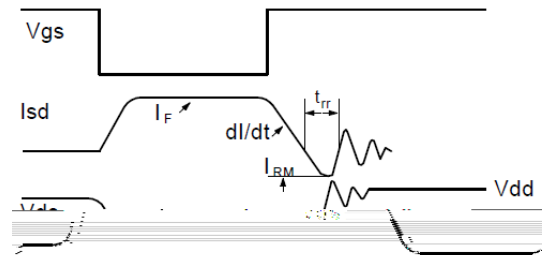
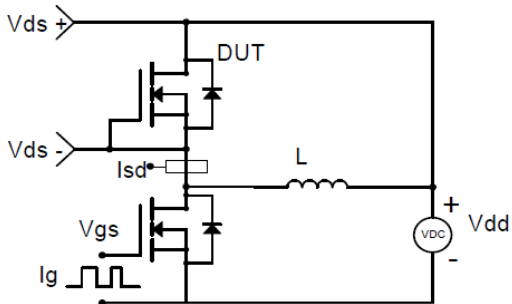


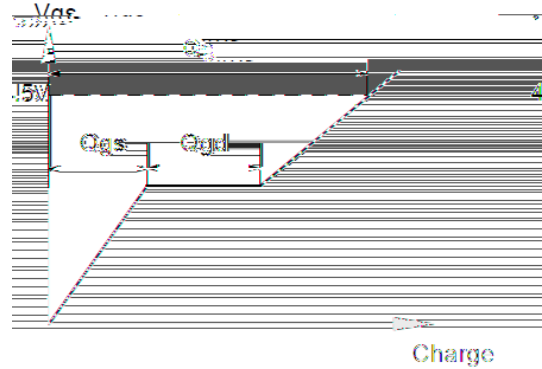
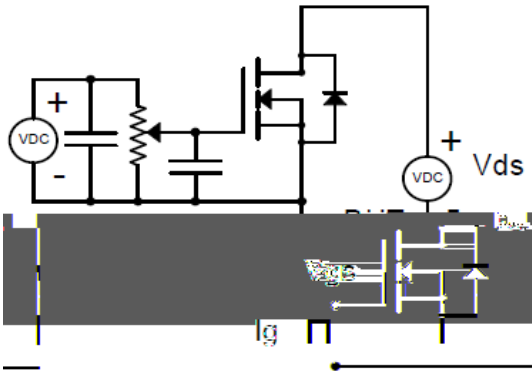
Figure 14. Safe Operation Area



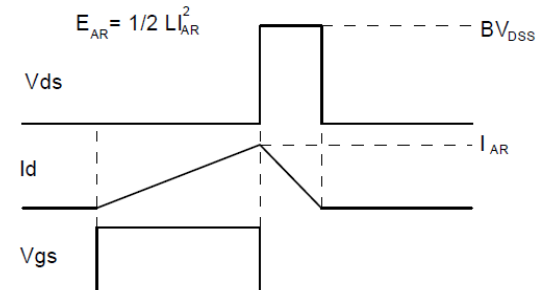
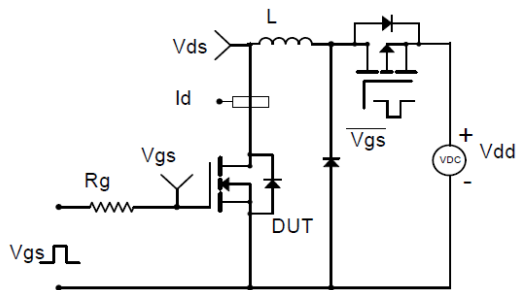
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

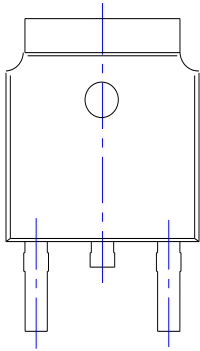


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



YJD80N03A

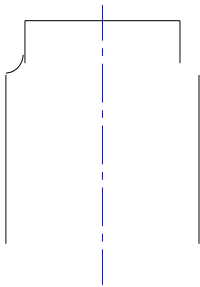
TO-252-B Package information



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SUGGESTED SOLDER PAD LAYOUT

| SYMBOL | DIMENSIONS | | | |
|--------|------------|-------|--|--|
| | INCHES | | | |
| | MIN. | NOM. | | |
| A1 | 0.000 | | | |
| A2 | 0.087 | 0.091 | | |
| A3 | 0.035 | 0.039 | | |
| b | 0.026 | 0.030 | | |
| c | 0.018 | 0.020 | | |
| D | 0.256 | 0.260 | | |
| D1 | | | | |
| D2 | 0.181 | 0.189 | | |
| E | 0.390 | 0.398 | | |
| E1 | 0.236 | 0.240 | | |

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



YJD80N03A

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