



# YJD90G06A

## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	60V
$I_D$	90A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	4.8m
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	7.2m
100% EAS Tested	
100% $V_{DS}$ Tested	

### General Description

Split gate trench MOSFET technology  
 Excellent package for heat dissipation  
 High density cell design for low  $R_{DS(ON)}$   
 Moisture Sensitivity Level 1  
 Epoxy Meets UL 94 V-0 Flammability Rating  
 Halogen Free

### Applications

Power switching application  
 Uninterruptible power supply  
 DC-DC convertor

### Absolute Maximum Ratings ( $T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	60	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ C$	$I_D$	15	A
	$T_A=100^\circ C$		10	
	$T_C=25^\circ C$		90	
	$T_C=100^\circ C$		63	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	360	A
Avalanche energy <sup>B</sup>		EAS	144	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ C$	$P_D$	3.7	W
	$T_A=100^\circ C$		1.8	
	$T_C=25^\circ C$		115	
	$T_C=100^\circ C$		57	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 +175	$^\circ C$

### Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State	R	30	40	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	R	1.1	1.3	

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
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## Typical Electrical and Thermal Characteristics Diagrams

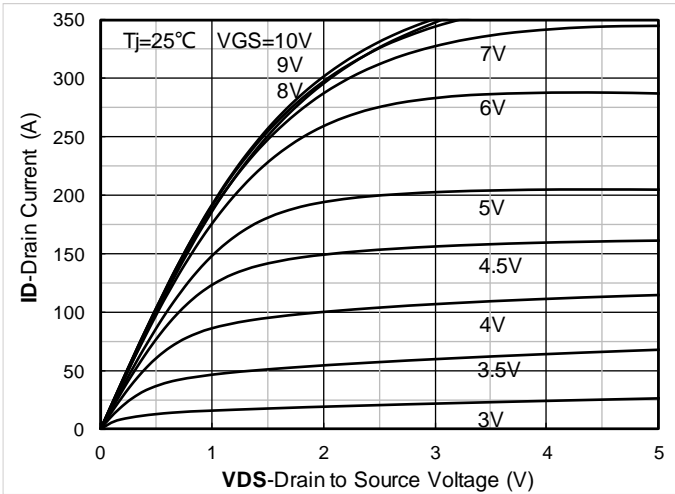


Figure 1. Output Characteristics

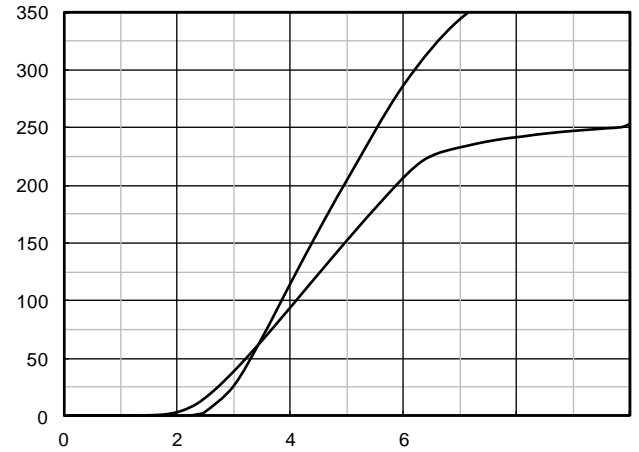


Figure 2. Transfer Characteristics

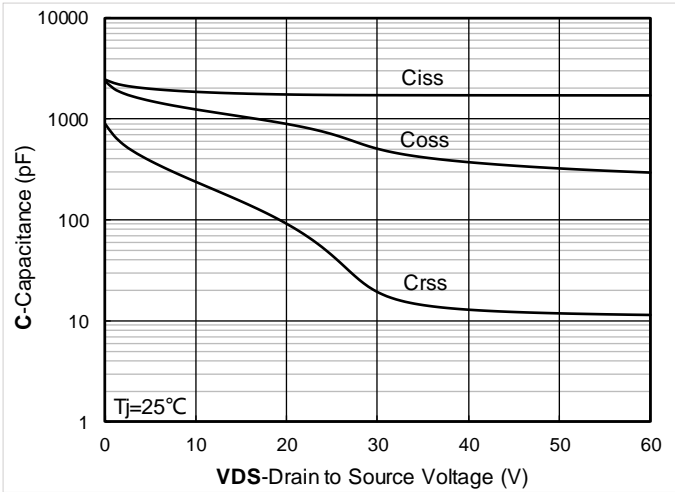


Figure 3. Capacitance Characteristics

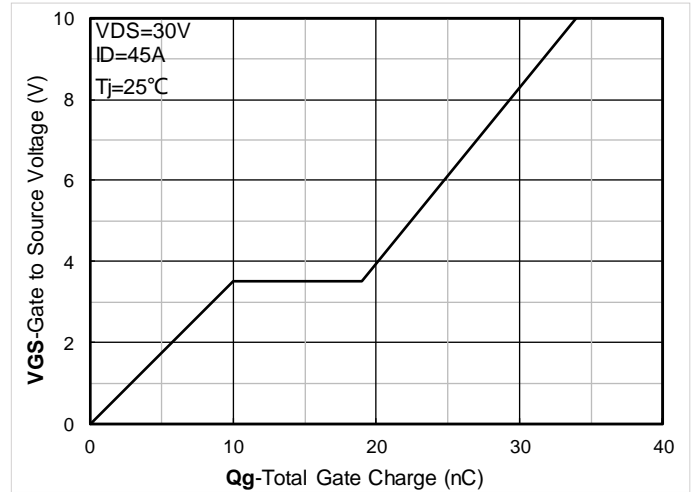


Figure 4. Gate Charge

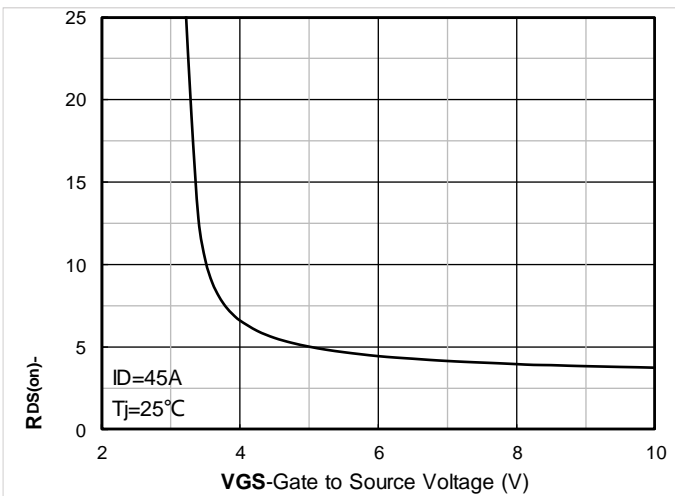


Figure 5. On-Resistance vs Gate to Source Voltage

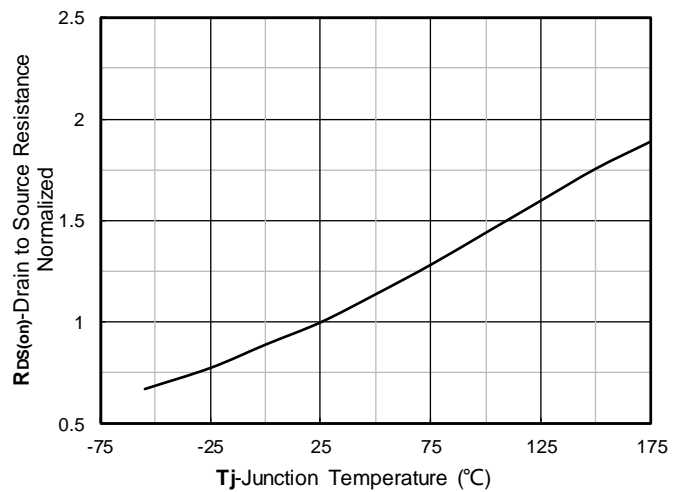


Figure 6. Normalized On-Resistance



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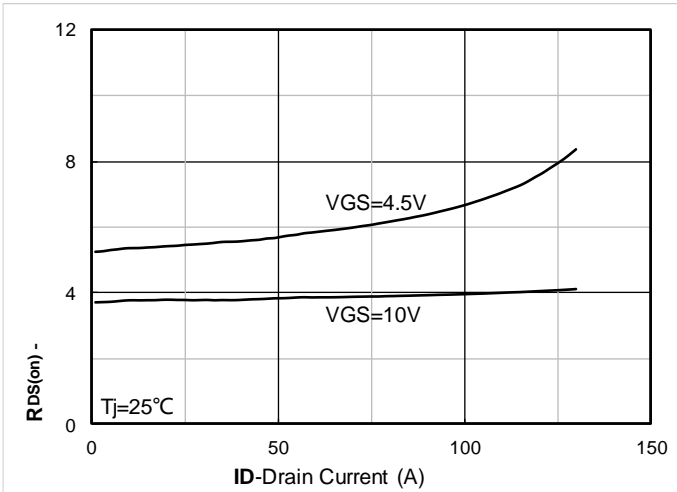


Figure 7. RDS(on) VS Drain Current

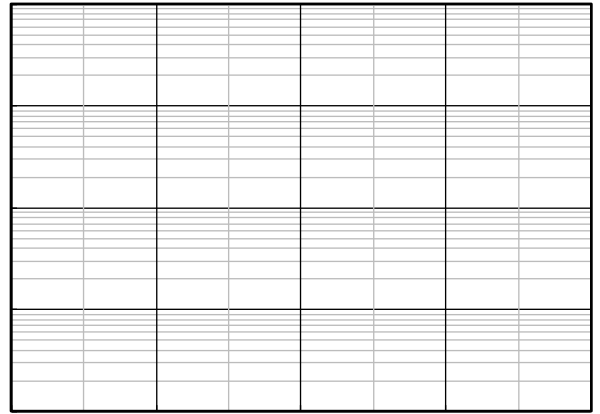


Figure 8. Forward characteristics of reverse diode

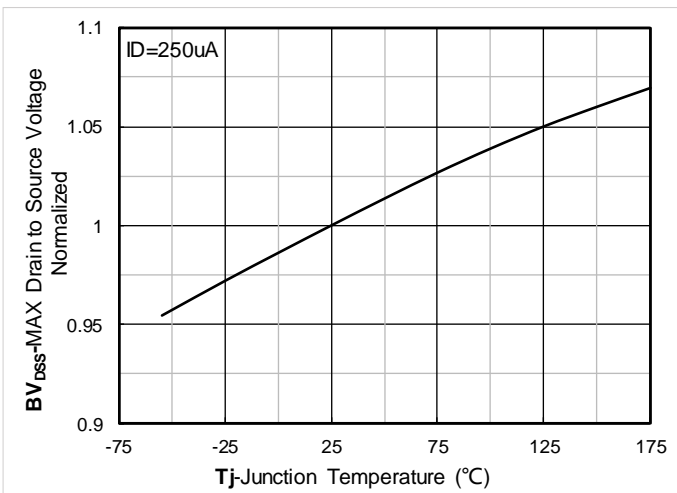


Figure 9. Normalized breakdown voltage

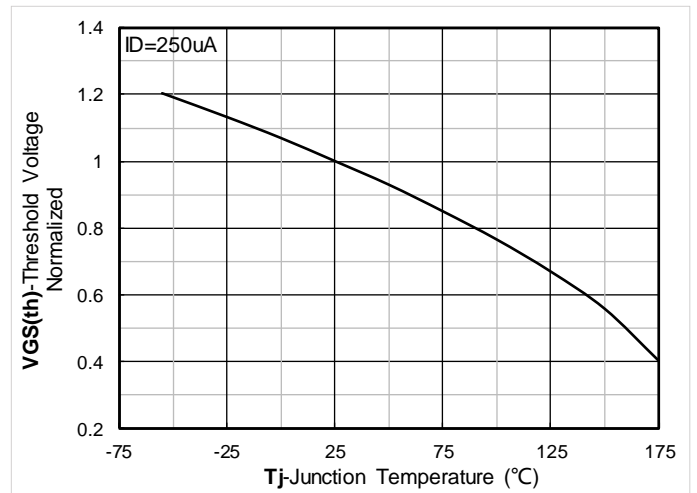


Figure 10. Normalized Threshold voltage

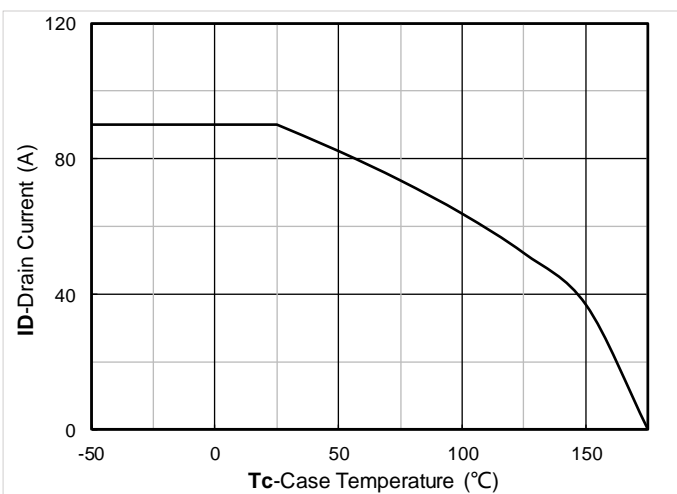


Figure 11. Current dissipation

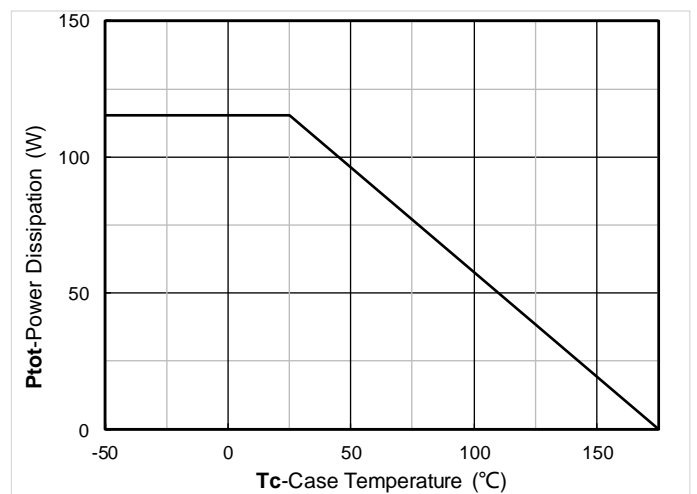


Figure 12. Power dissipation

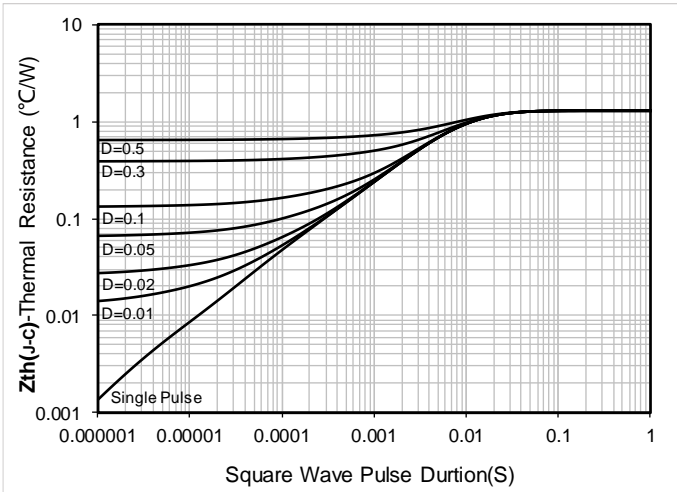


Figure 13. Maximum Transient Thermal Impedance

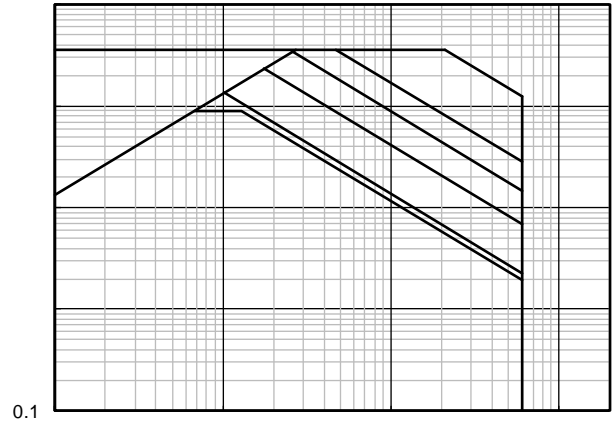


Figure 14. Safe Operation Area

## Test Circuits & Waveforms

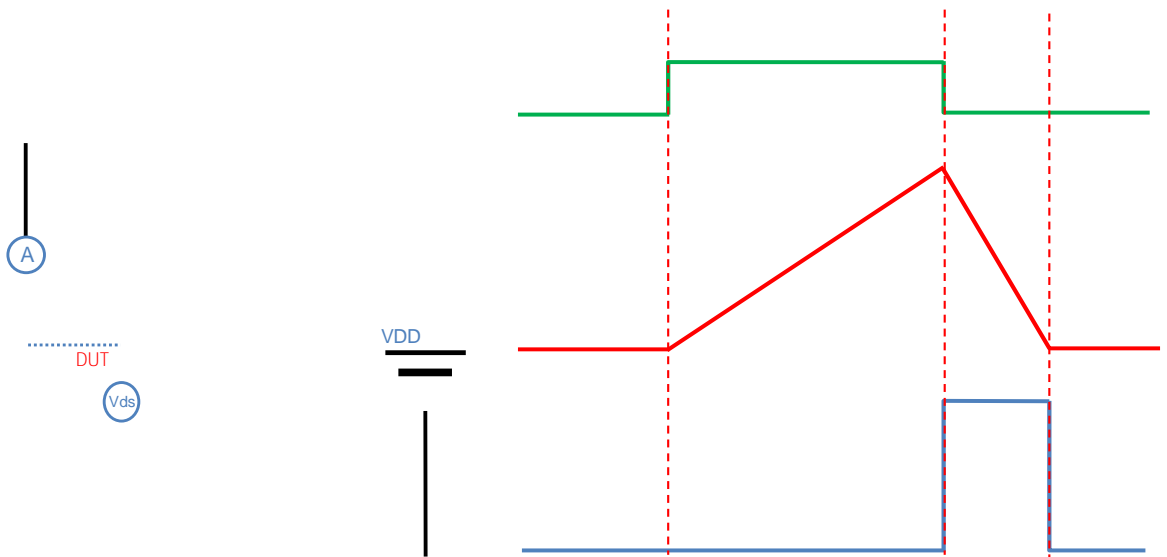


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

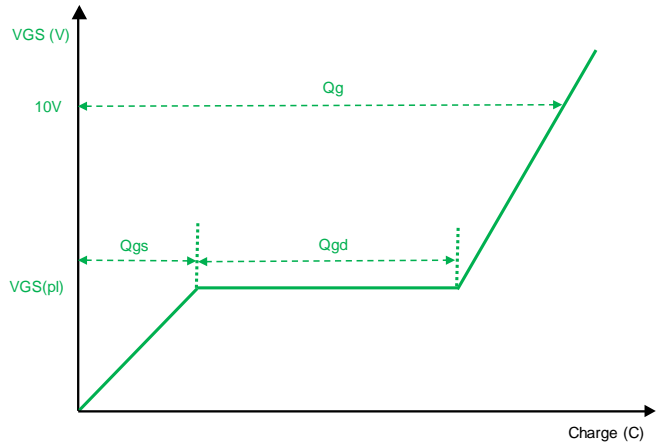
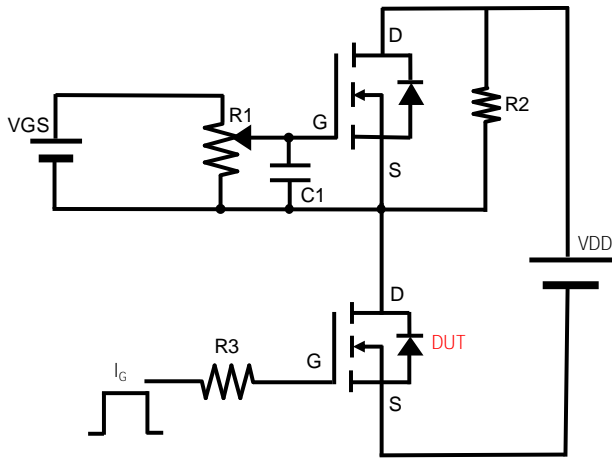


Figure B. Gate Charge Test Circuit & Waveform

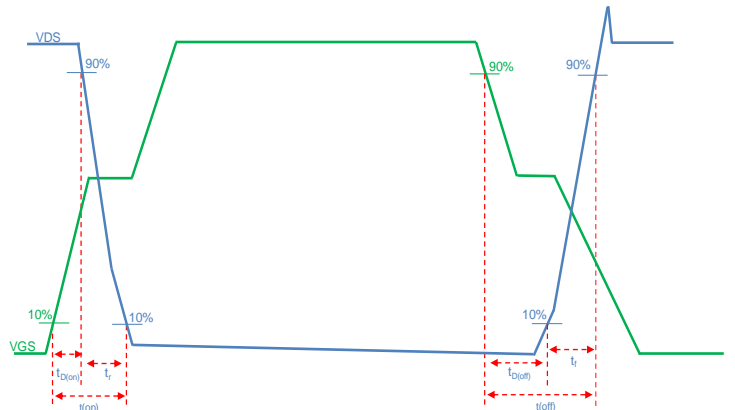
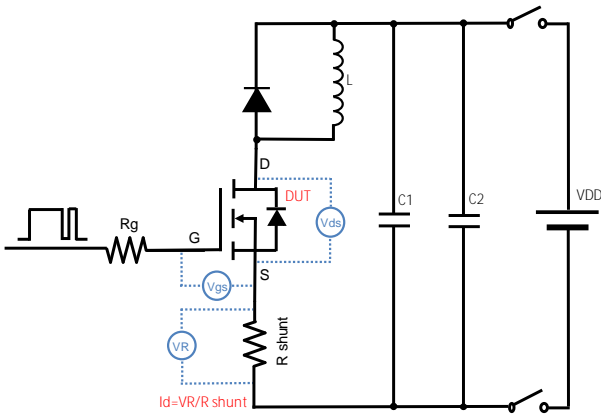


Figure C. Resistive Switching Test Circuit & Waveform

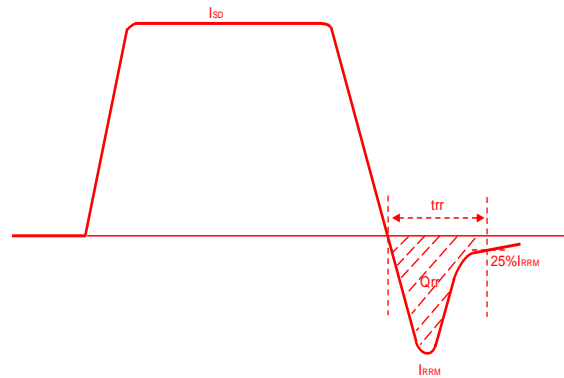
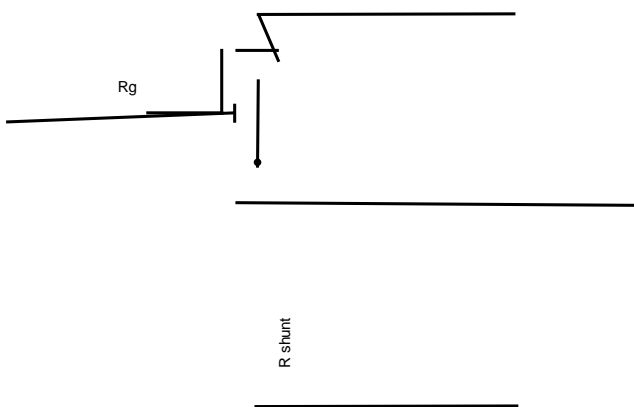
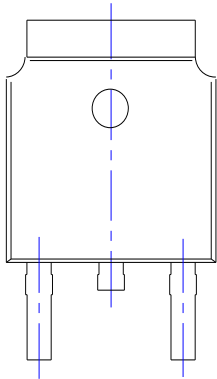


Figure D. Diode Recovery Test Circuit & Waveform



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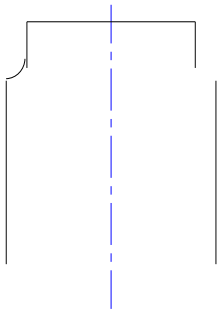
## TO-252-B Package information



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS				
	INCHES				
	MIN.	NOM.			
A1	0.000				
A2	0.087	0.091			
A3	0.035	0.039			
b	0.026	0.030			
c	0.018	0.020			
D	0.256	0.260			
D1					
D2	0.181	0.189			
E	0.390	0.398			
E1	0.236	0.240			

**NOTE:**

- 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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## Disclaimer

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