



YJF70G10A

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	100V
I_D	70A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	5.5m
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	6.5m
100% EAS Tested	
100% V_{DS} Tested	

General Description

gate trench MOSFET technology
 $R_{DS(on)}$ & FOM
 Excellent stability and uniformity
 -0 Flammability Rating
 Free

Applications

agement

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Units
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25$	I_D	15	A
	$T_A=100$		9.5	
	$T_C=25$		70	
	$T_C=100$		44	
Pulsed Drain Current ^A		I_{DM}	300	A
Avalanche energy ^B		EAS	306	mJ
Total Power Dissipation ^C	$T_A=25$	P_D	2.5	W
	$T_A=100$		1	
	$T_C=25$		62	
	$T_C=100$		25	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	R	40	50	/W
Thermal Resistance Junction-to-Case	Steady-State	R	1.6	2	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJF70G10A	B1	YJF70G10A	50	/	5000	

YJF70G10A



Typical Electrical and Thermal Characteristics Diagrams

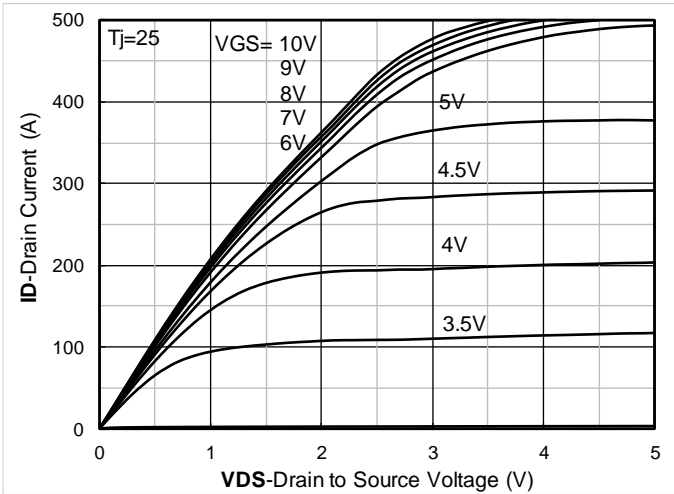


Figure 1. Output Characteristics

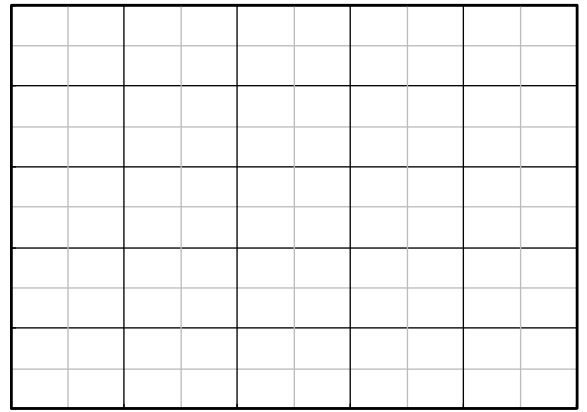


Figure 2. Transfer Characteristics

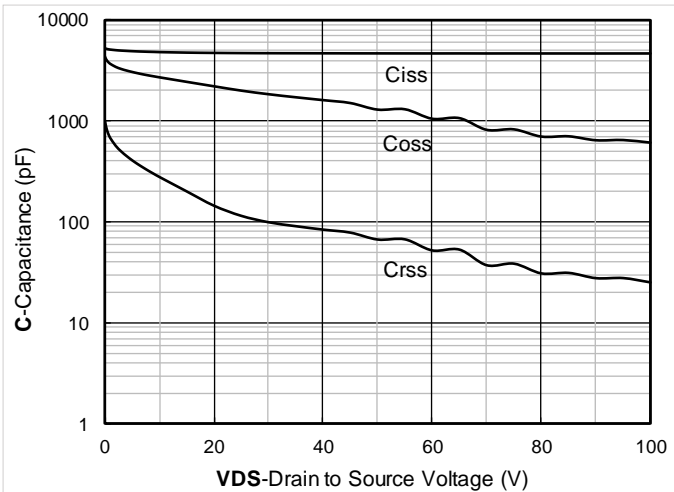


Figure 3. Capacitance Characteristics

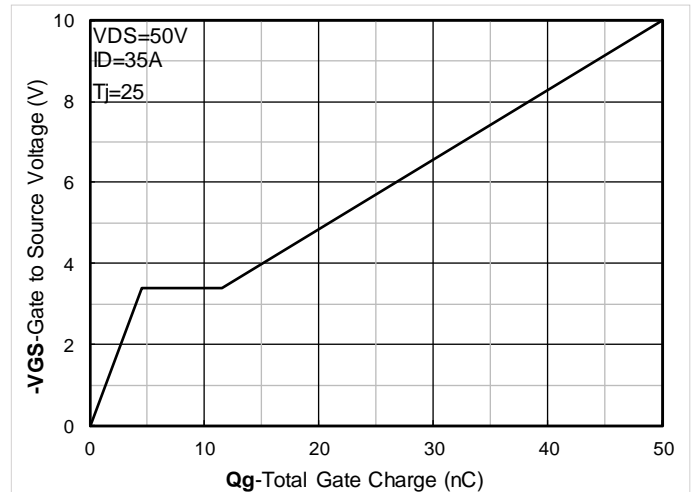


Figure 4. Gate Charge

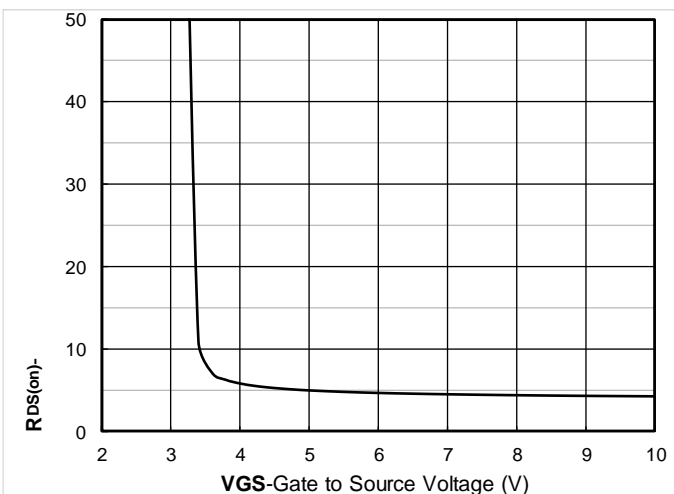


Figure 5. On-Resistance vs Gate to Source Voltage

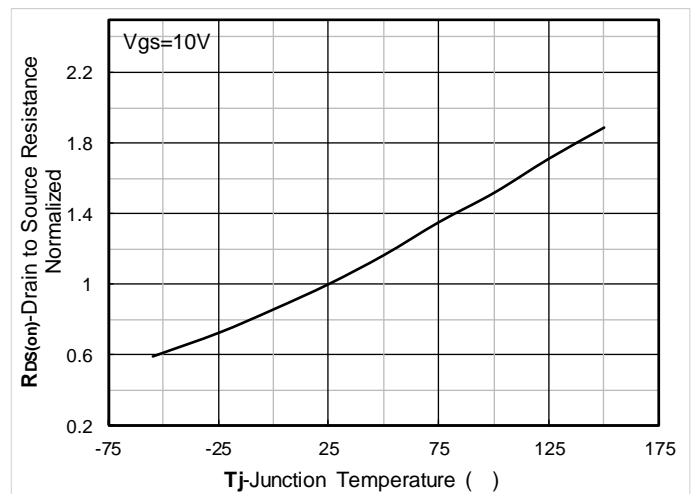


Figure 6. Normalized On-Resistance



YJF70G10A

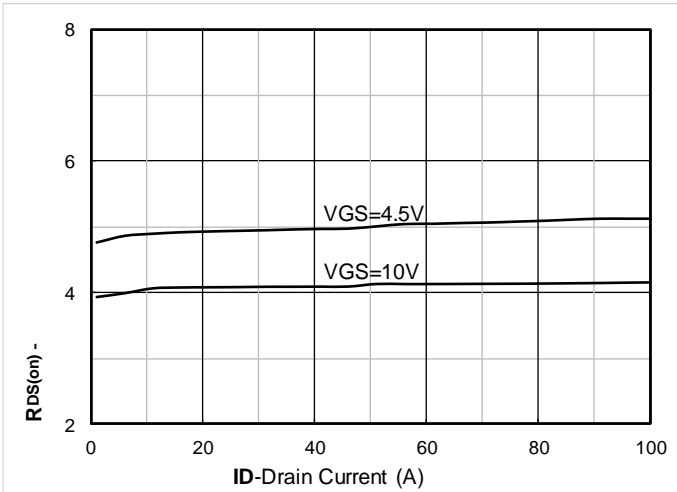


Figure 7. RDS(on) VS Drain Current

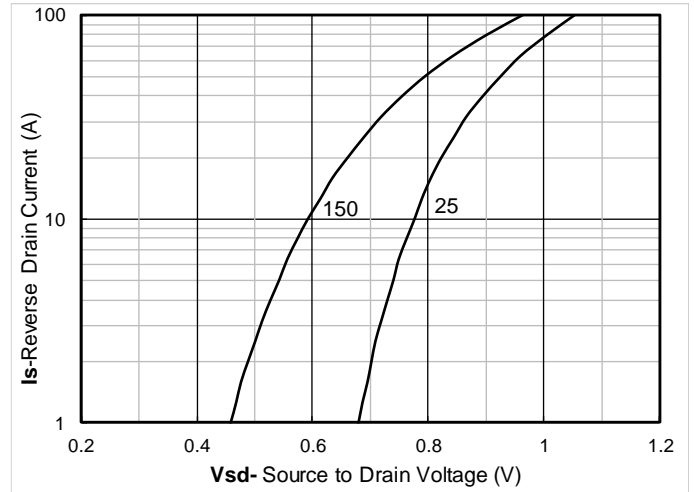


Figure 8. Forward characteristics of reverse diode

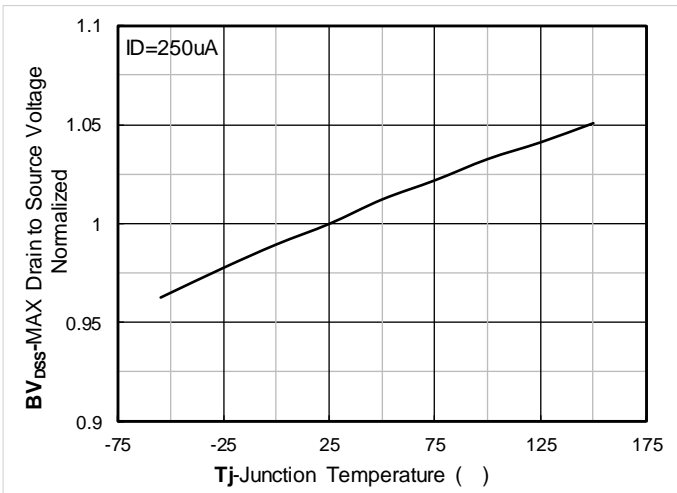


Figure 9. Normalized breakdown voltage

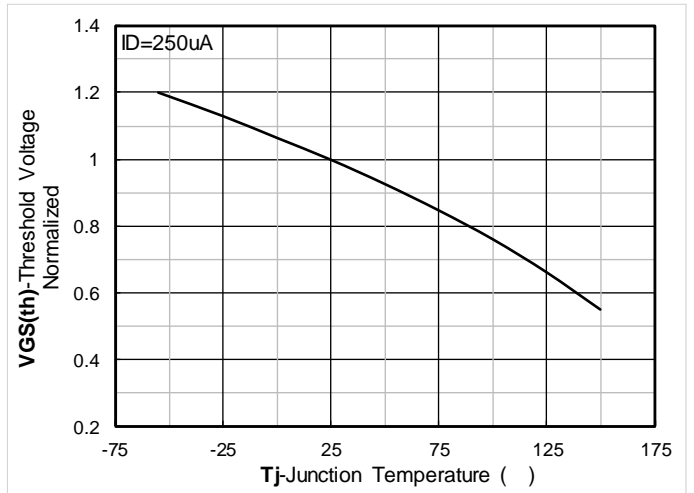


Figure 10. Normalized Threshold voltage

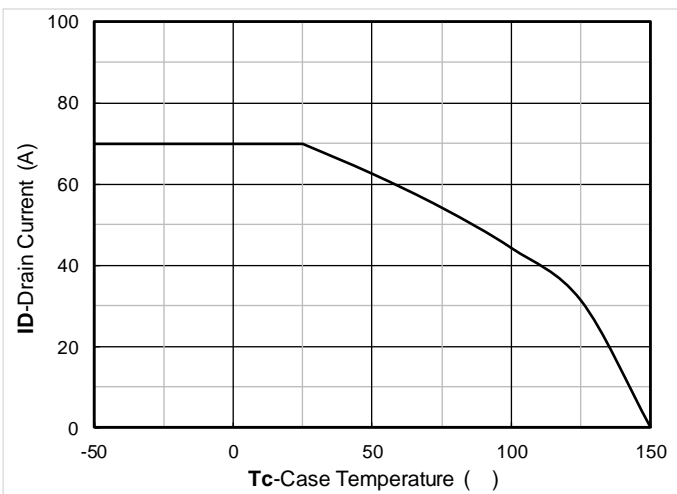


Figure 11. Current dissipation

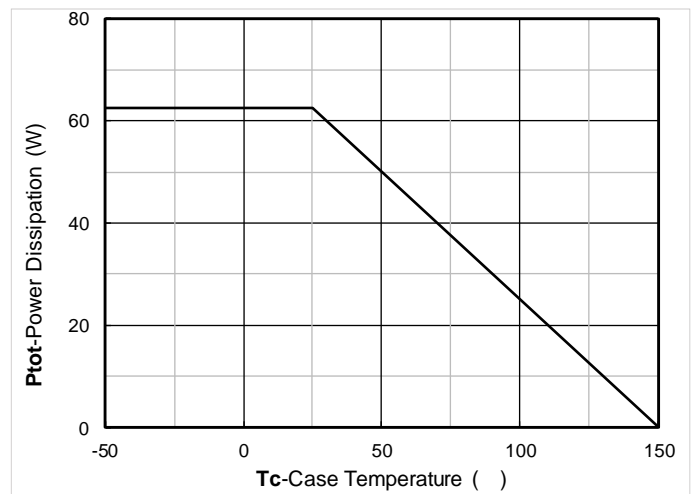


Figure 12. Power dissipation

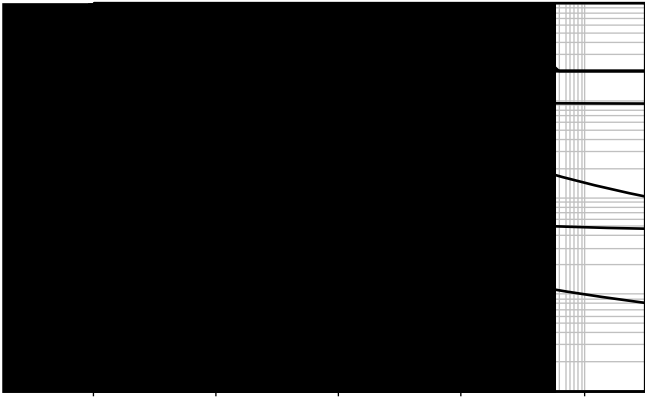


Figure 13. Maximum Transient Thermal Impedance

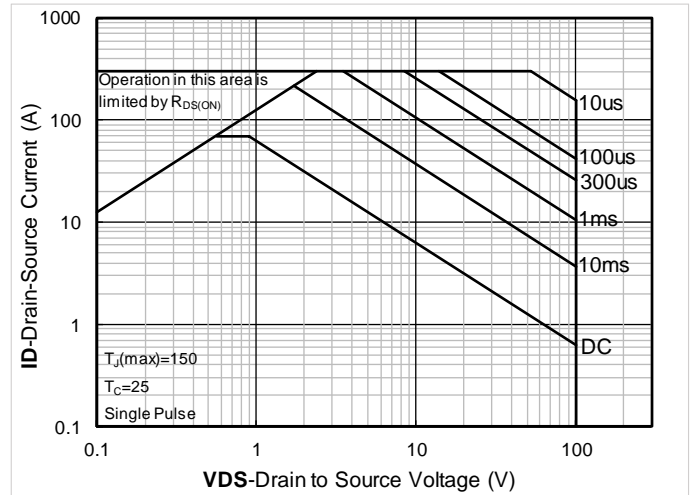


Figure 14. Safe Operation Area

Test Circuits & Waveforms

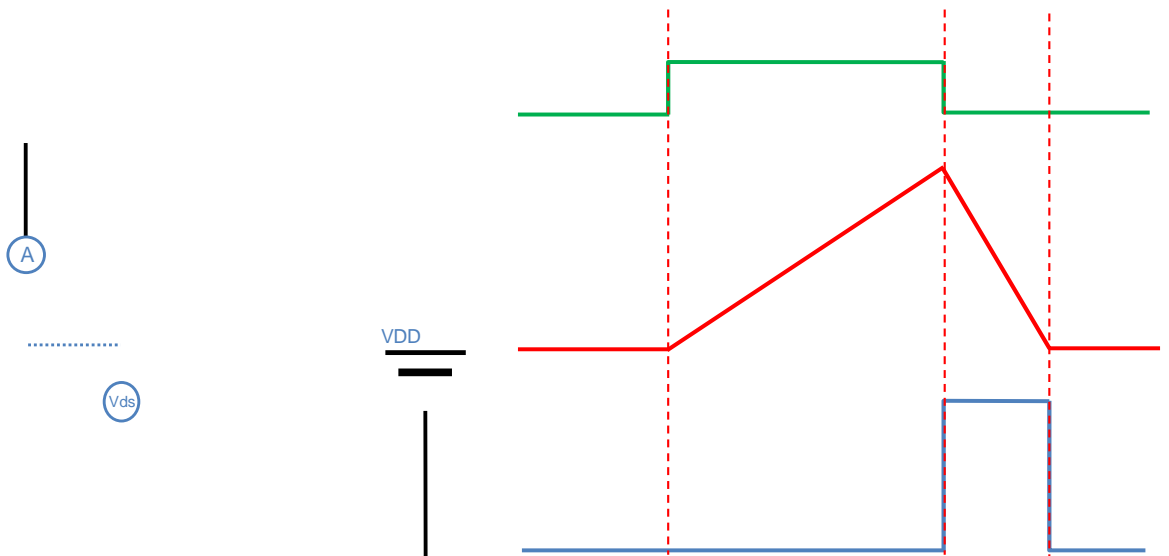


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

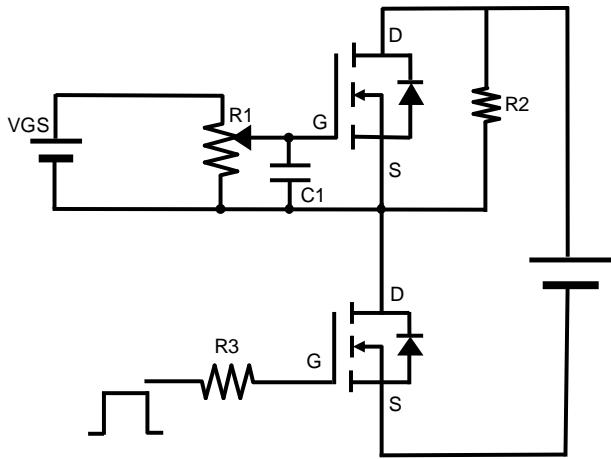


Figure B. Gate Charge Test Circuit & Waveform

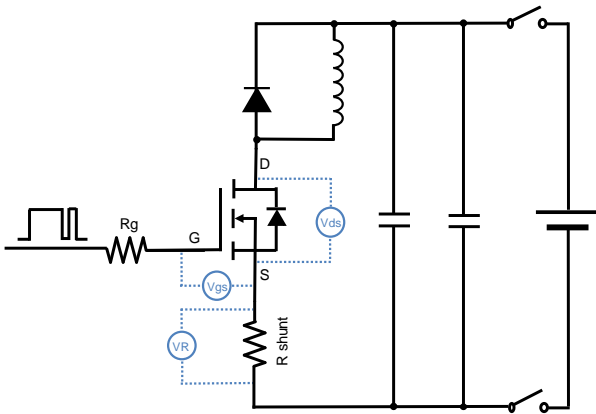


Figure C. Resistive Switching Test Circuit & Waveform

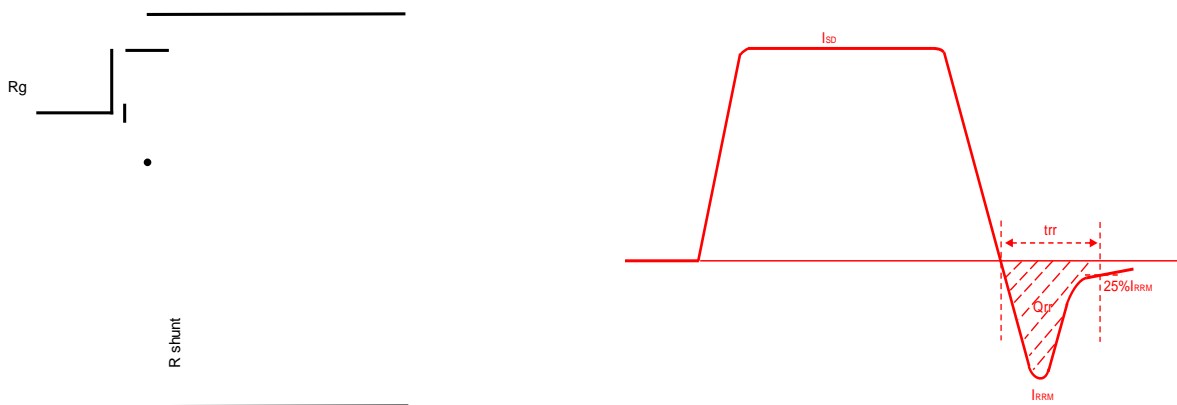


Figure D. Diode Recovery Test Circuit & Waveform



ITO-220AB-B Package information

B	
C	
C1	
D	
H	
L	



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