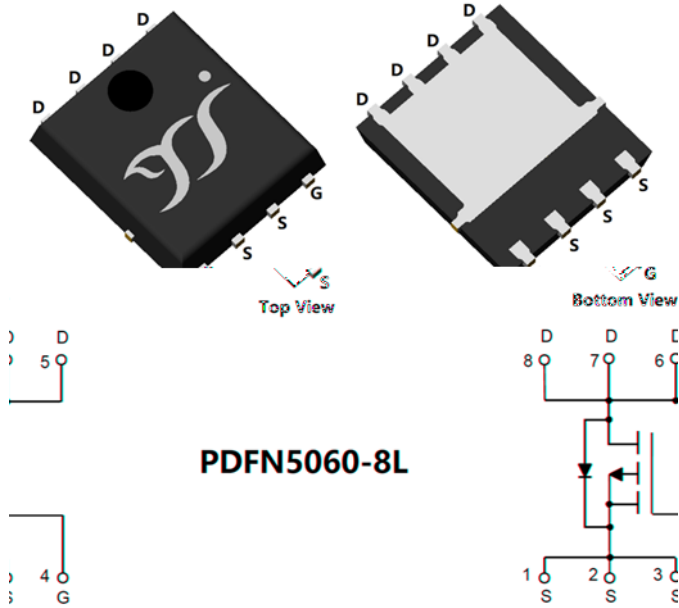




YJG055P10A

P-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L

Product Summary

V_{DS}	-100 V
I_D	-25 A
$R_{DS(ON)}$ (at $V_{GS}=-10V$)	55 m
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	64 m
100% EAS Tested	
100% V_{DS} Tested	

General Description

- Trench Power MOSFET technology
- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- High density cell design for low $R_{DS(on)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

Absolute Maximum Ratings ($T_J=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit	
Drain-source Voltage		V_{DS}	-100	V	
Gate-source Voltage		V_{GS}	± 20	V	
Continuous Drain Current (Note 1,2)	Steady-State	I_D	$T_A=25^\circ C$	-4	A
			$T_A=100^\circ C$	-2.5	
Continuous Drain Current (Note 1,3)	Steady-State		$T_C=25^\circ C$	-25	
			$T_C=100^\circ C$	-15.5	
Pulsed Drain Current	$T_C=25$, $t_p=100\mu s$	I_{DM}	-100	A	
Avalanche energy	$V_G=-10V$, R_G 2mH, $I_{AS}=-12A$	EAS	144	mJ	
Total Power Dissipation (Note 1,2)	Steady-State	P_D	$T_A=25^\circ C$	2.2	W
			$T_A=100^\circ C$	0.9	
Total Power Dissipation (Note 1,3)	Steady-State		$T_C=25^\circ C$	62.5	
			$T_C=100^\circ C$	25	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	$^\circ C$	

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	R	45	55	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	R	1.7	2	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG055P10A	F1	YJG055P10A	5000	10000	100000	13 reel



YJG055P10A

Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
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Static Parameter



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Typical Electrical and Thermal Characteristics Diagrams

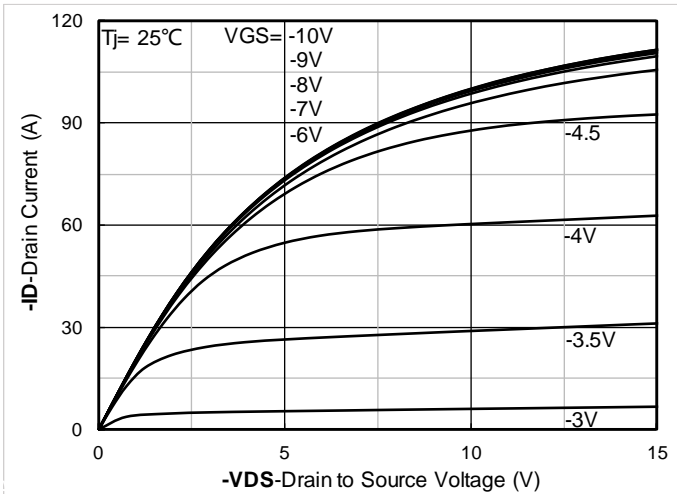


Figure 1. Output Characteristics

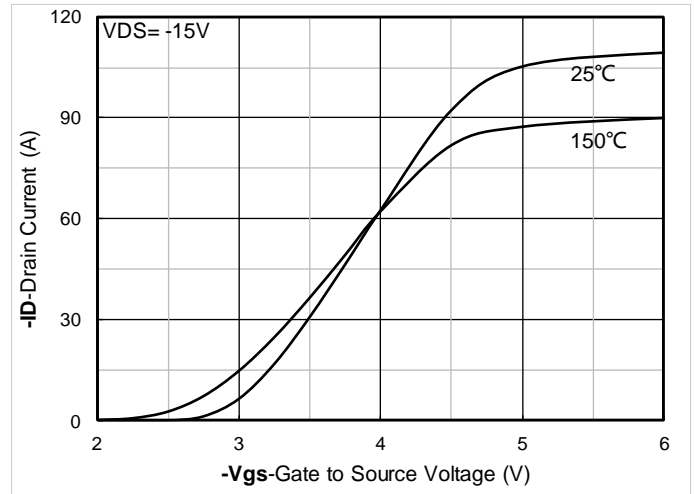


Figure 2. Transfer Characteristics

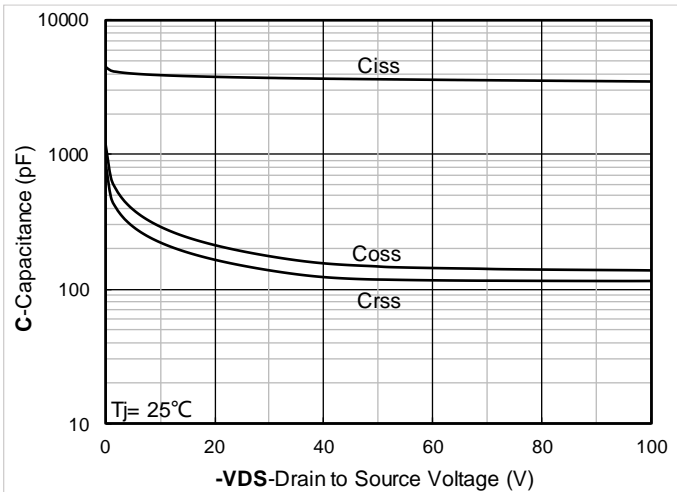


Figure 3. Capacitance Characteristics

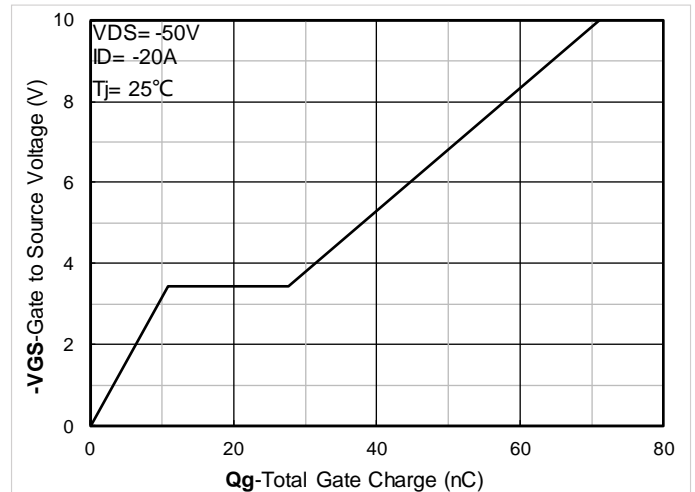


Figure 4. Gate Charge

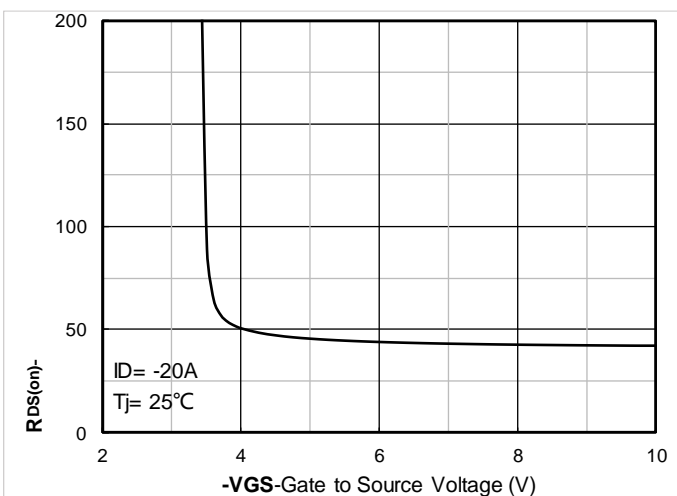


Figure 5. On-Resistance vs Gate to Source Voltage

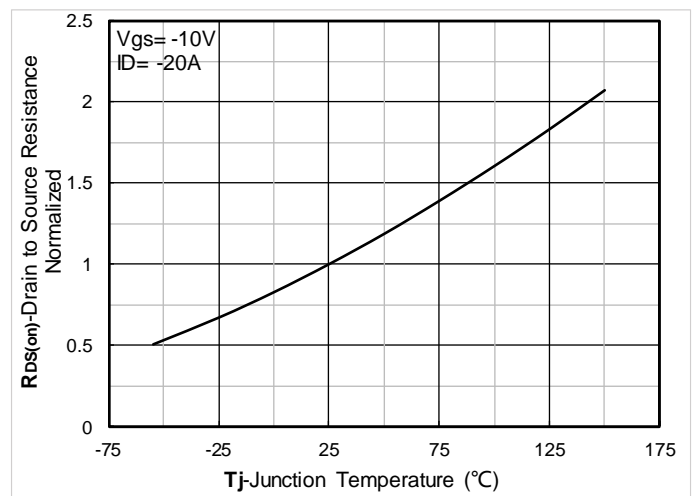


Figure 6. Normalized On-Resistance



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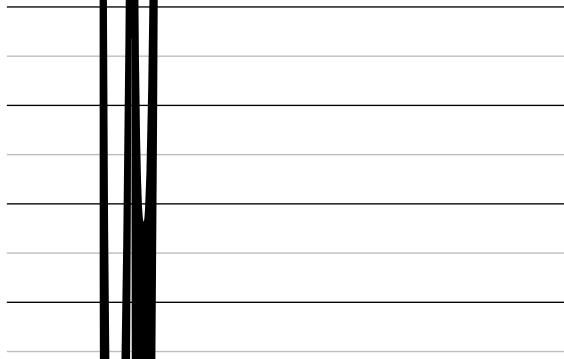


Figure 7. RDS(on) VS Drain Current

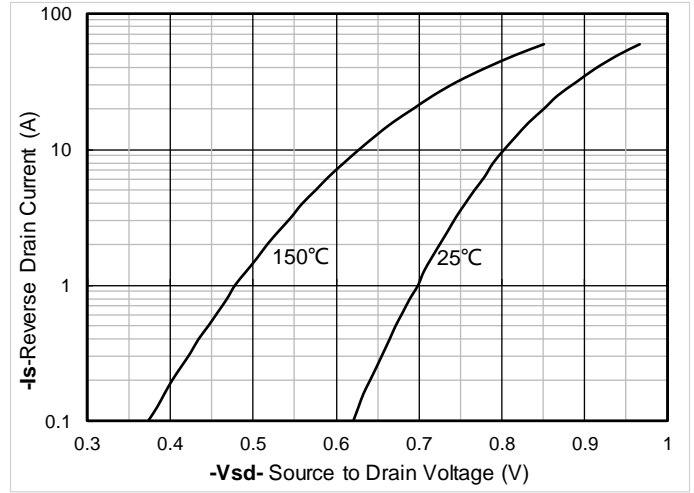


Figure 8. Forward characteristics of reverse diode

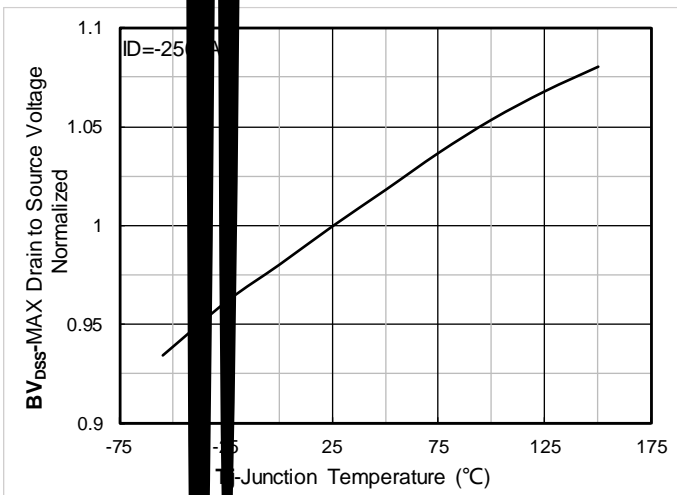


Figure 9. Normalized breakdown voltage

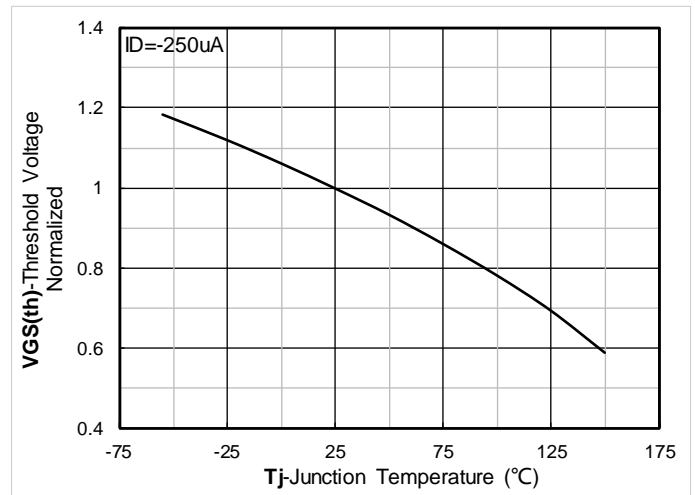


Figure 10. Normalized threshold voltage



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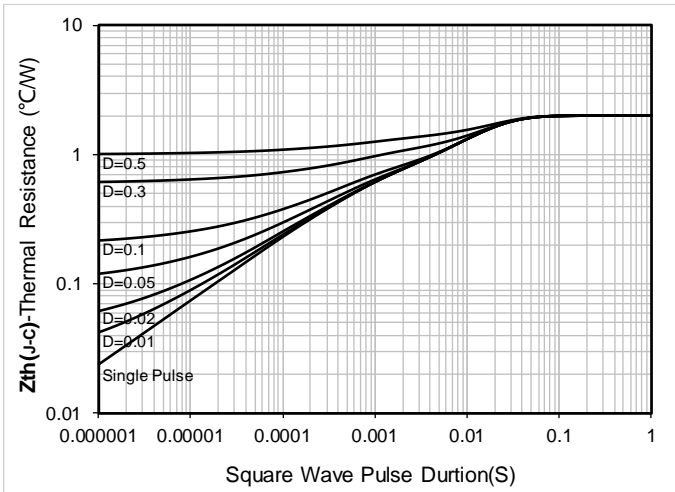


Figure 13. Maximum Transient Thermal Impedance

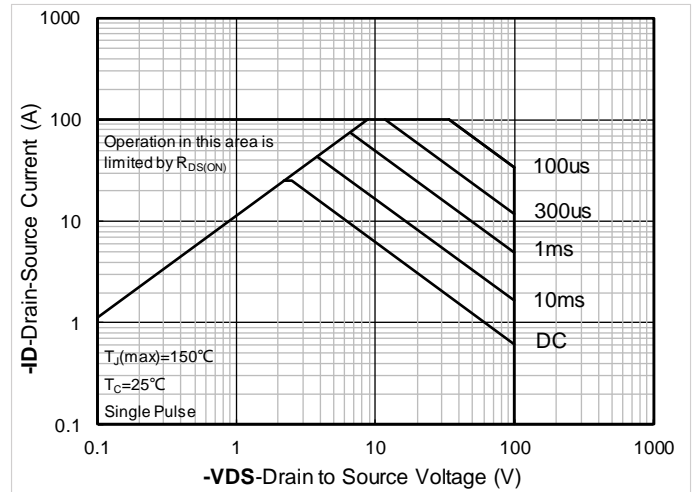
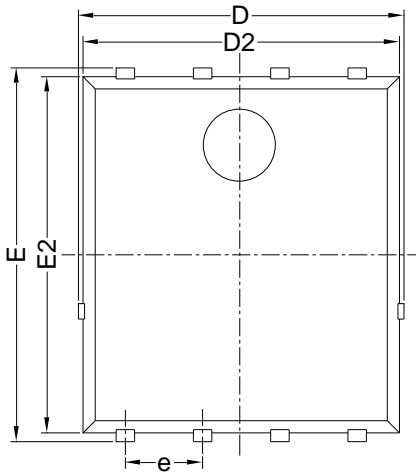


Figure 14. Safe Operation Area

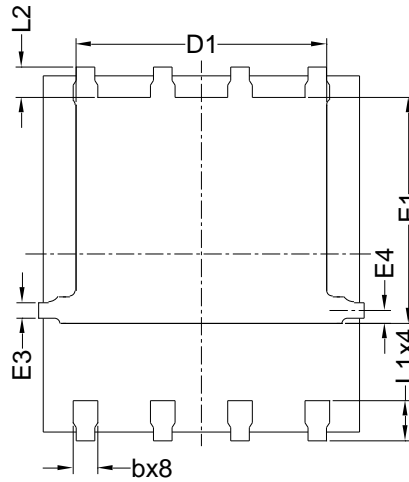


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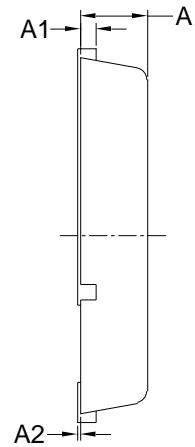
PDFN5060-8L-B-1.1MM Package information



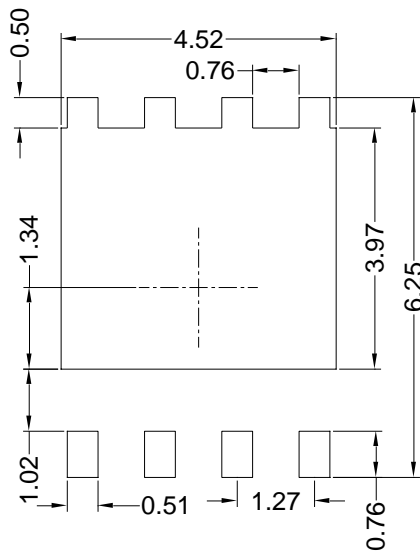
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



Disclaimer

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