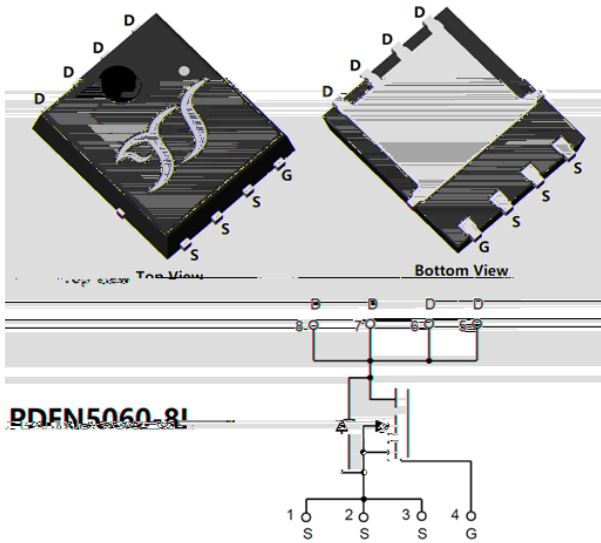




N-Channel Enhancement Mode Field Effect Transistor



Product Summary

V_{DS}	80V
I_D	100A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	4.5mohm
100% EAS Tested	
100% V_{DS} Tested	

General Description

Split gate trench MOSFET technology
 Excellent package for heat dissipation
 High density cell design for low $R_{DS(ON)}$
 Moisture Sensitivity Level 1
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

Battery protection
 Load switch
 Uninterruptible power supply

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	80	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25$	I_D	100	A
	$T_C=100$		63	
Pulsed Drain Current ^A		I_{DM}	400	A
Avalanche energy ^B		EAS	600	mJ
Total Power Dissipation ^C	$T_C=25$	P_D	152	W
	$T_C=100$		61	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	

Thermal resistance

Parameter		Symbol	Limit	Units
Thermal Resistance Junction-to-Ambient ^D	t 10S	R	22.3	/W
Thermal Resistance Junction-to-Ambient ^D	Steady-State		40.7	
Thermal Resistance Junction-to-Case	Steady-State	R	0.819	

Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG100G08A	F1	YJG100G08A	5000	10000	100000	13 reel



Typical Performance Characteristics

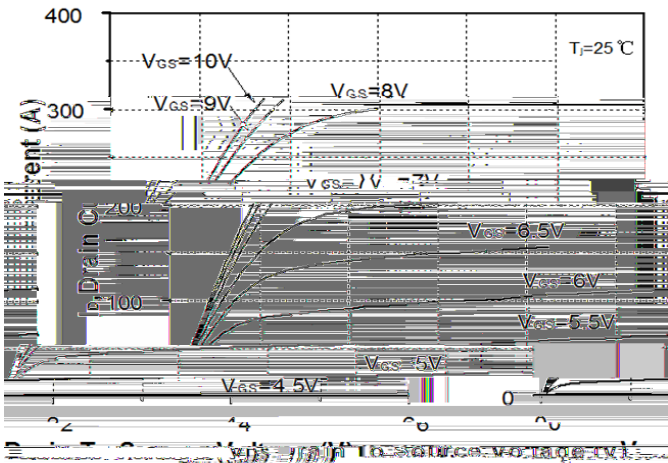


Figure1. Output Characteristics

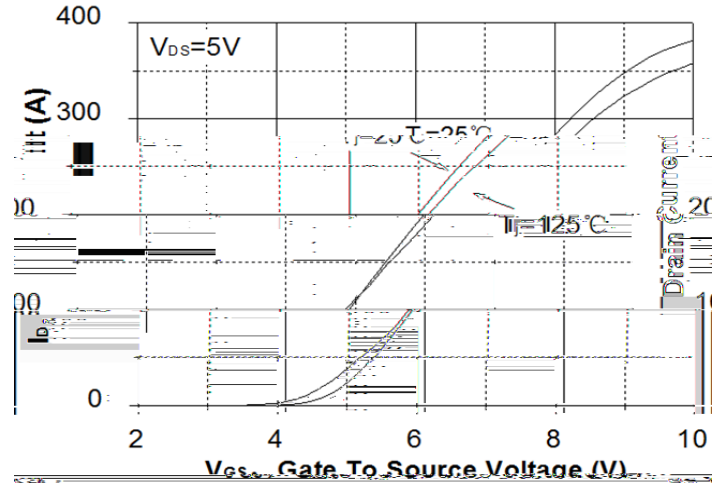


Figure2. Transfer Characteristics

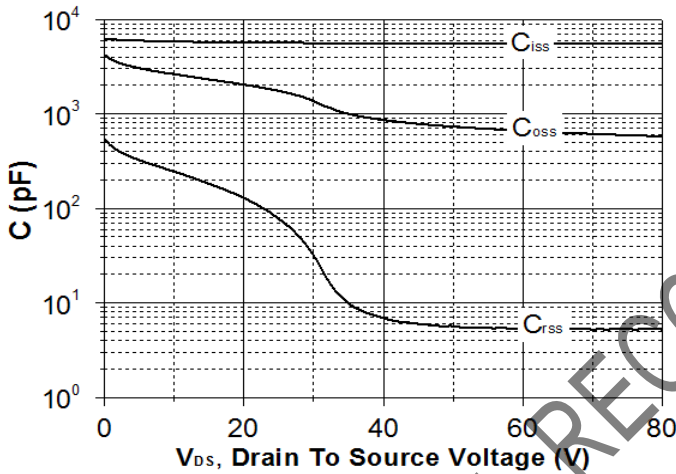


Figure3. Capacitance Characteristics

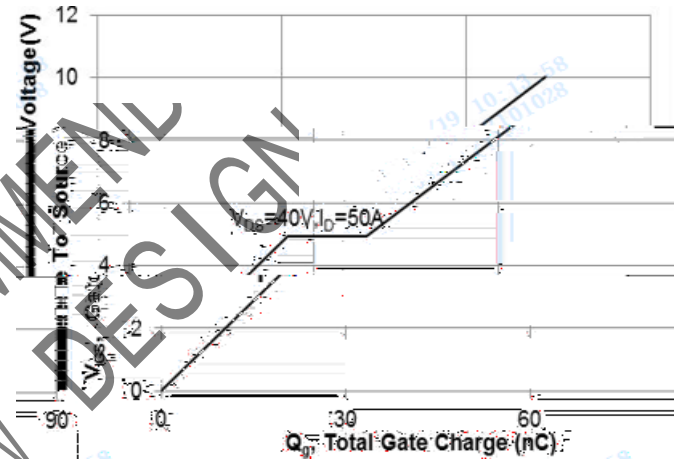


Figure4. Gate Charge

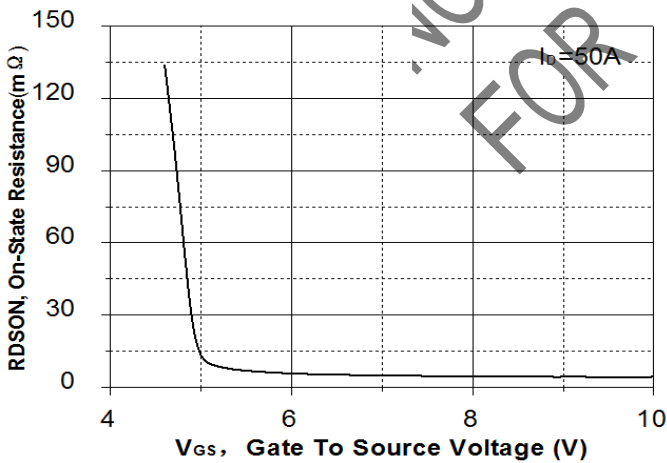


Figure5. On-Resistance vs. Gate to Source Voltage

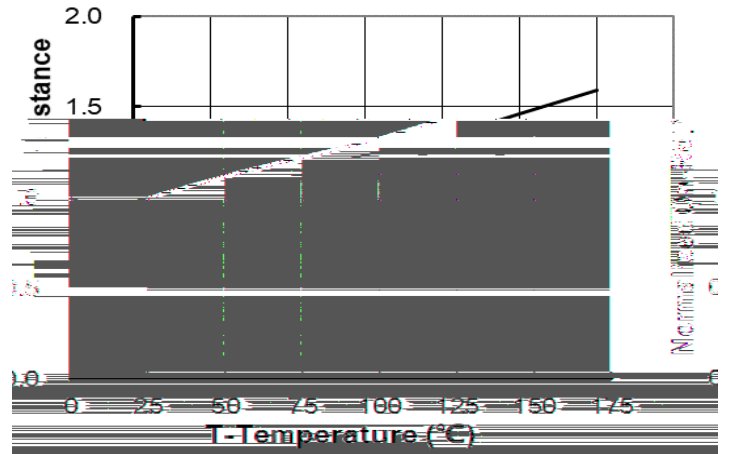
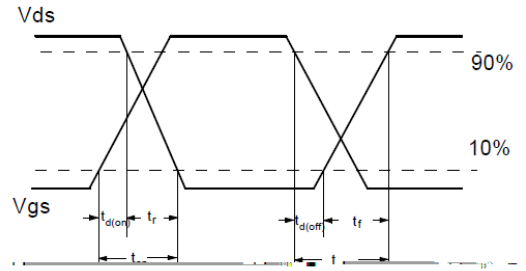
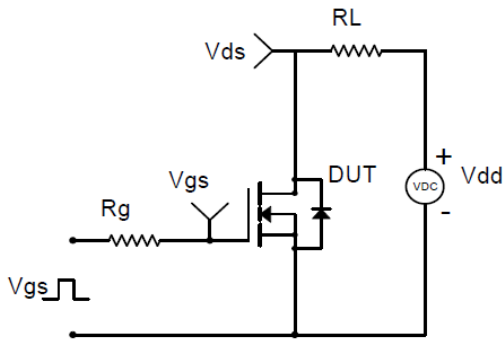


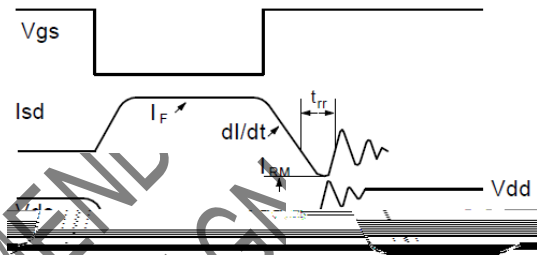
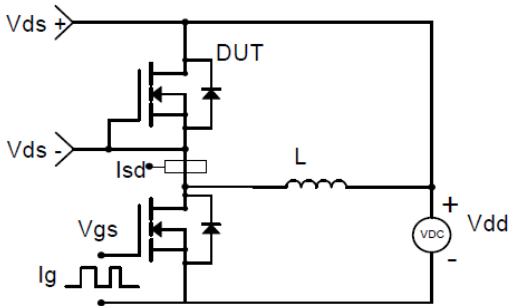
Figure6. Normalized On-Resistance

YJG100G08A

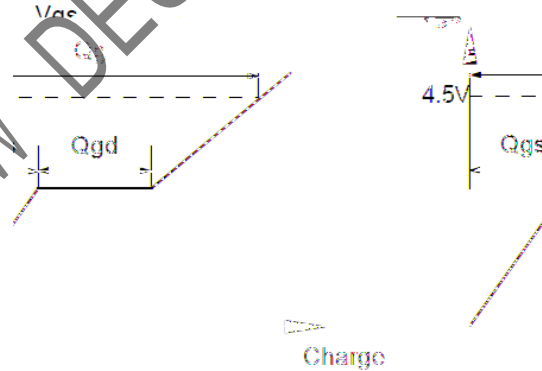
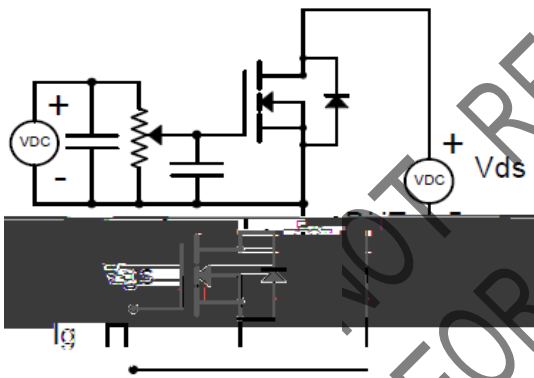
RECOMMEND
YJG90G08HJR
FOR NEW DESIGN



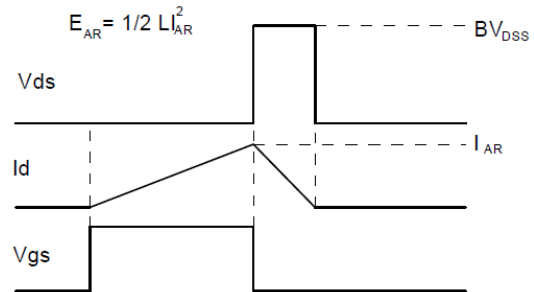
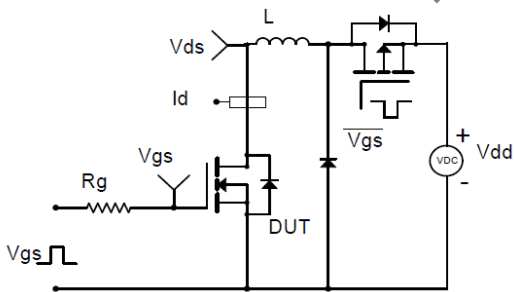
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform



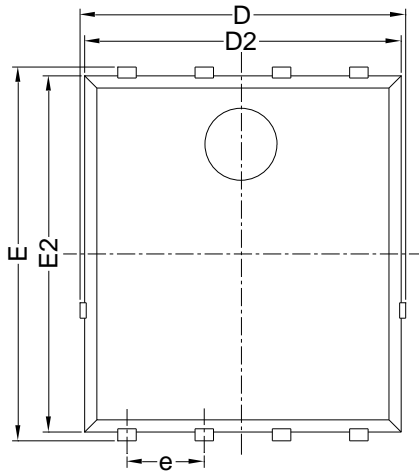
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



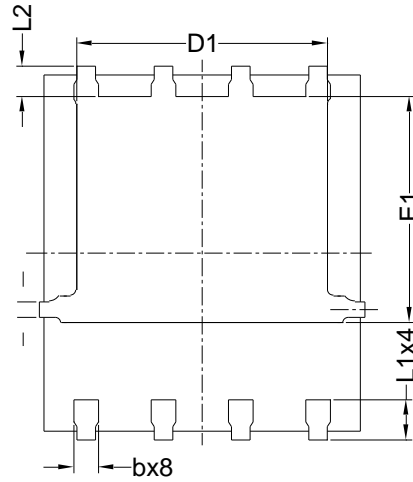
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RECOMMEND
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FOR NEW DESIGN

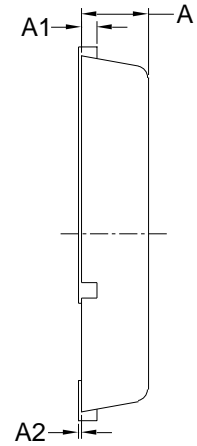
PDFN5060-8L-B-1.1MM Package information



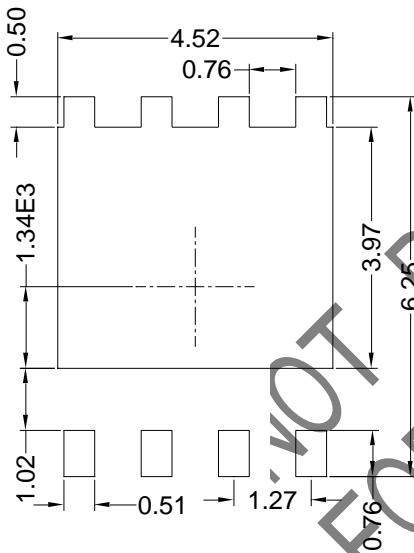
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2	0.10		
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



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