

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

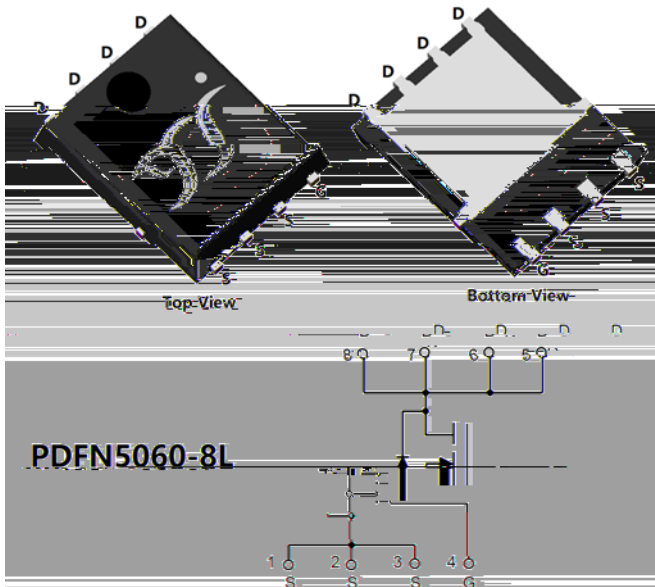
V_{DS}	40 V
I_D	100 A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	3.5 mohm
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	4.8 mohm
100% EAS Tested	
100% V_{DS} Tested	

General Description

Trench Power LV MOSFET technology
 Excellent package for heat dissipation
 High density cell design for low $R_{DS(ON)}$
 Moisture Sensitivity Level 1
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

DC-DC Converters
 Power management functions
 Backlighting



Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	40	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current	I_D	$T_C=25$	100
		$T_C=100$	63
Pulsed Drain Current ^A	I_{DM}	360	A
Total Power Dissipation @ $T_C=25$ ^B	P_D	83	W
Total Power Dissipation @ $T_C=100$ ^B	P_D	30	W
Total Power Dissipation @ $T_A=25$ ^C	P_D	6.2	W
Single Pulse Avalanche Energy ^D	E_{AS}	400	mJ
Thermal Resistance Junction-to-Case	R_{JC}	1.67	/ W
Thermal Resistance Junction-to-Ambient	R_{JA}	20	/ W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 +150	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG100N04A	F1	YJG100N04A	5000	10000	100000	13" reel



YJG100N04A

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	40			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ± 20V, V _{DS} =0V			± 100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =20A		2.8	3.5	mΩ
		V _{GS} = 4.5V, I _D =20A		4.0	4.8	
Diode Forward Voltage		I _S =20A, V _{GS} =0V		0.80		V

Maximum Body-Diode Continuous Current

Typical Performance Characteristics

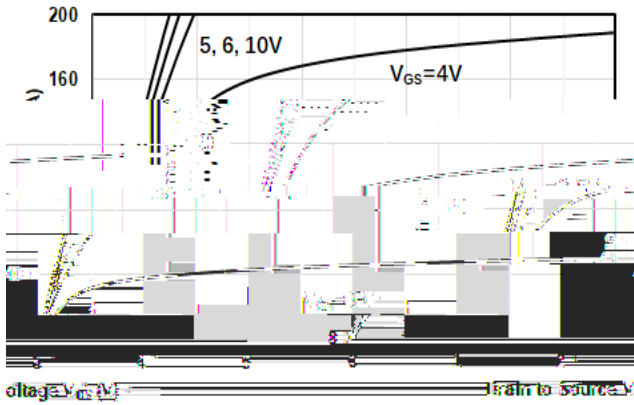


Figure1. Output Characteristics

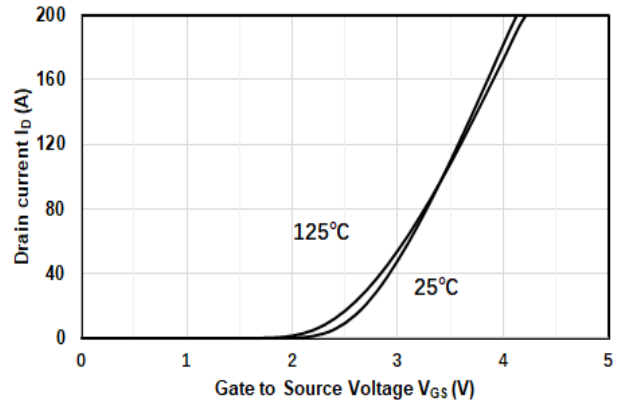


Figure2. Transfer Characteristics

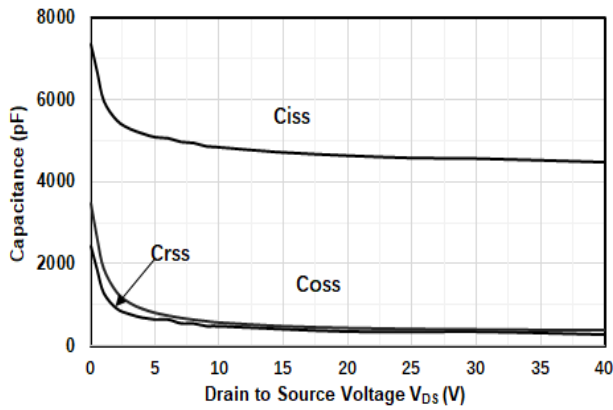


Figure3. Capacitance Characteristics

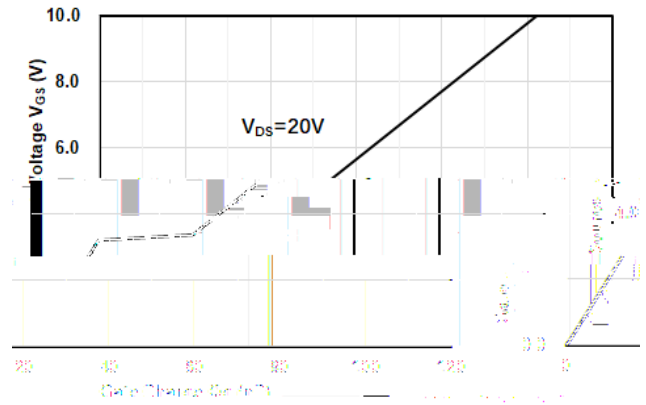


Figure4. Gate Charge

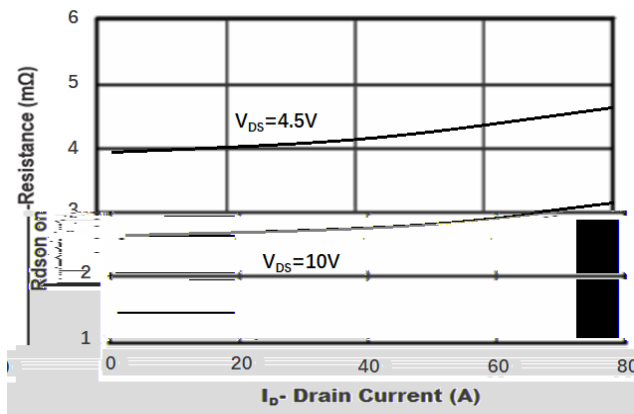


Figure5. Drain-Source on Resistance

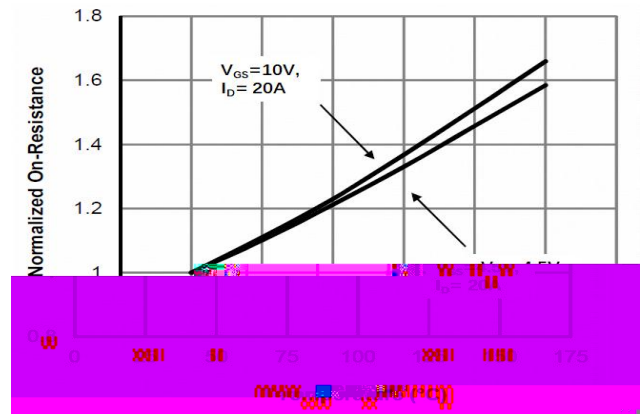


Figure6. Drain-Source on Resistance



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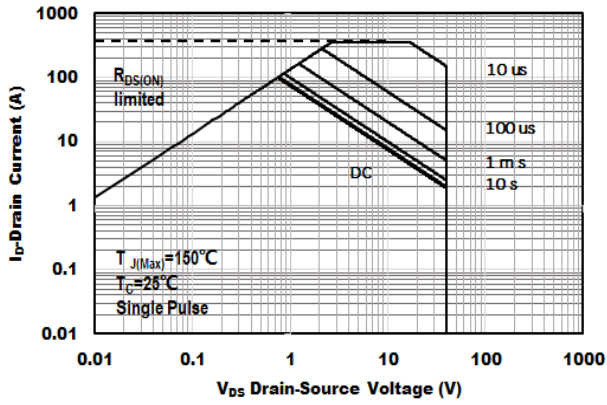


Figure7. Safe Operation Area

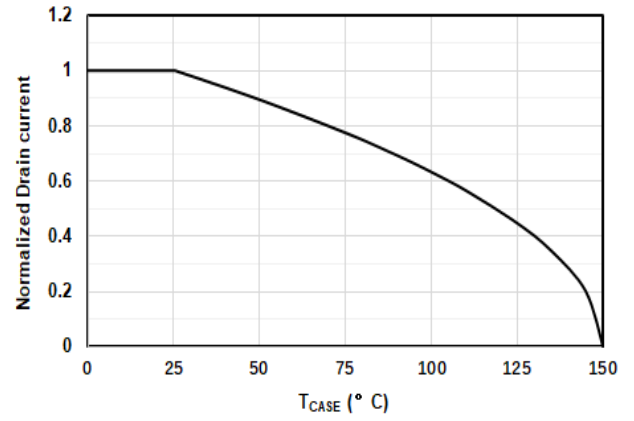


Figure8. Drain current vs. Case Temperature

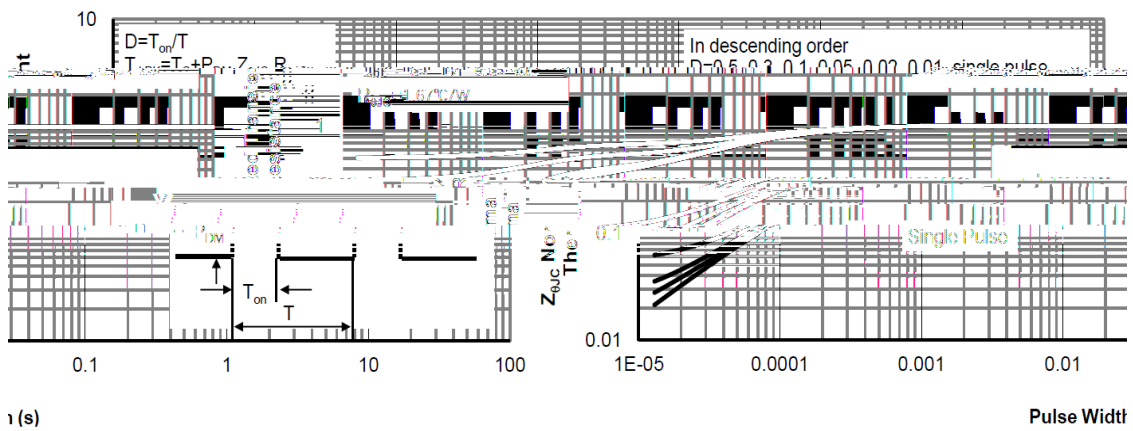
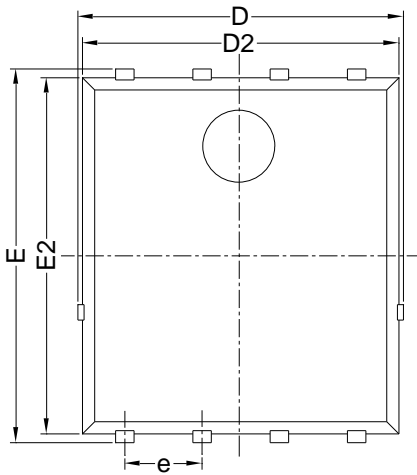


Figure9. Normalized Maximum Transient Thermal Impedance

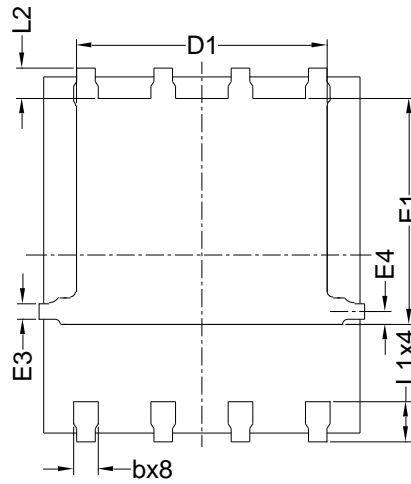


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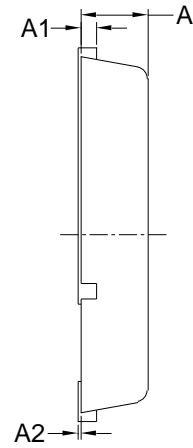
PDFN5060-8L-B-1.1MM Package information



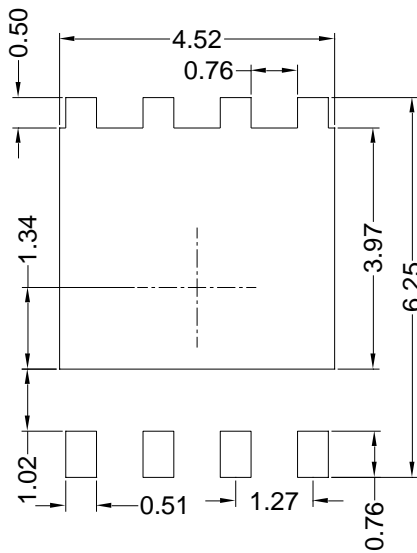
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



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The product listed herein is designed to be used with ordinary electronic equipment or devices, and not designed to be used with equipment or devices which require high level of reliability and the malfunction of which would directly endanger human life (such as