



YJG110G08HR

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	80V
I_D	110A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	3.9m
$R_{DS(ON)}$ (at $V_{GS}=6V$)	6m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Split gate trench MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Moisture Sensitivity Level 3
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

Power switching application
Uninterruptible power supply
DC-DC convertor

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}	80	V
Gate-source Voltage	V_{GS}	± 20	V

$T_A=25^{\circ}C$

Drain Current

I_D



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Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	80	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$	-	-	1	μA
		$V_{DS}=80V, V_{GS}=0V, T_J=150^\circ C$	-	-	100	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=55A$	-	2.9	3.9	m
		$V_{GS}=10V, I_D=20A$	-	2.9	3.9	
		$V_{GS}=6V, I_D=20A$	-	4.5	6	
Diode Forward Voltage	V_{SD}	$I_S=55A, V_{GS}=0V$	-	0.9	1.2	V
Gate resistance	R_G	$f=1MHz, \text{Open drain}$	-	2	-	
Maximum Body-Diode Continuous Current	I_S		-	-	110	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=40V, V_{GS}=0V, f=1MHz$	-	5290	-	μF
Output Capacitance	C_{oss}		-	870	-	
Reverse Transfer Capacitance	C_{riss}		-	445	-	
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=40V, I_D=55A$	-	68	-	nC
Gate-Source Charge	Q_{gs}		-	20	-	
Gate-Drain Charge	Q_{gd}		-	13	-	
Reverse Recovery Charge	Q_{rr}	$I_F=55A, di/dt=$				



Typical Electrical and Thermal Characteristics Diagrams

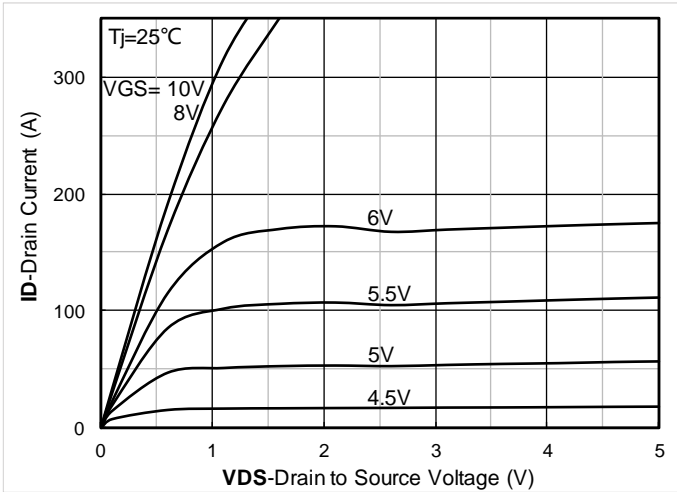


Figure 1. Output Characteristics

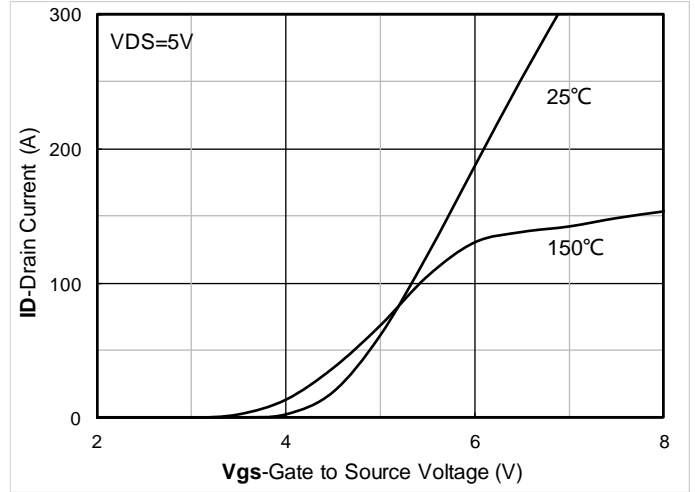


Figure 2. Transfer Characteristics

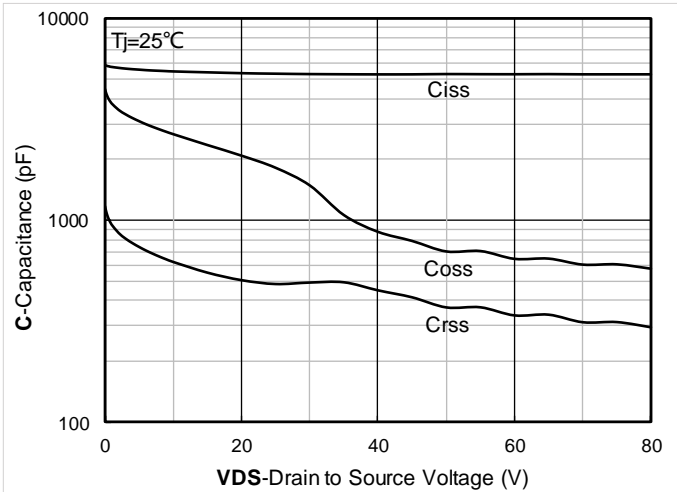


Figure 3. Capacitance Characteristics

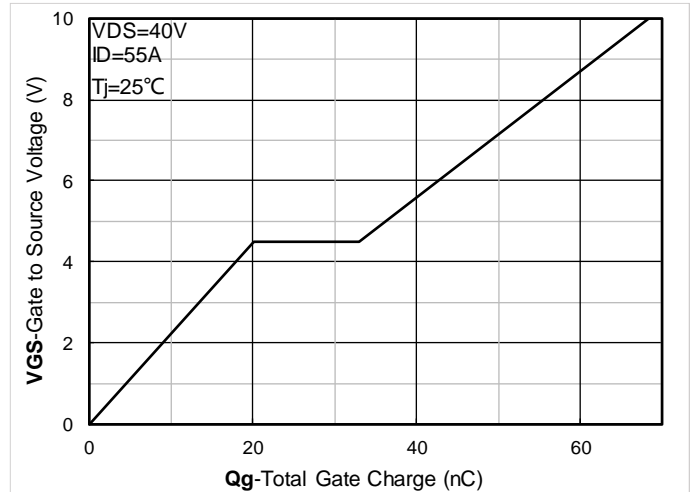


Figure 4. Gate Charge

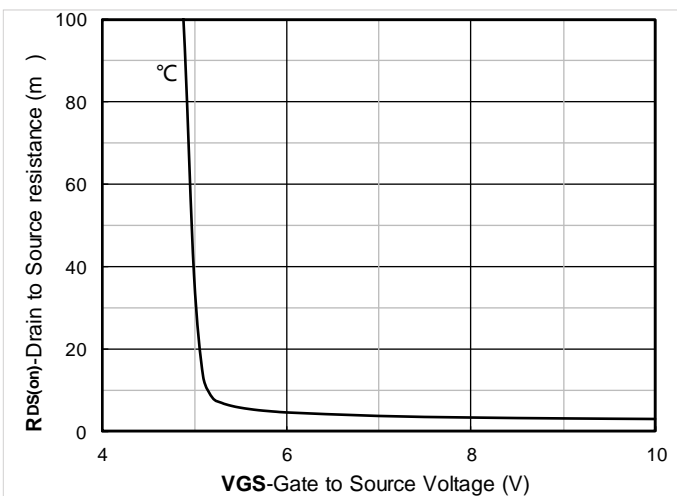


Figure 5. On-Resistance vs Gate to Source Voltage

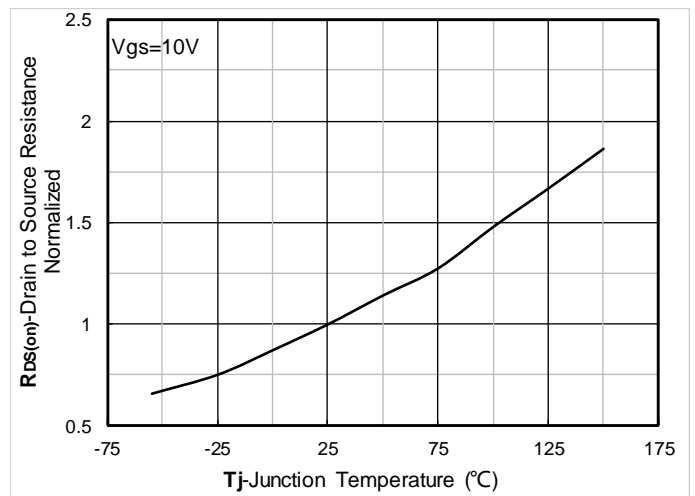


Figure 6. Normalized On-Resistance



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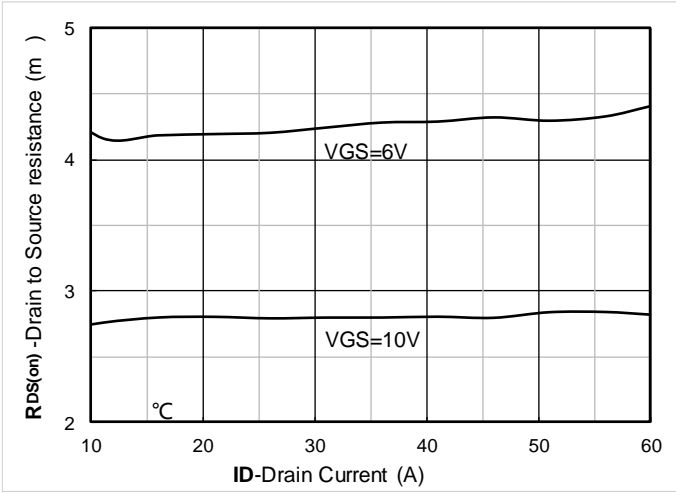


Figure 7. RDS(on) VS Drain Current

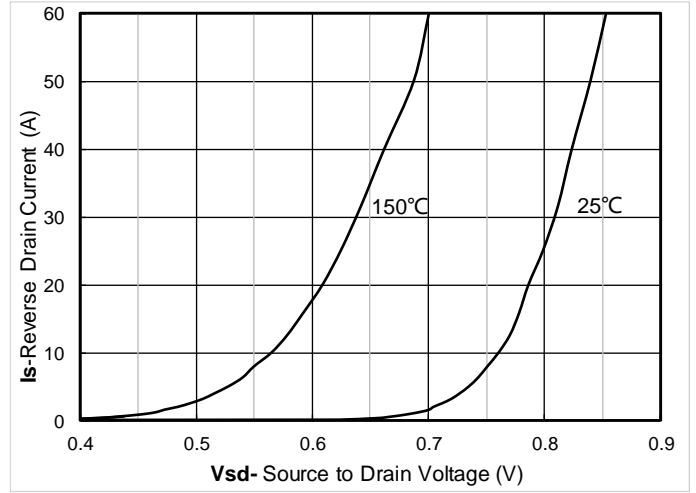


Figure 8. Forward characteristics of reverse diode

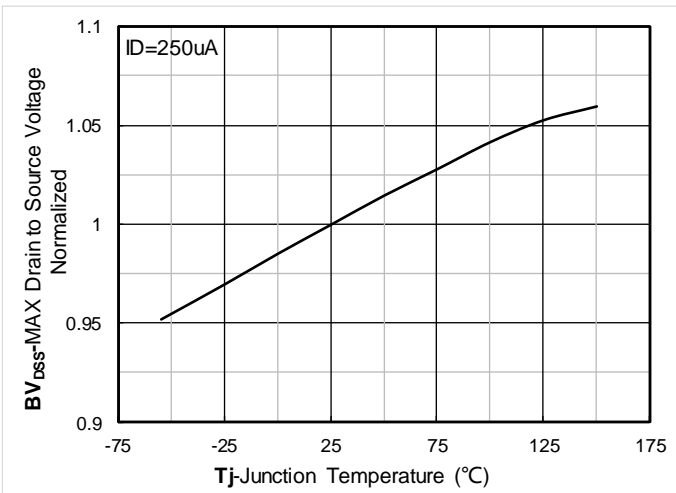


Figure 9. Normalized breakdown voltage

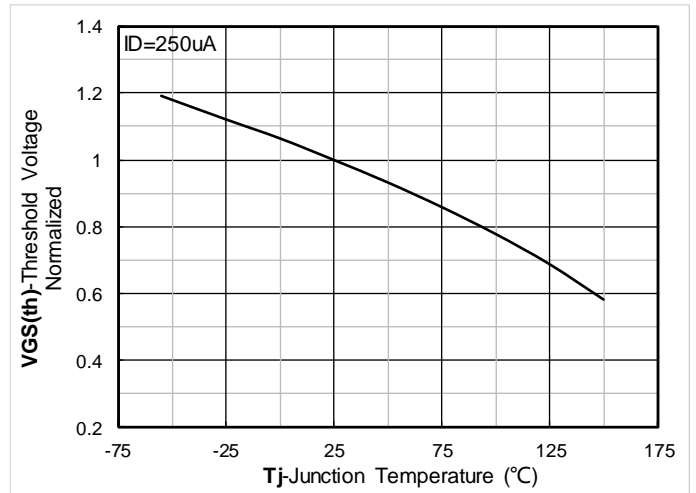


Figure 10. Normalized Threshold voltage

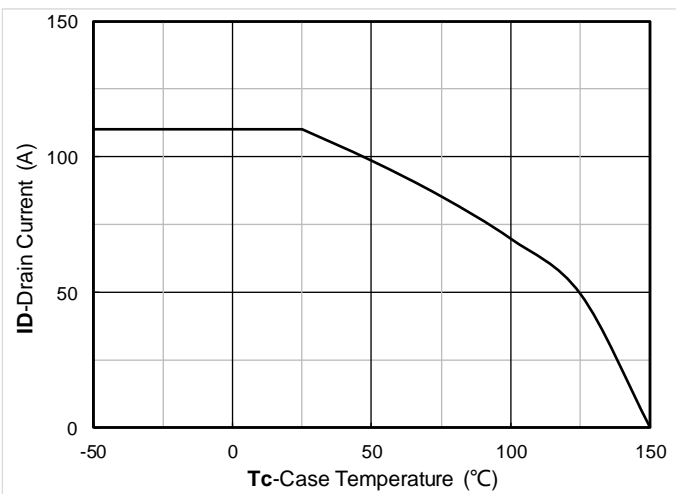


Figure 11. Current dissipation

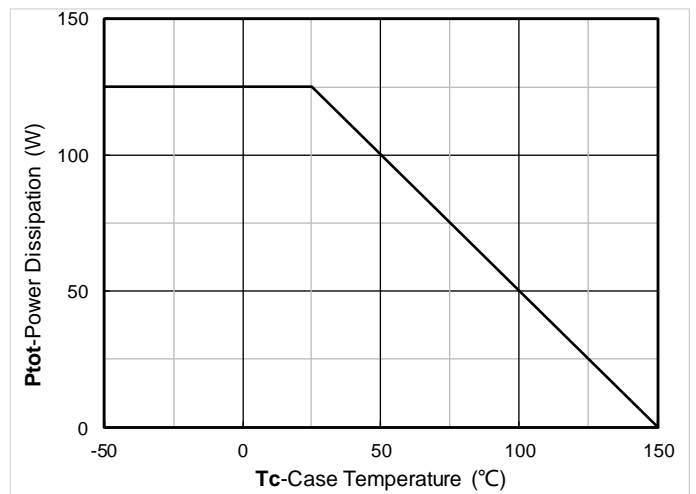


Figure 12. Power dissipation

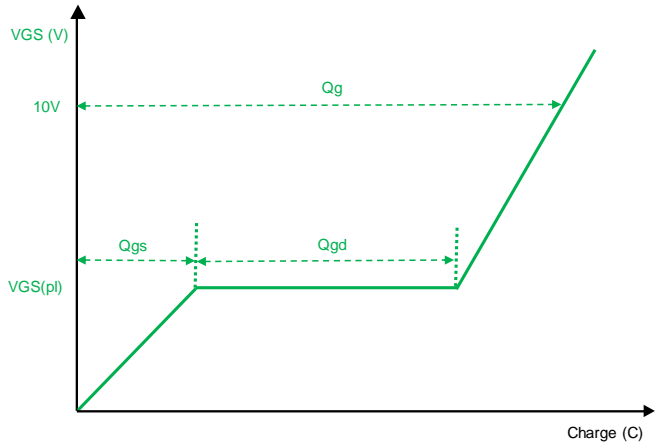
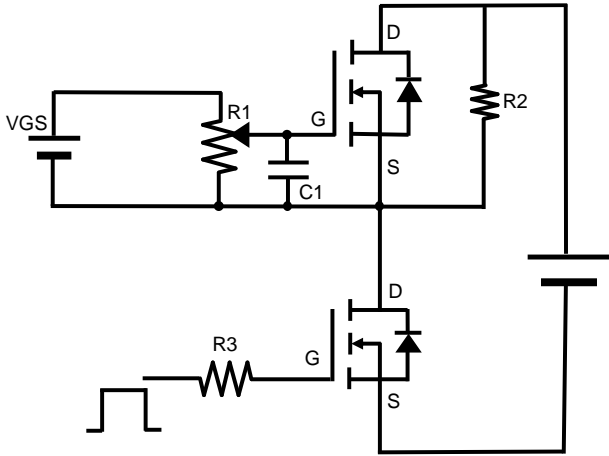


Figure B. Gate Charge Test Circuit & Waveform

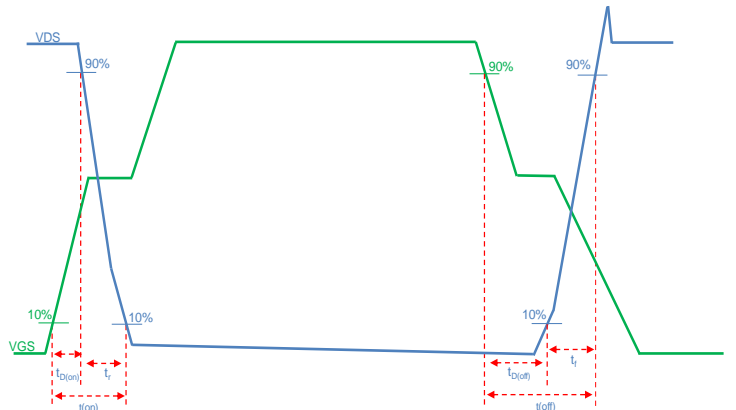
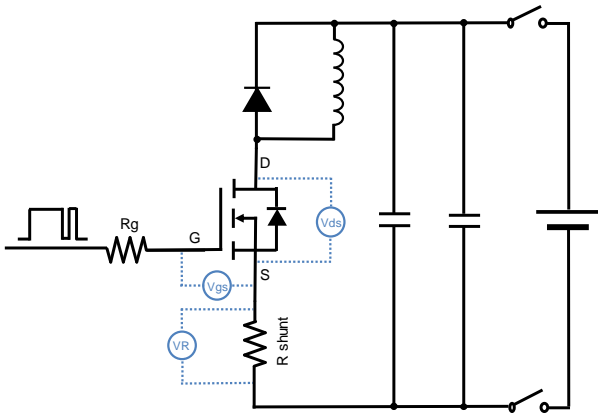


Figure C. Resistive Switching Test Circuit & Waveform

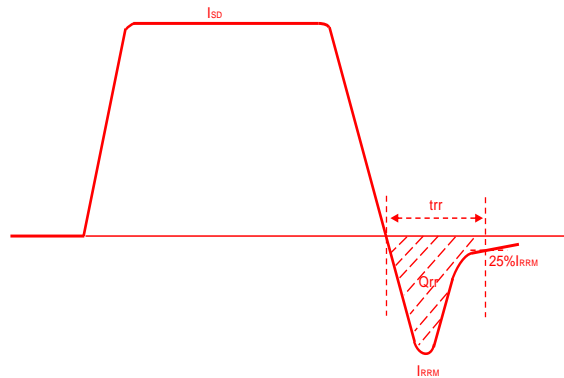
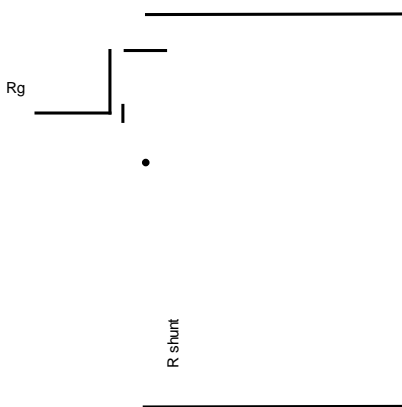
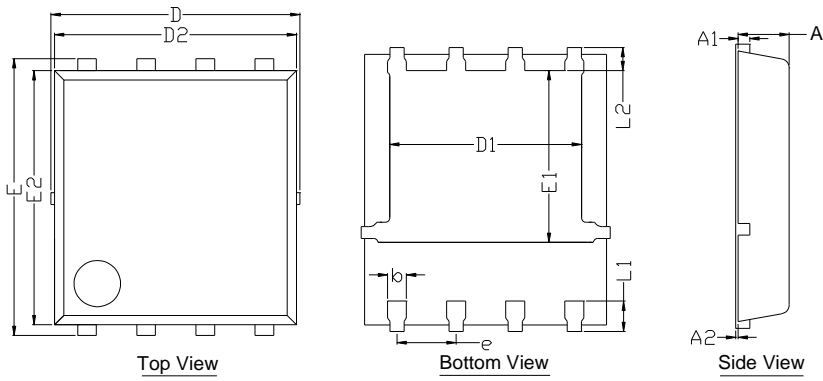


Figure D. Diode Recovery Test Circuit & Waveform

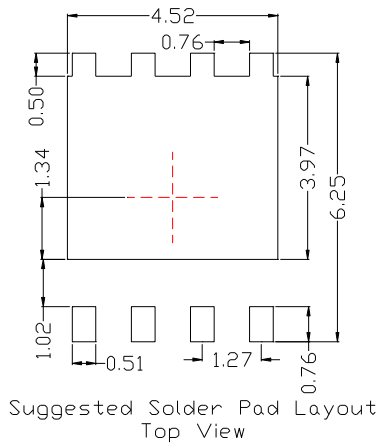


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PDFN5060-8L-D-0.95MM Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.05	6.15
A	0.85	0.95	1.00
A1	0.203 BSC		
A2			0.08
D1	4.25	4.35	4.45
E1	3.525	3.625	3.725
D2		5.20	
E2		5.55	
L1	0.45	0.55	0.65
L2	0.68 BSC		
b	0.3	0.4	0.5
e	1.27 BSC		



Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.10 mm.
 3. The pad layout is for reference purposes only.



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