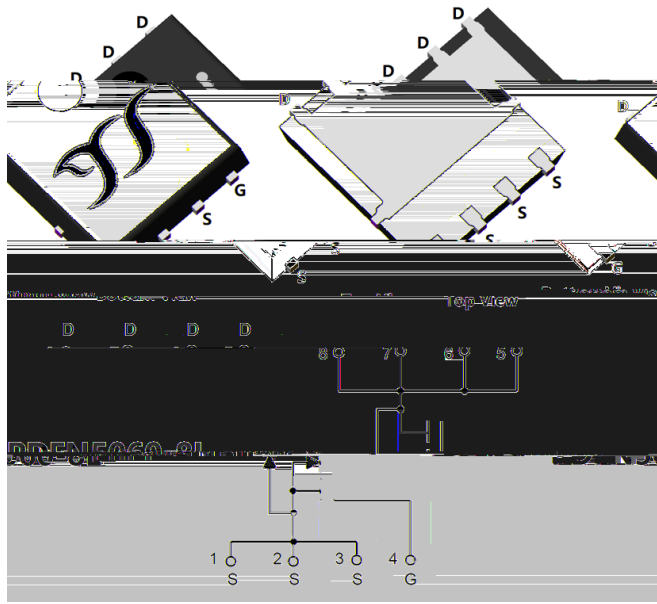




# N-Channel Enhancement Mode Field Effect Transistor



## Product Summary

$V_{DS}$	100V
$I_D$	110A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	5m
$R_{DS(ON)}$ ( at $V_{GS}=6V$ )	6.5m
100% EAS Tested	
100% $V_{DS}$ Tested	

## General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

## Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

### Absolute Maximum Ratings ( $T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	100	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^{\circ}C$	$I_D$	15	A
	$T_A=100^{\circ}C$		9.5	
	$T_C=25^{\circ}C$		110	
	$T_C=100^{\circ}C$		70	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	440	A
Avalanche energy <sup>B</sup>		EAS	400	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^{\circ}C$	$P_D$	2.4	W
	$T_A=100^{\circ}C$		0.9	
	$T_C=25^{\circ}C$		113	
	$T_C=100^{\circ}C$		45	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 +150	$^{\circ}C$

### Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State	$R_{JA}$	42	53	$^{\circ}C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{JC}$	0.88	1.1	

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG110G10B	F1	YJG110G10B	5000	10000	100000	13" reel



# YJG110G10B

## Electrical Characteristics ( $T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
		$V_{DS}=100V, V_{GS}=0V, T_J=150^\circ C$	-	-	100	
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=55A$	-	4	5	m
		$V_{GS}=10V, I_D=20A$	-	4	5	
		$V_{GS}=6V, I_D=20A$	-	5.2	6.5	
Diode Forward Voltage	$V_{SD}$	$I_S=55A, V_{GS}=0V$	-	0.8	1.2	V
Gate resistance	$R_G$	$f=1MHz$	-	0.8	-	
Maximum Body-Diode Continuous Current	$I_S$		-	-	110	A
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V, f=1MHz$	-	4300	-	$\mu F$
Output Capacitance	$C_{oss}$		-	1600	-	
Reverse Transfer Capacitance	$C_{rss}$		-	30	-	
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g$	$V_{GS}=10V, V_{DS}=50V, I_D=55A$	-	55	-	nC
Gate-Source Charge	$Q_{gs}$		-	16	-	
Gate-Drain Charge	$Q_{gd}$		-	14	-	
Reverse Recovery Charge	$Q_{rr}$	$I_F=55A, di/dt=350A/us$	-	165	-	nC
Reverse Recovery Time	$t_{rr}$		-	47	-	ns

Turn-on DQq27202.234.07 Tm0 g0 G[ ]T225



# YJG110G10B

## Typical Electrical and Thermal Characteristics Diagrams

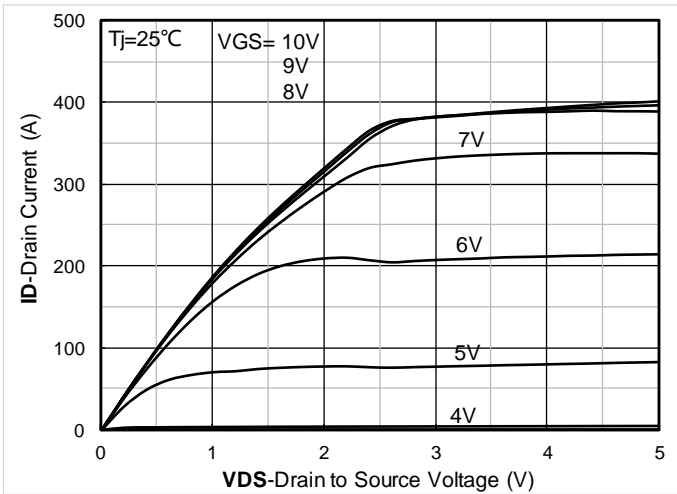


Figure 1. Output Characteristics

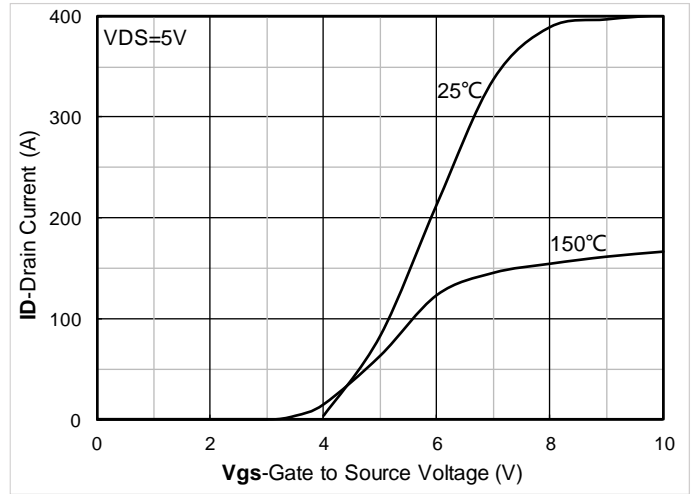


Figure 2. Transfer Characteristics

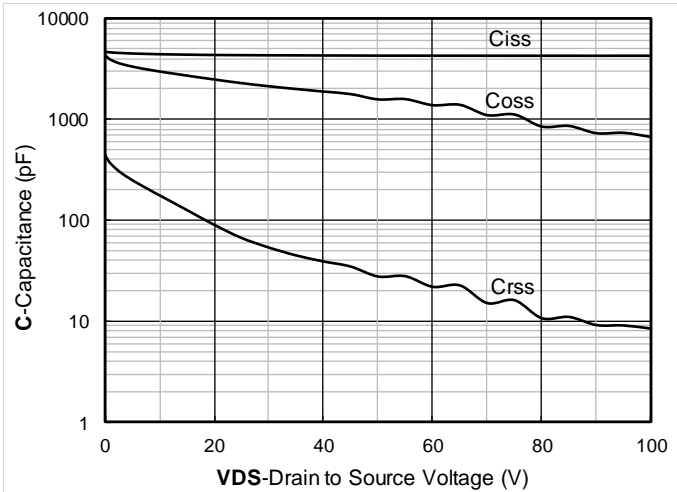


Figure 3. Capacitance Characteristics

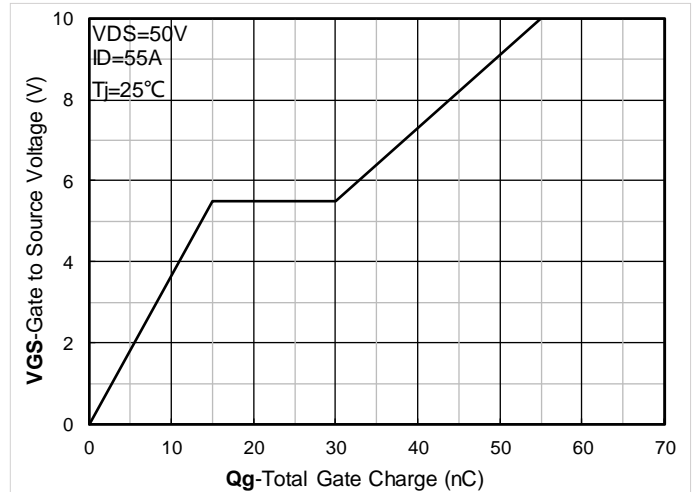


Figure 4. Gate Charge

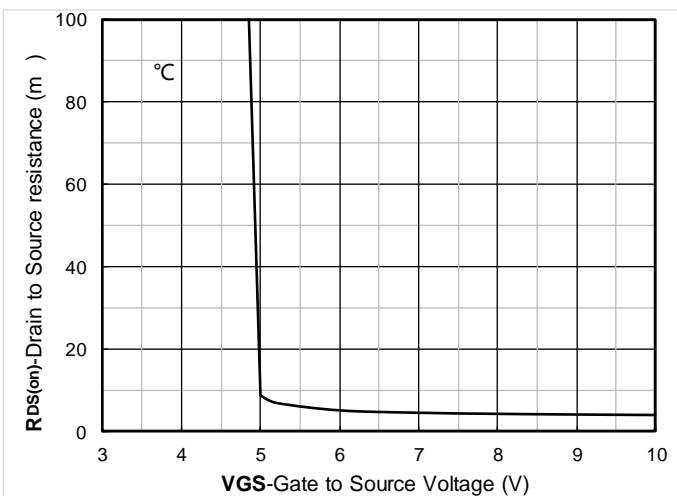


Figure 5. On-Resistance vs Gate to Source Voltage

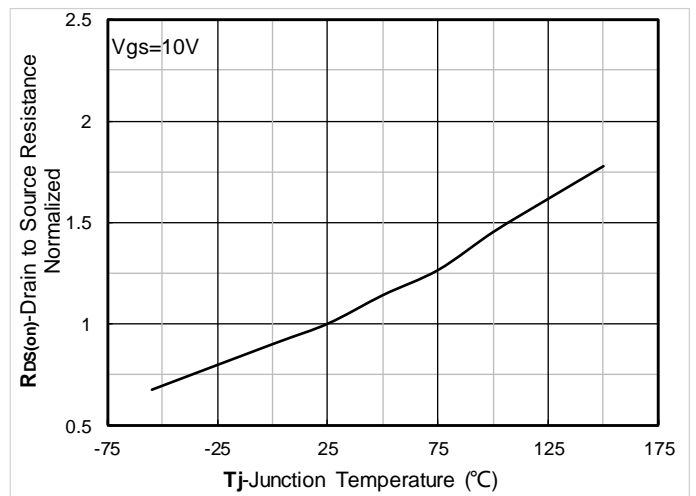


Figure 6. Normalized On-Resistance



# YJG110G10B

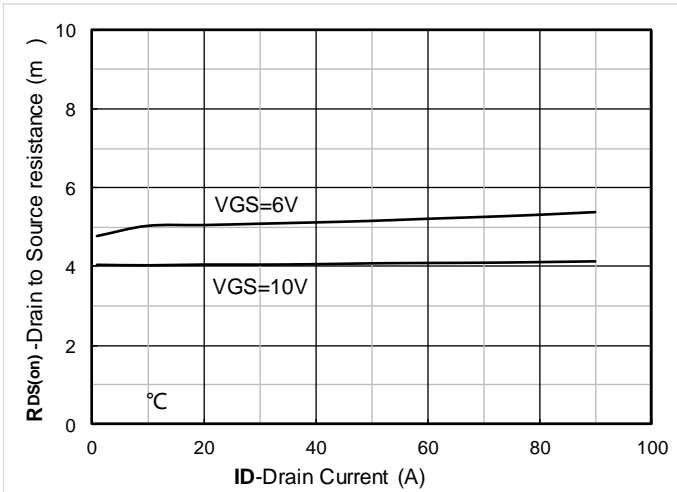


Figure 7.  $R_{DS(on)}$  VS Drain Current

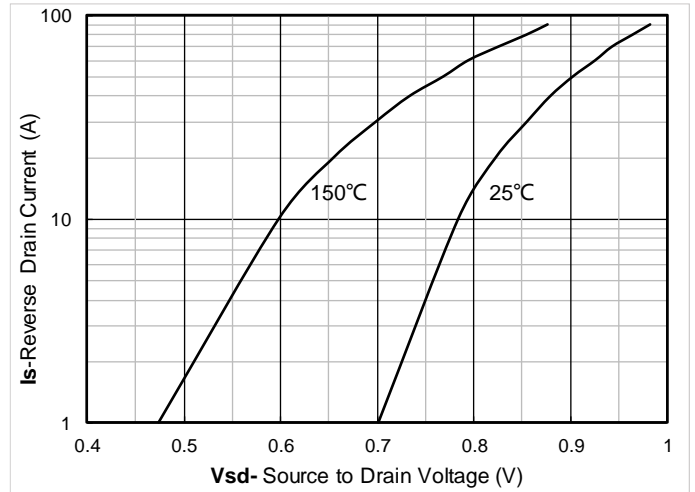


Figure 8. Forward characteristics of reverse diode

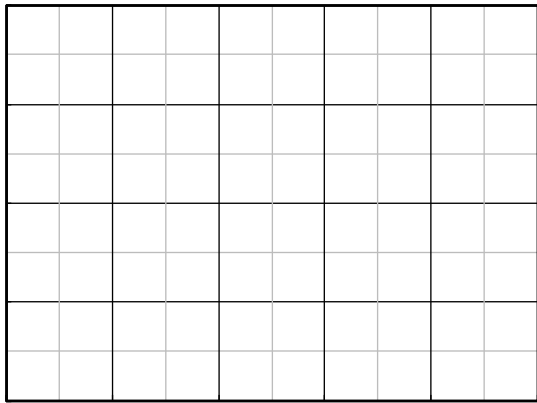


Figure 9. Normalized breakdown voltage

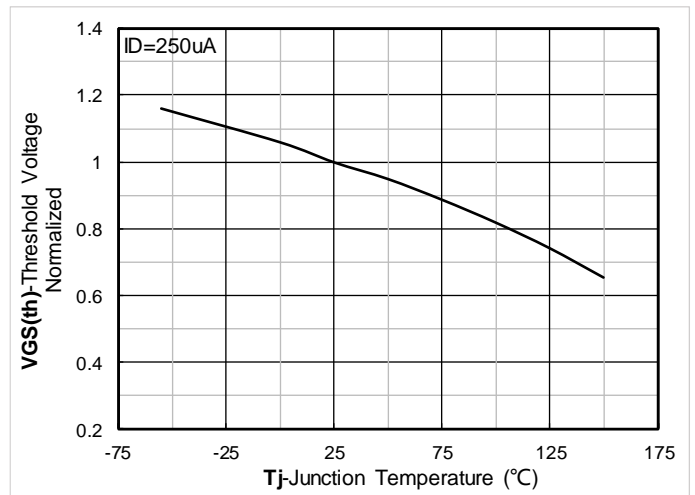


Figure 10. Normalized Threshold voltage

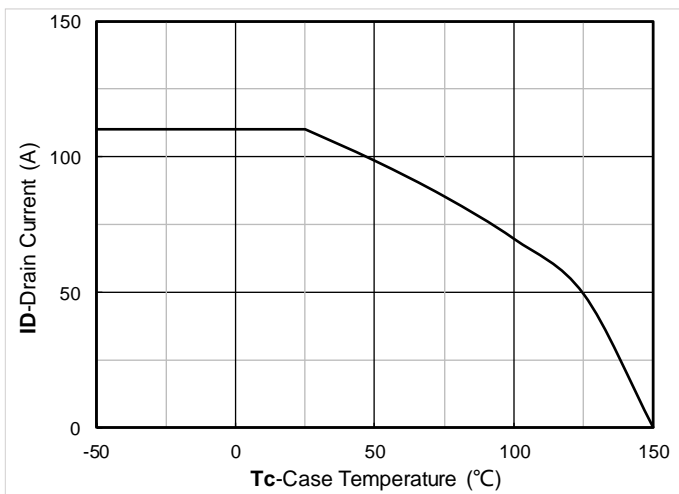


Figure 11. Current dissipation

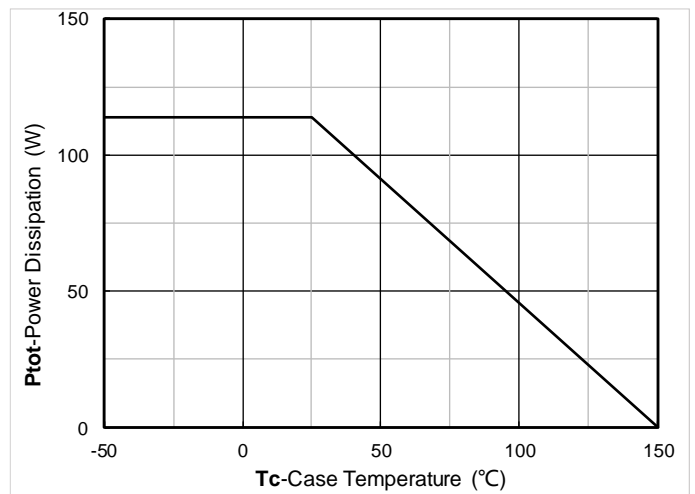


Figure 12. Power dissipation

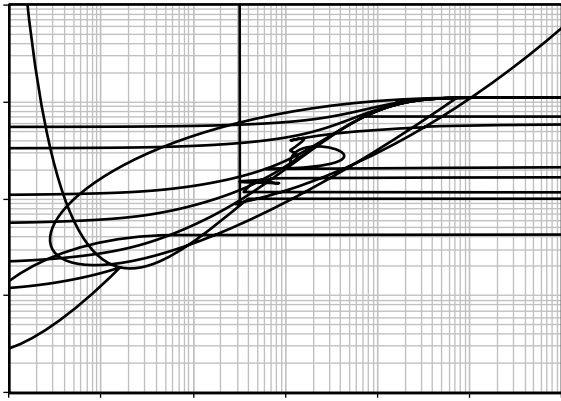


Figure 13. Maximum Transient Thermal Impedance

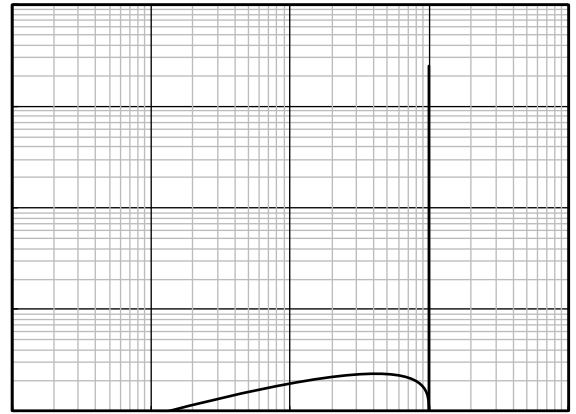


Figure 14. Safe Operation Area

## Test Circuits & Waveforms

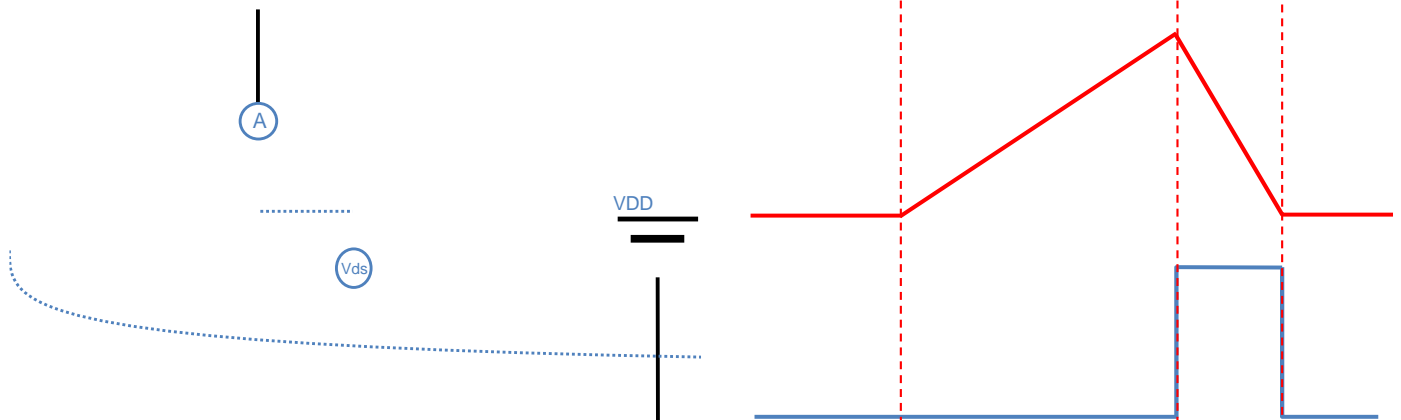


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

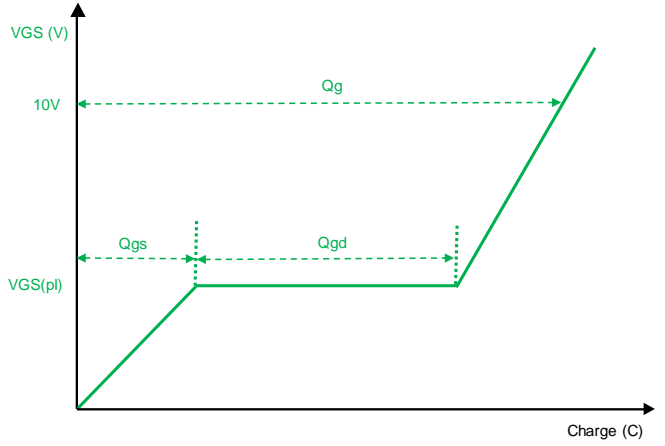
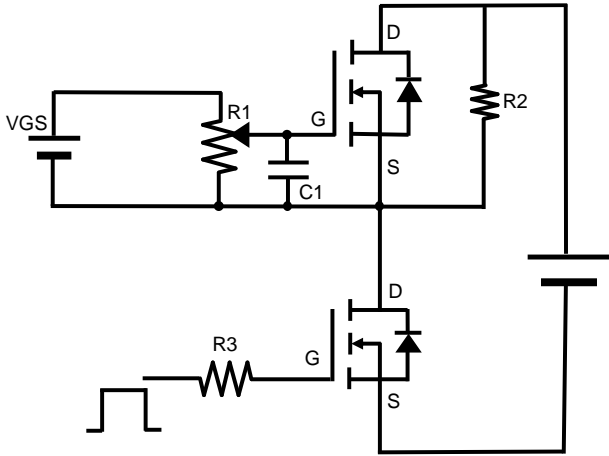


Figure B. Gate Charge Test Circuit & Waveform

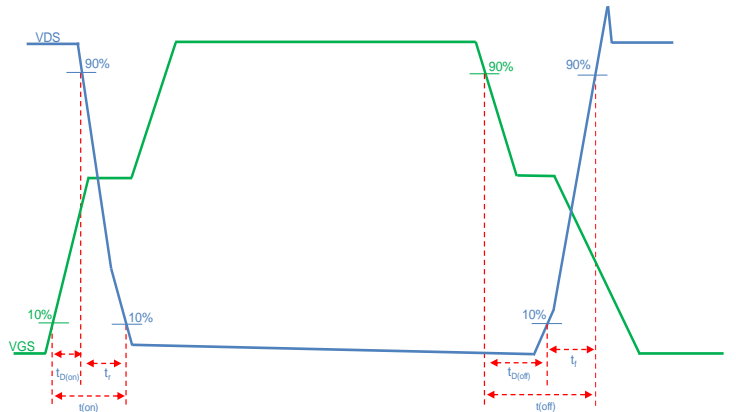
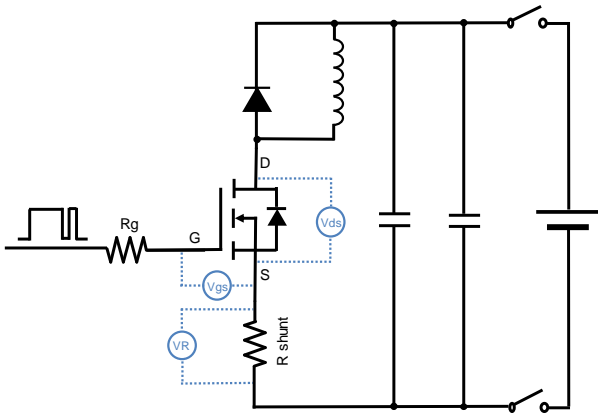


Figure C. Resistive Switching Test Circuit & Waveform

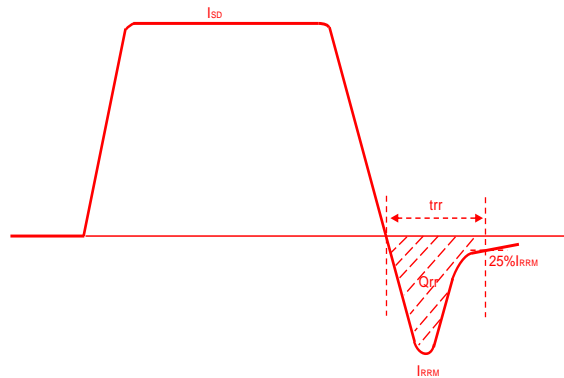
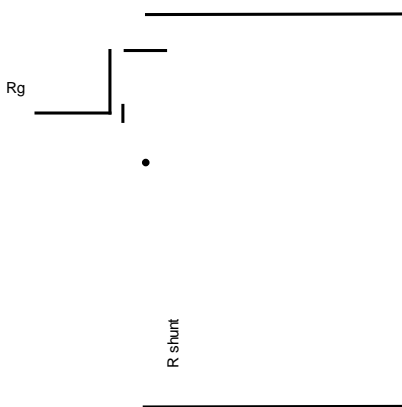
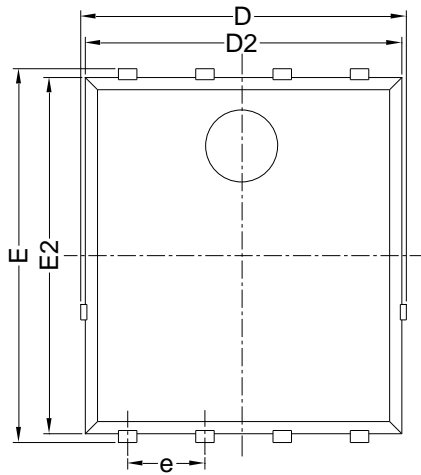


Figure D. Diode Recovery Test Circuit & Waveform

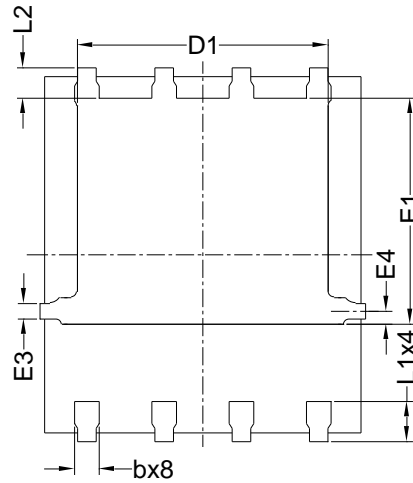


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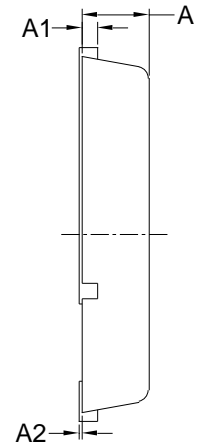
## PDFN5060-8L-B-1.1MM Package information



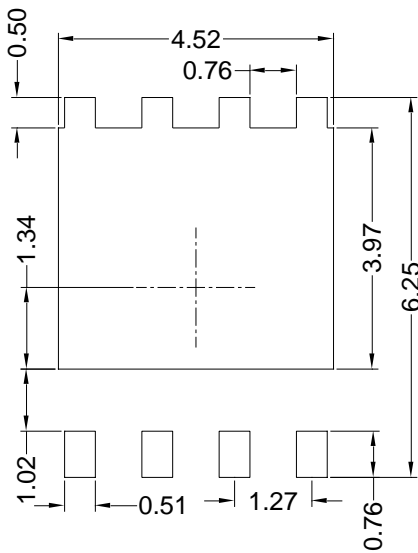
Top View



Bottom View



Side View



Suggested Solder Pad Layout  
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



# YJG110G10B

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