



N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	30V
I_D	170A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	1.3m
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	2.5m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Split gate trench MOSFET technology
 Excellent package for heat dissipation
 High density cell design for low $R_{DS(ON)}$
 Moisture Sensitivity Level 3
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

Motor Drivers
 Switching Voltage Regulators
 DC-DC convertor

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	30	A
			19	
	$T_C=25^\circ C$		170	
	$T_C=100^\circ C$		107.5	
Pulsed Drain Current ^A		I_{DM}	400	A
Avalanche energy ^B		EAS	645	mJ
		$T_A=25^\circ C$	2.5	
Total Power Dissipation ^C		P_D		W



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Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V



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Typical Electrical and Thermal Characteristics Diagrams

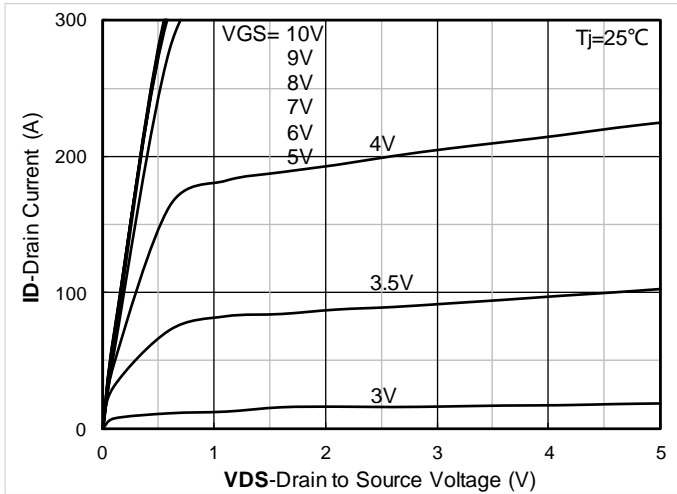


Figure 1. Output Characteristics

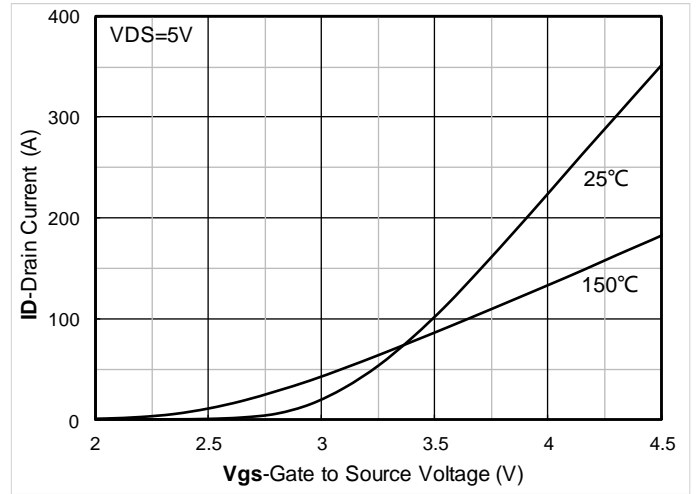


Figure 2. Transfer Characteristics

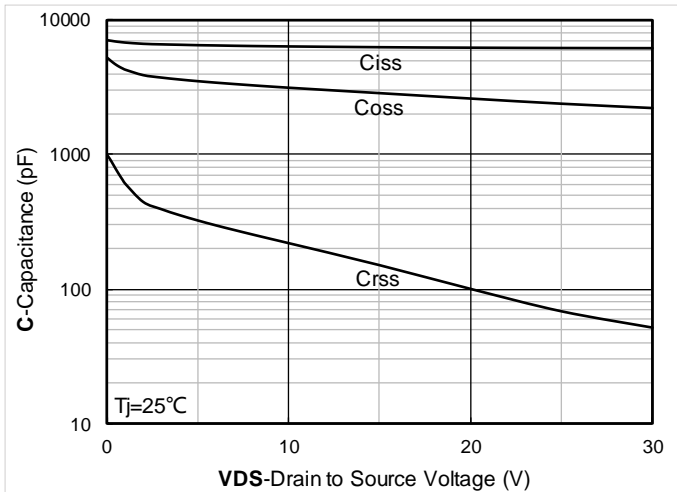


Figure 3. Capacitance Characteristics

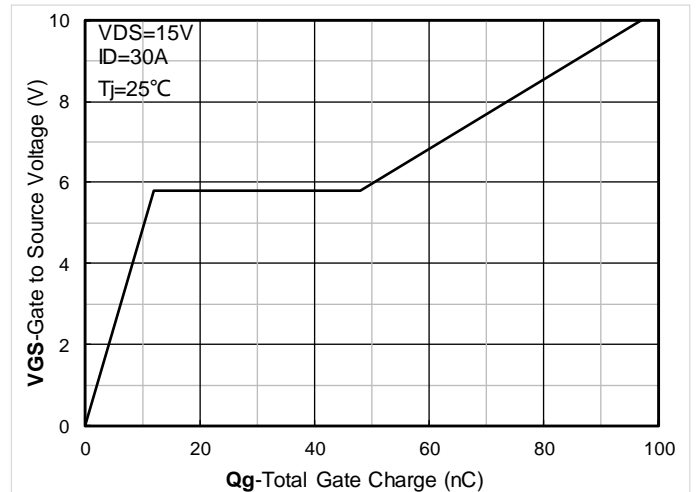


Figure 4. Gate Charge

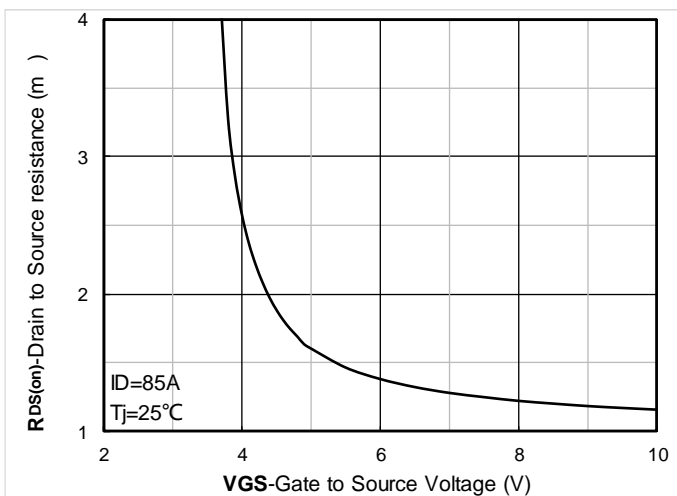


Figure 5. On-Resistance vs Gate to Source Voltage

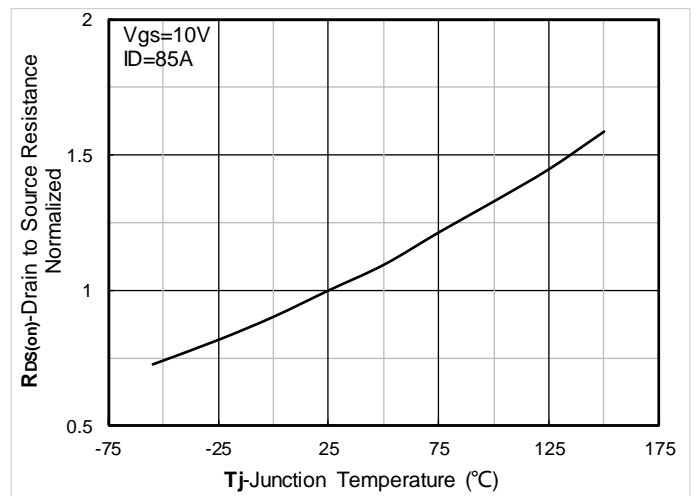


Figure 6. Normalized On-Resistance



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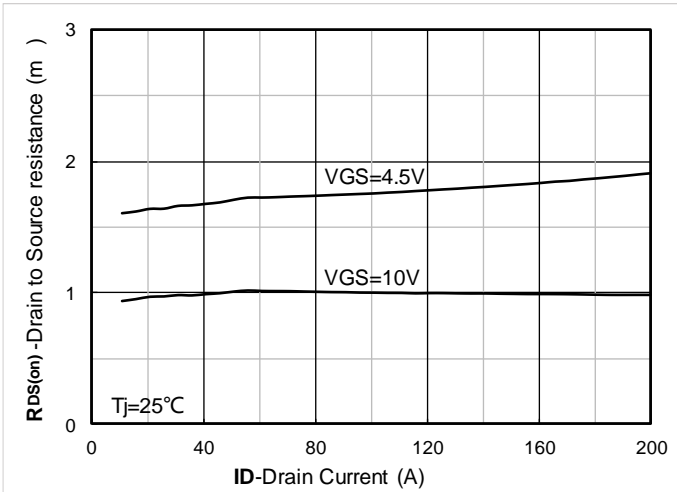


Figure 7. $R_{DS(on)}$ VS Drain Current

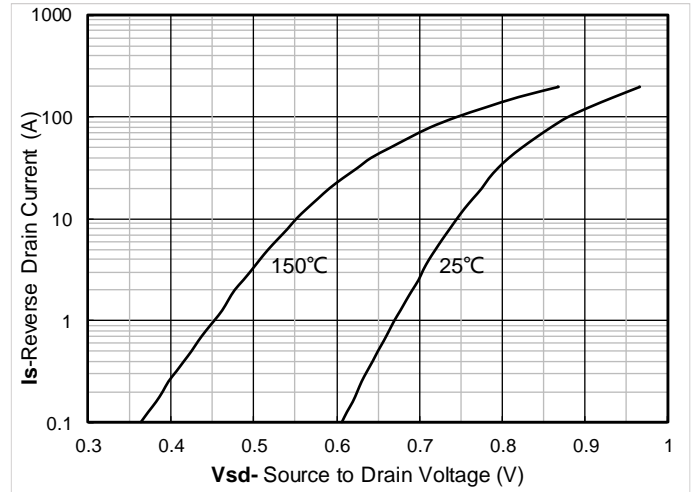


Figure 8. Forward characteristics of reverse diode

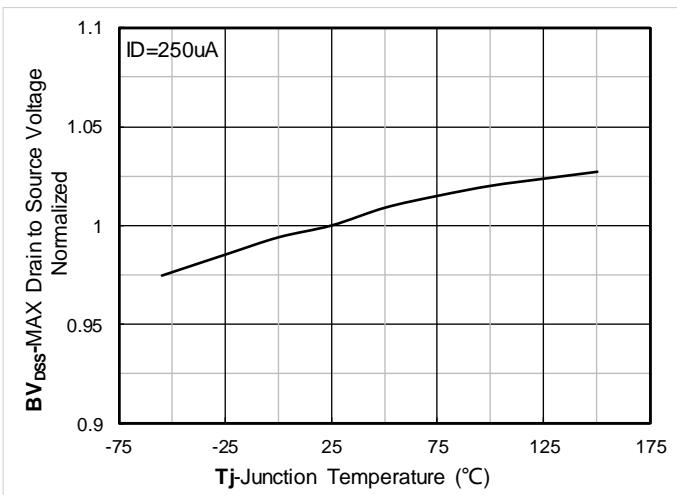


Figure 9. Normalized breakdown voltage

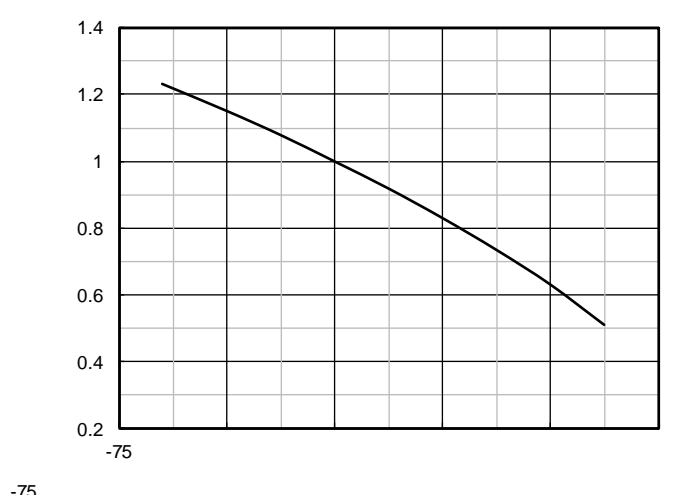


Figure 10. Normalized Threshold voltage

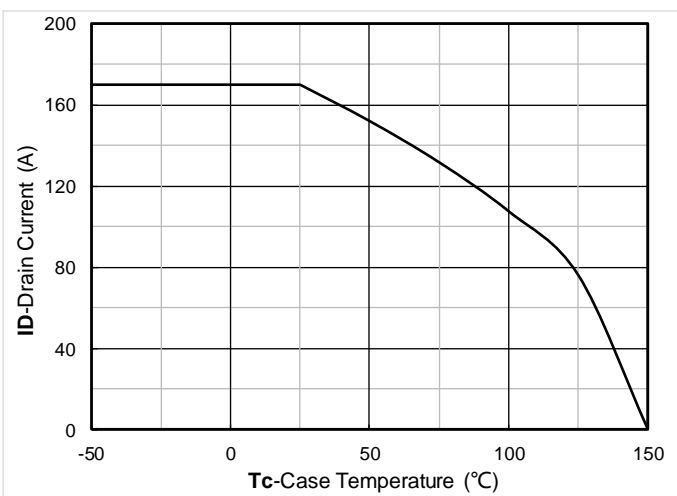


Figure 11. Current dissipation

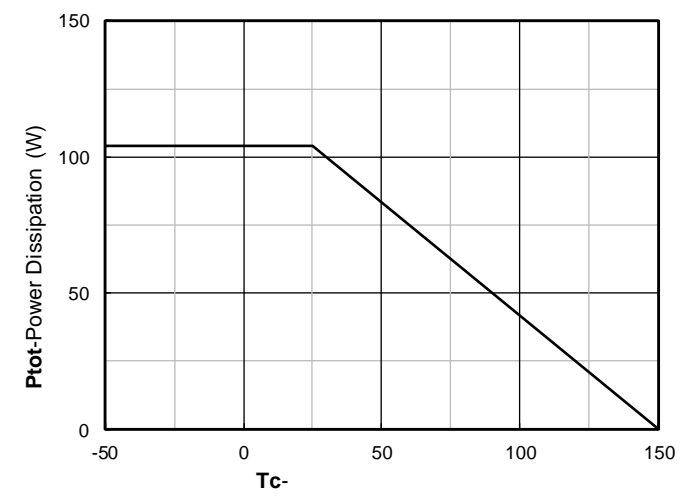


Figure 12. Power dissipation

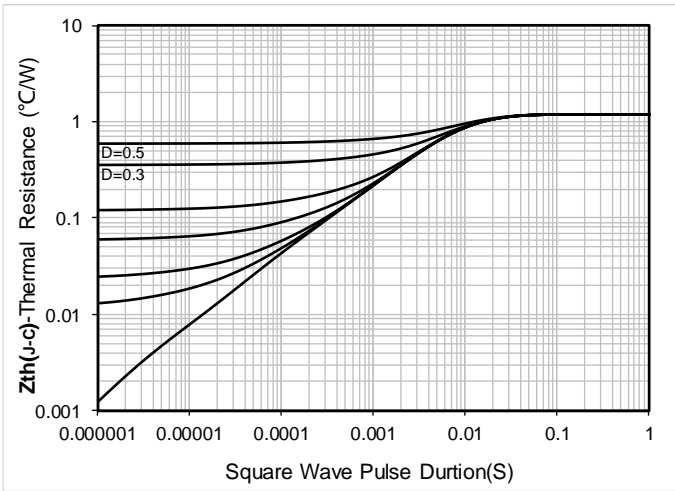


Figure 13. Maximum Transient Thermal Impedance

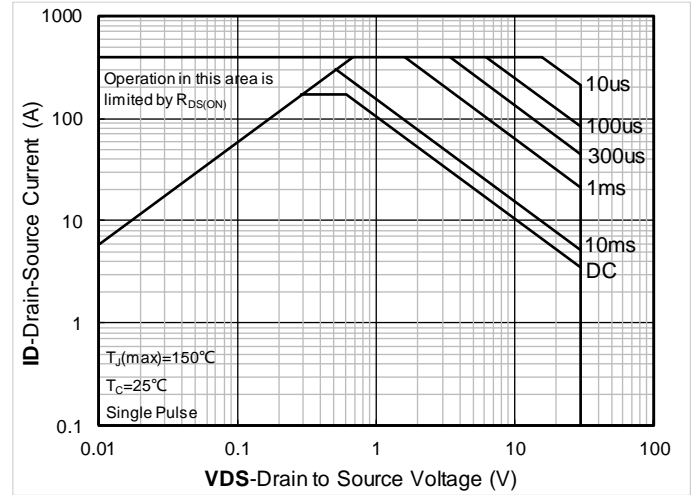


Figure 14. Safe Operation Area

Test Circuits & Waveforms

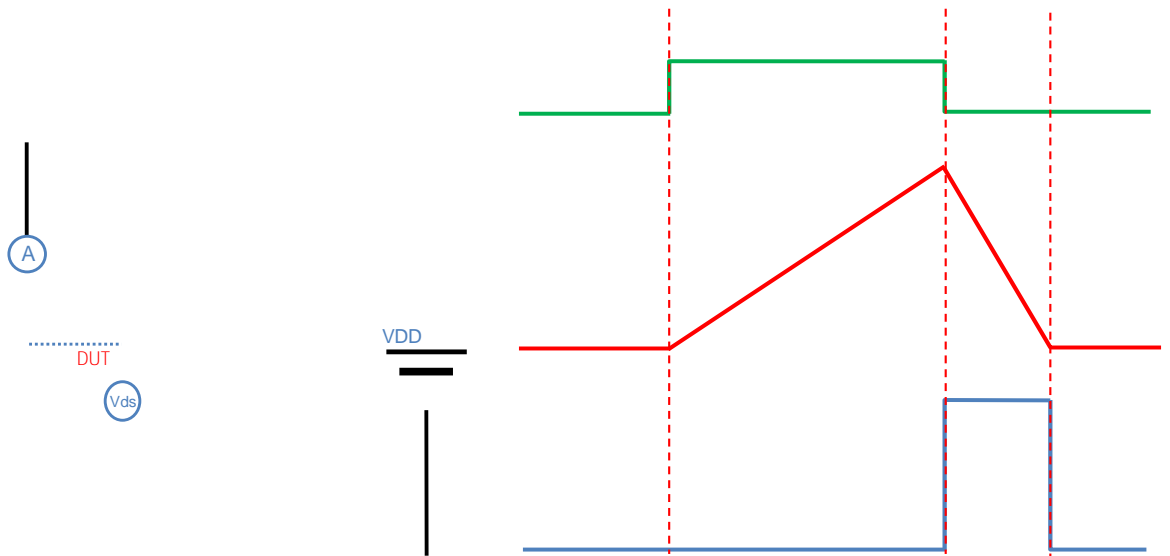


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

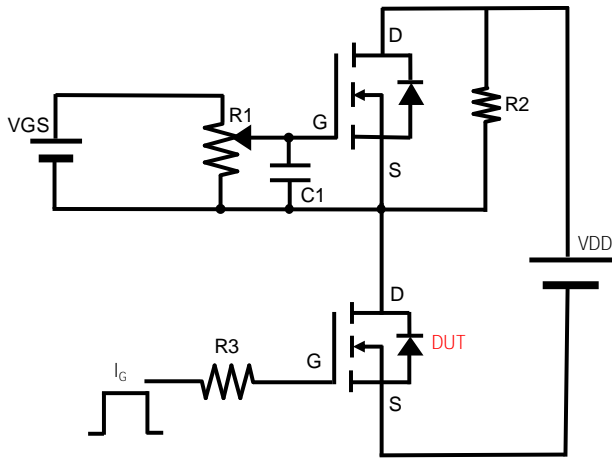


Figure B. Gate Charge Test Circuit & Waveform

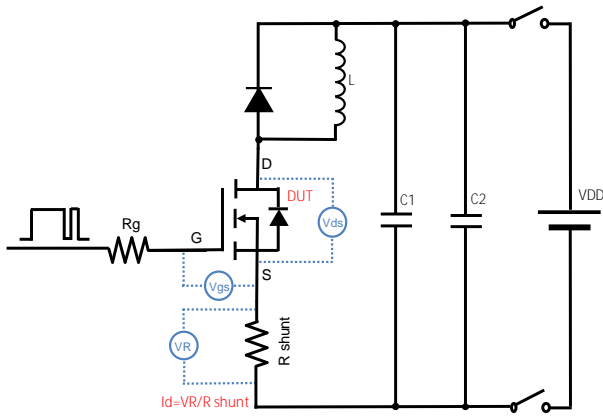


Figure C. Resistive Switching Test Circuit & Waveform

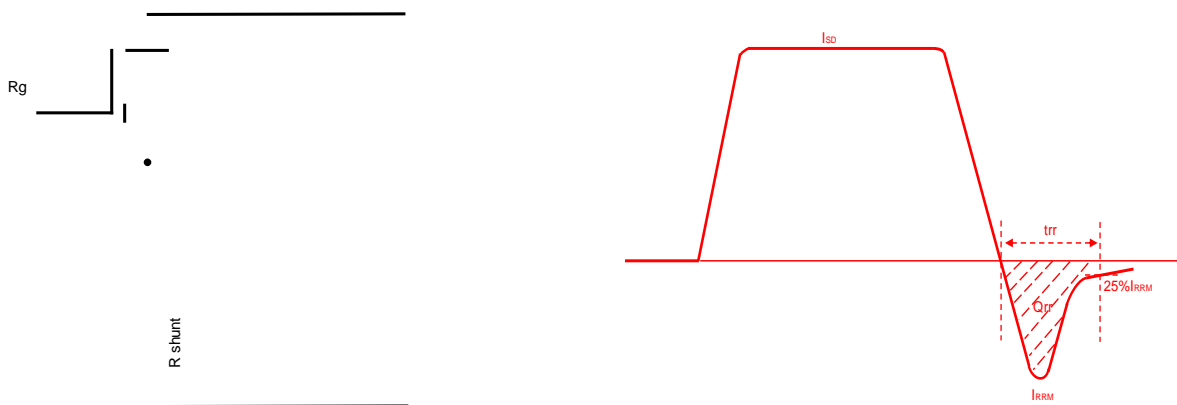
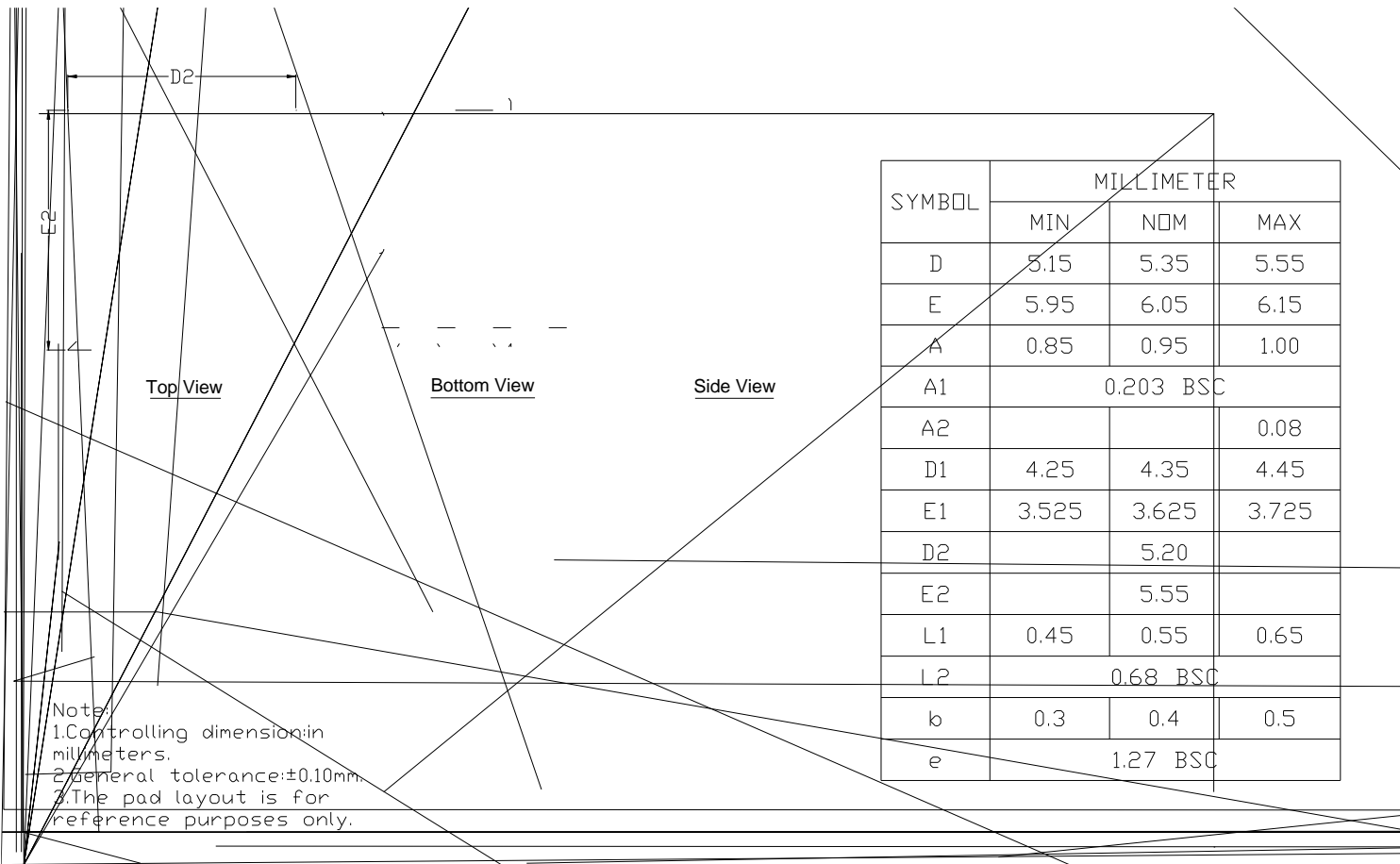


Figure D. Diode Recovery Test Circuit & Waveform



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PDFN5060-8L-D-0.95MM Package information





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