



N-Channel Enhancement Mode Field Effect Transistor

Product Summary

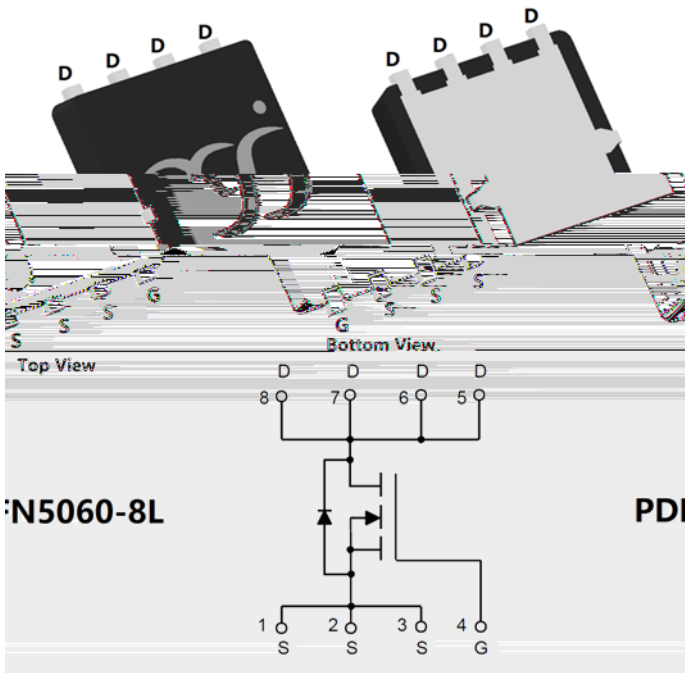
V_{DS}	60V
I_D	175A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	2.25mohm
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	3.0mohm
100% EAS Tested	
100% V_{DS} Tested	

General Description

Split gate trench MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Moisture Sensitivity Level 3
Epoxy Meets UL 94 V-0 Flammability Rating
HalogenFree

Applications

Power switching application
Uninterruptible power supply
PD charge
DC-DC convertor

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_c=25$	I_D	175	A
	$T_c=100$		110	
Pulsed Drain Current ^A		I_{DM}	700	A
Avalanche energy ^B		EAS	992	mJ
Total Power Dissipation ^C	$T_c=25$	P_D	140	W
	$T_c=100$		55	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	R_{JA}	38	46	/W
Thermal Resistance Junction-to-Case	Steady-State	R_{JC}	0.75	0.9	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG175G06AR	F1	G175G06AR	5000	10000	100000	13" reel

Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
		$V_{DS}=60V, V_{GS}=0V, T_J=150^\circ C$	-	-	100	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.65	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=87.5A$	-	1.8	2.25	m
		$V_{GS}=10V, I_D=20A$	-	1.8	2.25	
		$V_{GS}=4.5V, I_D=20A$	-	2.4	3.0	
Diode Forward Voltage	V_{SD}	$I_S=87.5A, V_{GS}=0V$	-	0.9	1.2	V
Gate resistance	R_G	$f=1MHz, \text{Open drain}$	-	2.2	-	
Maximum Body-Diode Continuous Current	I_S		-	-	175	A
Dynamic Parameters						
Input Capacitance	C_{iss}		-	5250	-	pF
Output Capacitance	C_{oss}	$V_{DS}=30V, V_{GS}=0V, f=1MHz$	-	1085	-	
Reverse Transfer Capacitance	C_{riss}		-	40	-	
Switching Parameters						
Total Gate Charge	Q_g		-	50	-	nC
Gate-Source Charge	Q_{gs}	$V_{GS}=10V, V_{DS}=30V, I_D=87.5A$	-	18	-	
Gate-Drain Charge	Q_{gd}		-	5	-	
Reverse Recovery Charge	Q_{rr}		-	140	-	nC
Reverse Recovery Time	t_{rr}	$I_F=87.5A, di/dt=500A/us$	-	35	-	ns
Turn-on Delay Time	$t_{D(on)}$		-	17	-	nS
Turn-on Rise Time	t_r	$V_{GS}=10V, V_{DD}=30V, I_D=87.5A$ $R_{GEN}=2.2$	-	160	-	
Turn-off Delay Time	$t_{D(off)}$		-	46	-	
Turn-off fall Time	t_f		-	12	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. $T_J=25^\circ C, V_{DD}=50V, V_G=10V, R_G=25, L=2mH, I_{AS}=31.5A$.

C. P_d is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{JA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $150^\circ C$. The value in any given application depends on the user's specific board design.



Typical Electrical and Thermal Characteristics Diagrams

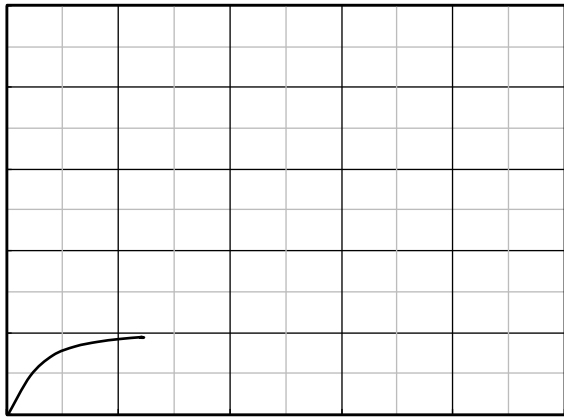


Figure 1. Output Characteristics

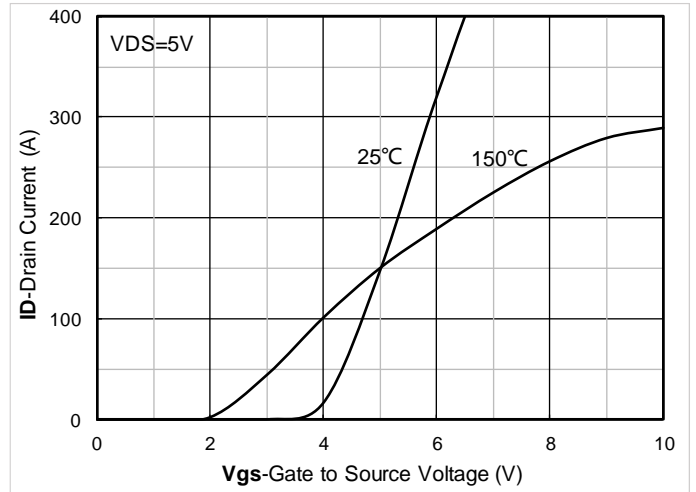


Figure 2. Transfer Characteristics

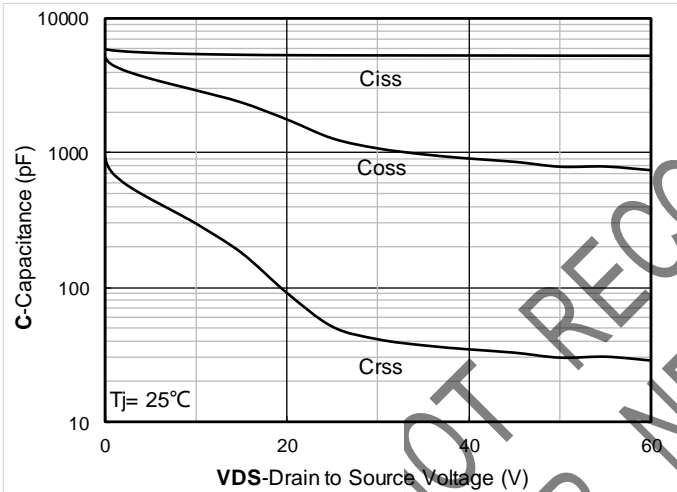


Figure 3. Capacitance Characteristics

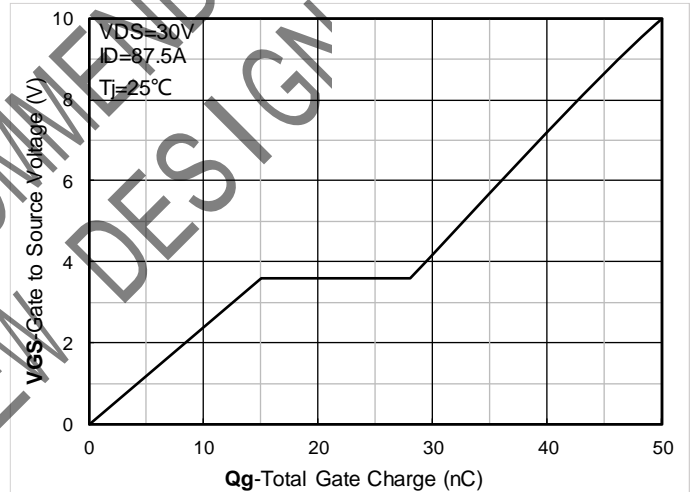


Figure 4. Gate Charge

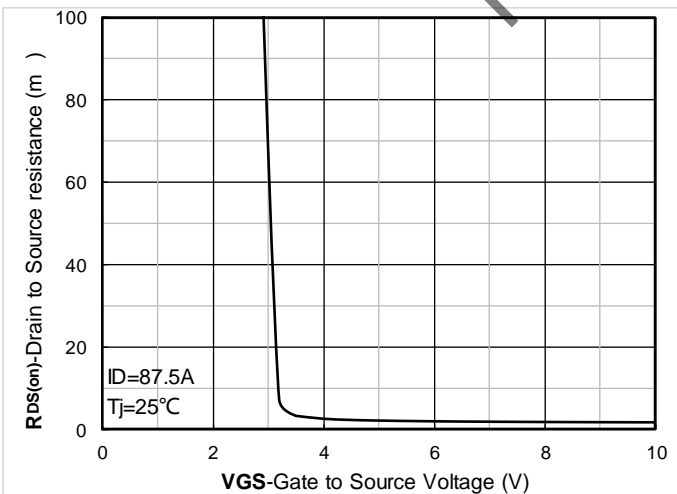


Figure 5. On-Resistance vs Gate to Source Voltage

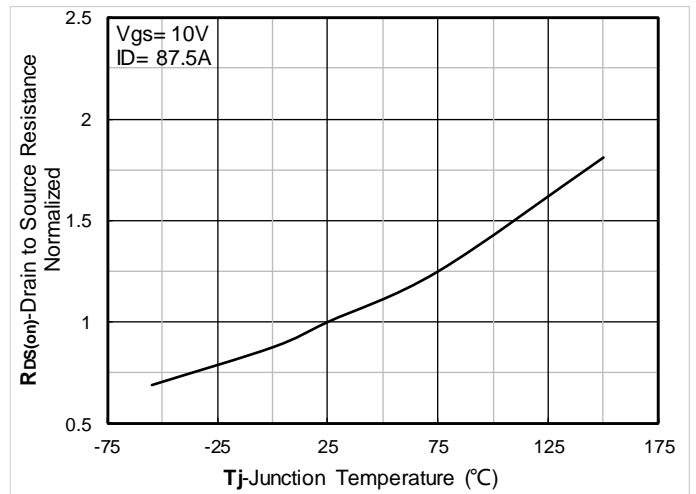


Figure 6. Normalized On-Resistance

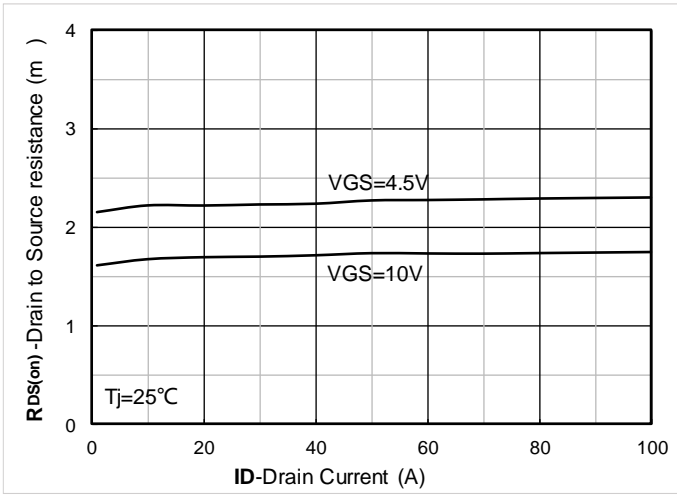


Figure 7. RDS(on) VS Drain Current

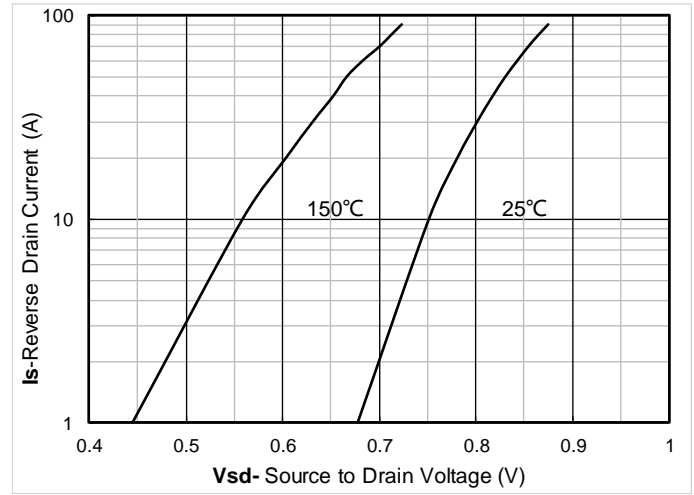


Figure 8. Forward characteristics of reverse diode

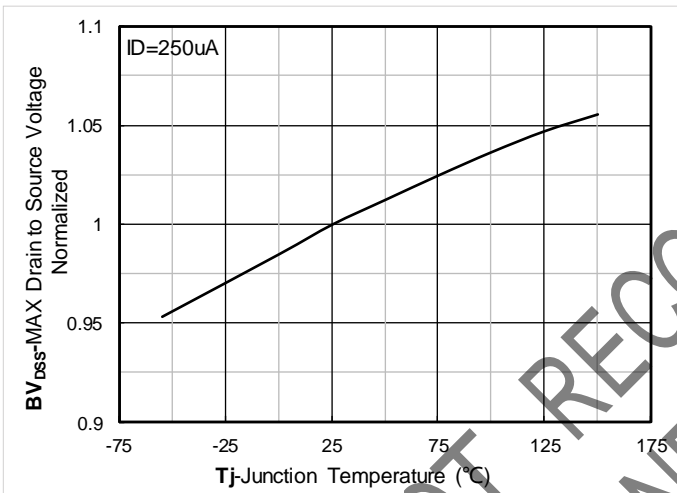


Figure 9. Normalized breakdown voltage

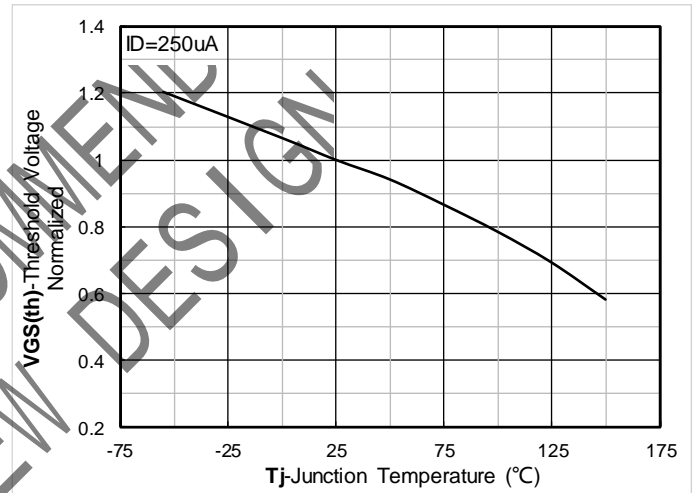


Figure 10. Normalized Threshold voltage

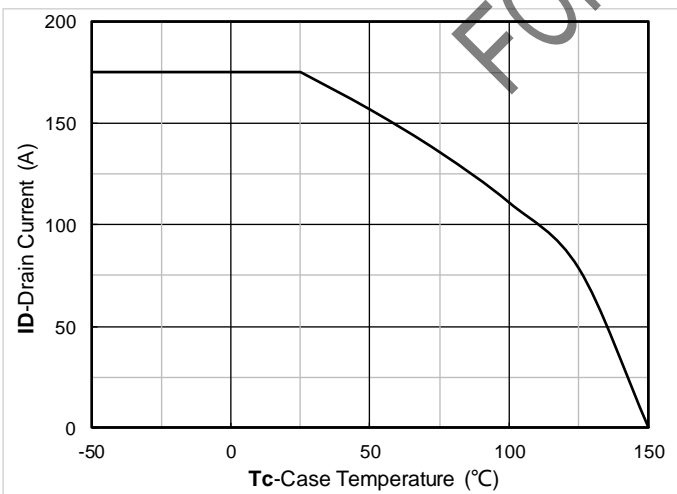


Figure 11. Current dissipation

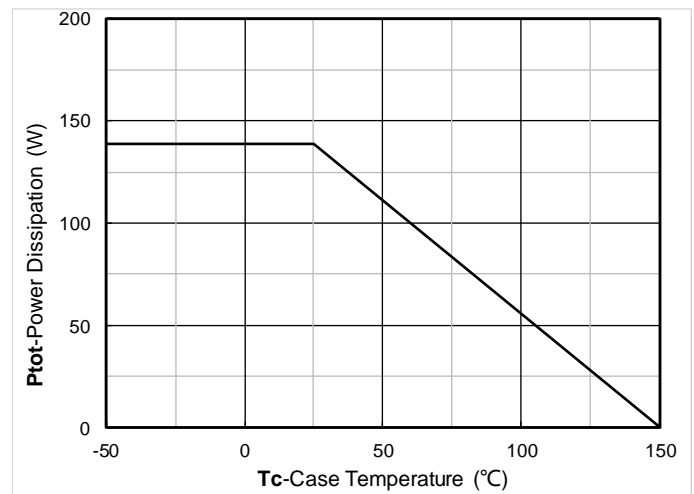


Figure 12. Power dissipation

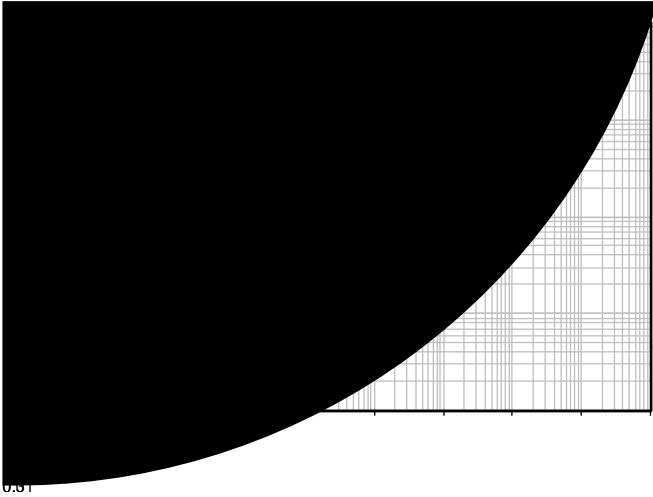


Figure 13. Maximum Transient Thermal Impedance

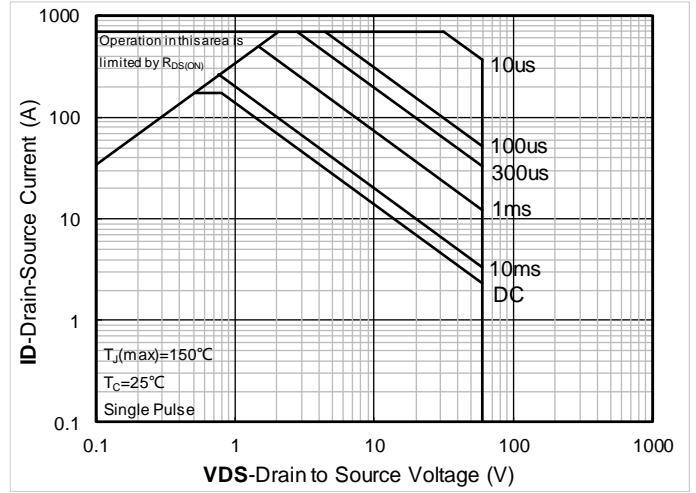


Figure 14. Safe Operation Area

Test Circuits & Waveforms

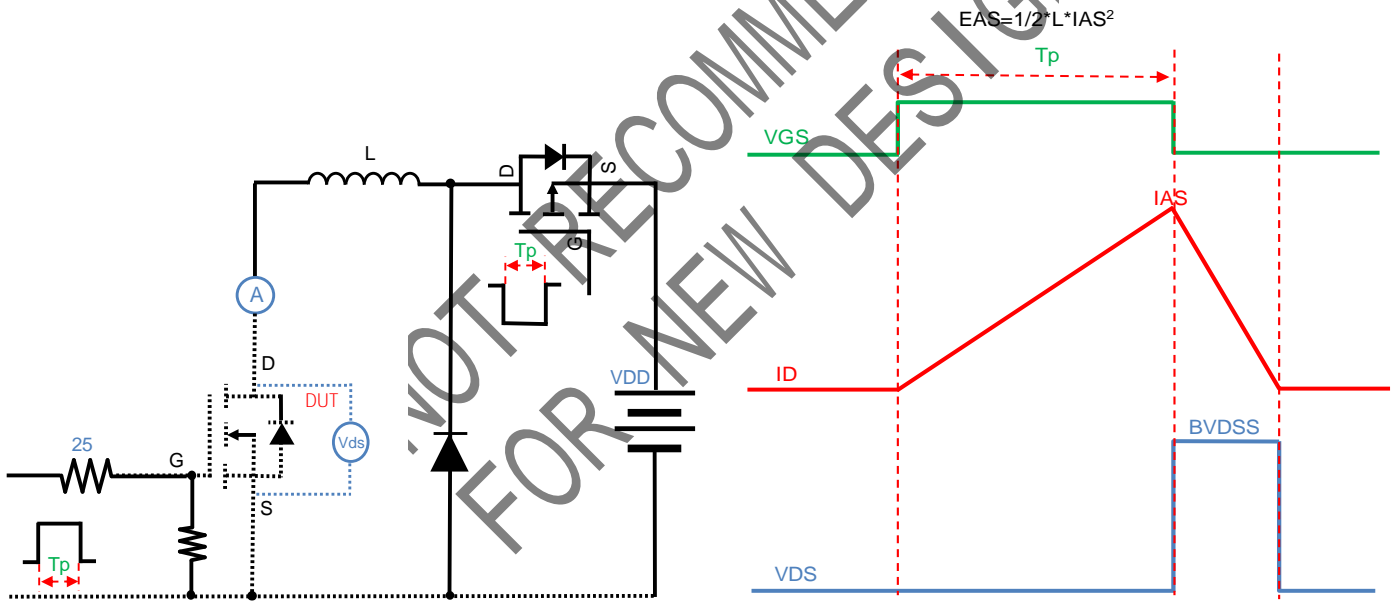


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

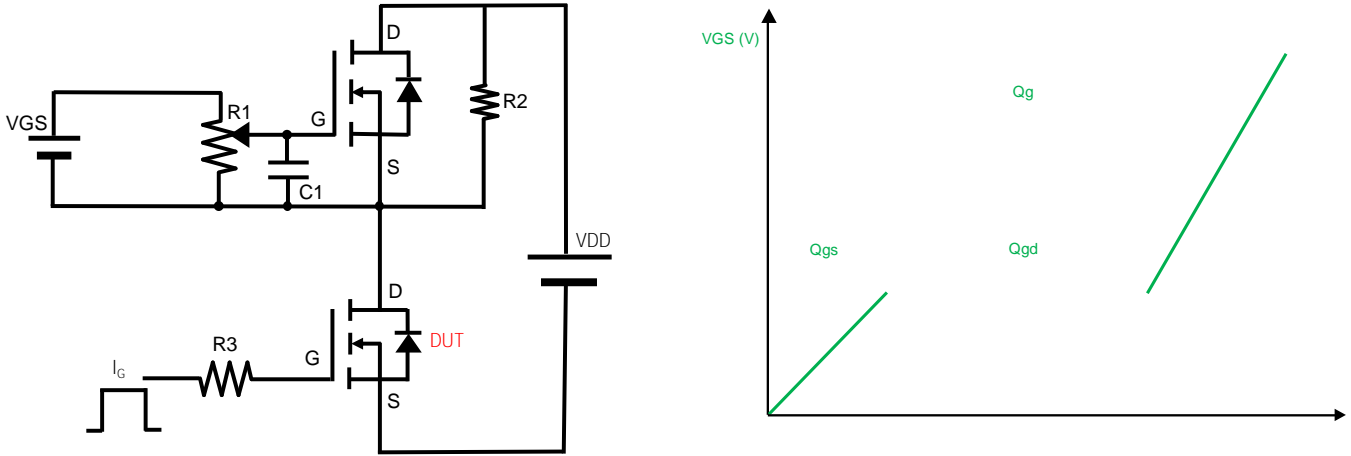


Figure B. Gate Charge Test Circuit & Waveform

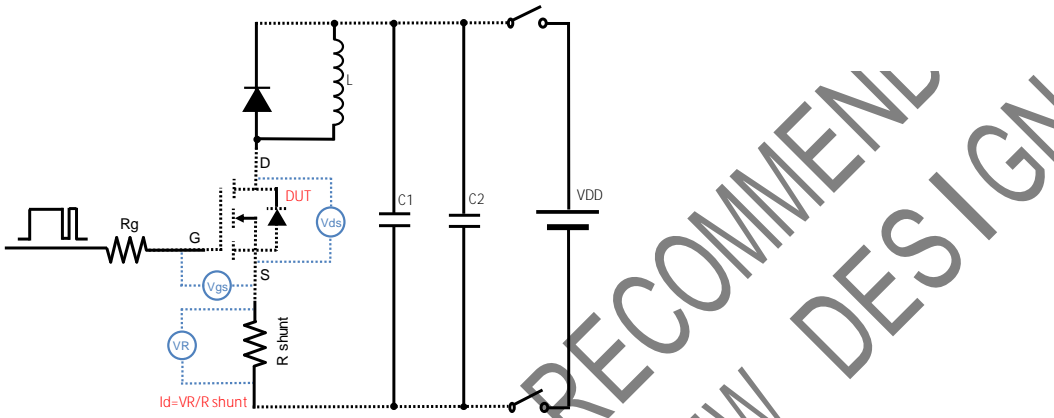


Figure C. Resistive Switching Test Circuit & Waveform

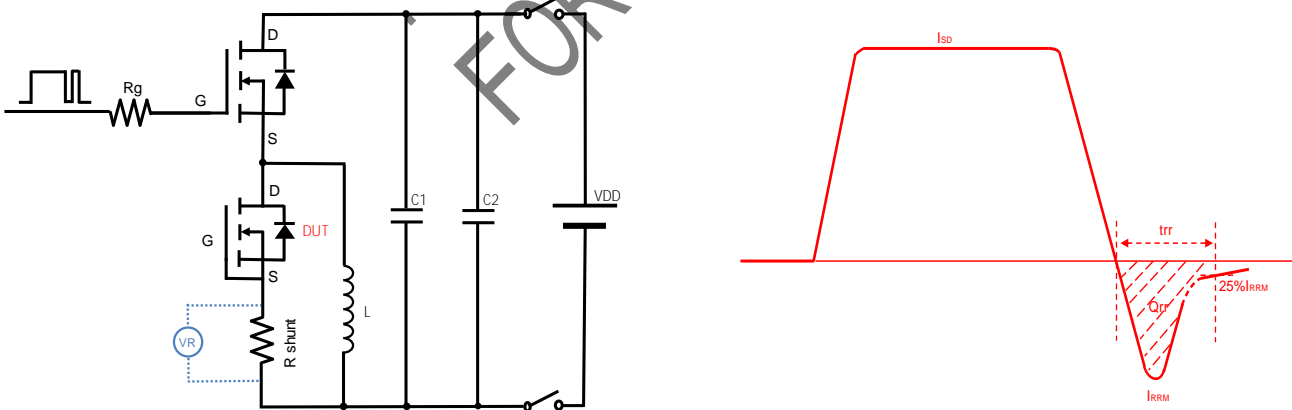


Figure D. Diode Recovery Test Circuit & Waveform

RECOMMEND
YJG210G06AR
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