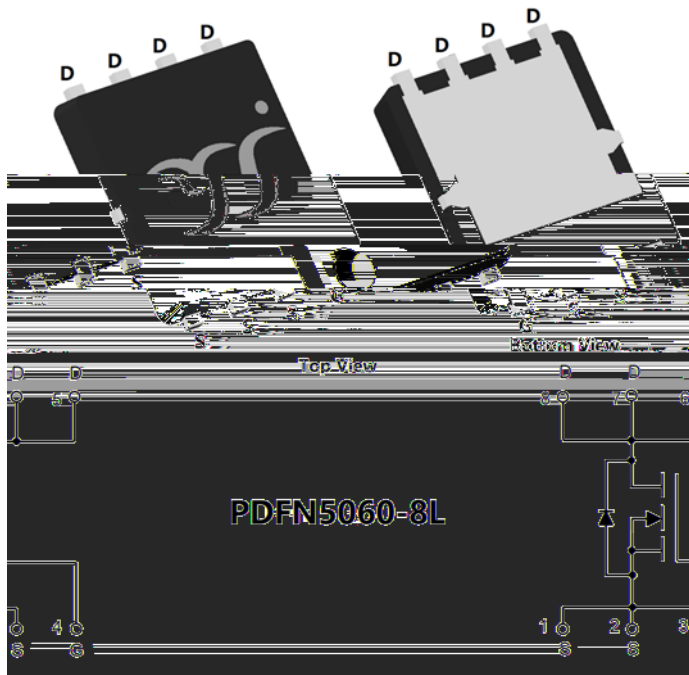




N-Channel Enhancement Mode Field Effect Transistor



Product Summary

V_{DS}	40V
I_D	180A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	1.8m
$R_{DS(ON)}$ (at $V_{GS}=6V$)	3.2m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Split gate trench MOSFET technology
 Excellent package for heat dissipation
 High density cell design for low $R_{DS(ON)}$
 Moisture Sensitivity Level 3
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

Power switching application
 Uninterruptible power supply
 DC-DC converter

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	30	A
	$T_A=100^\circ\text{C}$		21	
	$T_C=25^\circ\text{C}$		180	
	$T_C=100^\circ\text{C}$		127	
Pulsed Drain Current ^A		I_{DM}	720	A
Avalanche energy ^B		EAS	426	mJ
Total Power Dissipation ^C	$T_A=25^\circ\text{C}$	P_D	3.3	W
	$T_A=100^\circ\text{C}$		1.6	
	$T_C=25^\circ\text{C}$		125	
	$T_C=100^\circ\text{C}$		62	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +175	$^\circ\text{C}$

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	R_{JA}	35	45	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Case	Steady-State	R_{JC}	1	1.2	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG180G04HR	F1	G180G04HR	5000	10000	100000	13" reel



YJG180G04HR

Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
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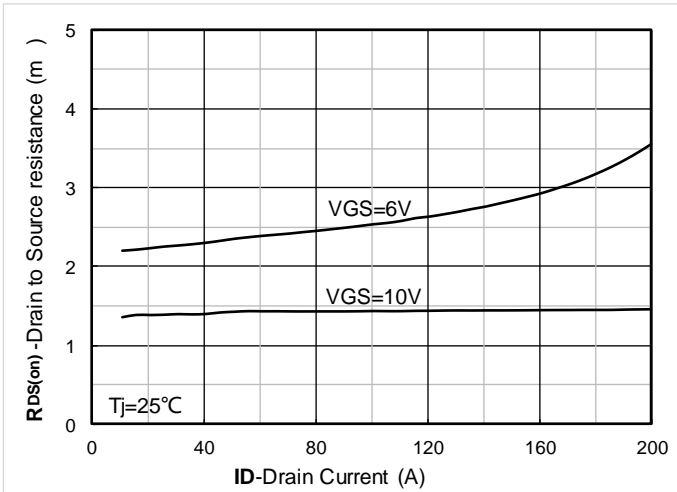


Figure 7. $R_{DS(on)}$ VS Drain Current

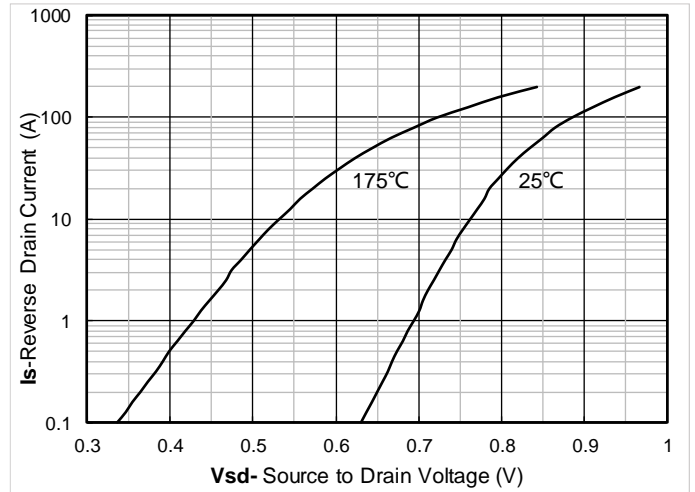


Figure 8. Forward characteristics of reverse diode

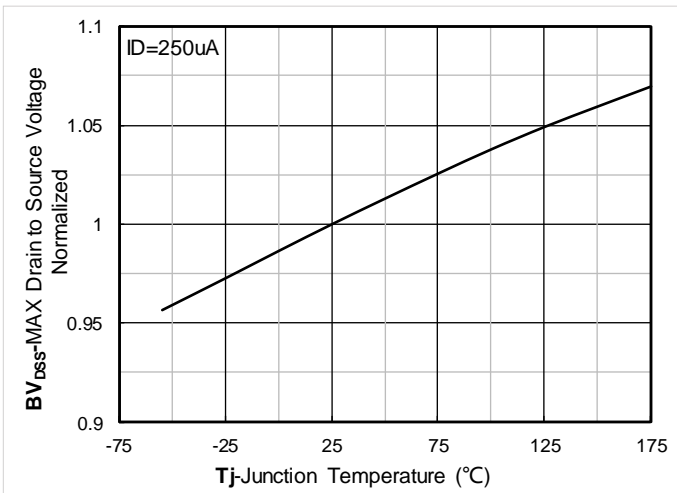


Figure 9. Normalized breakdown voltage

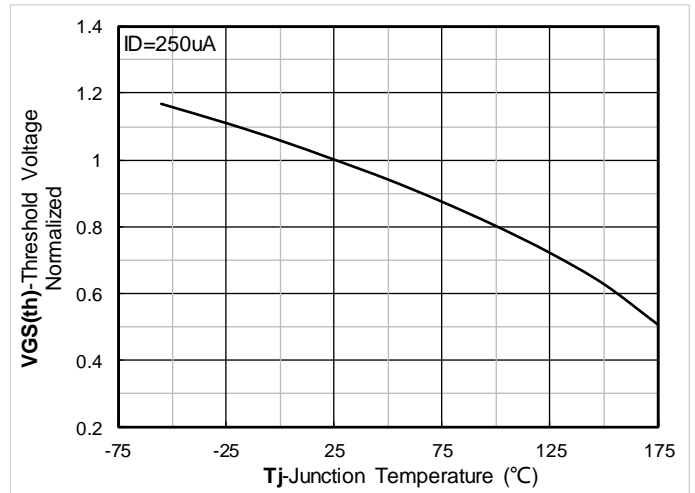


Figure 10. Normalized Threshold voltage

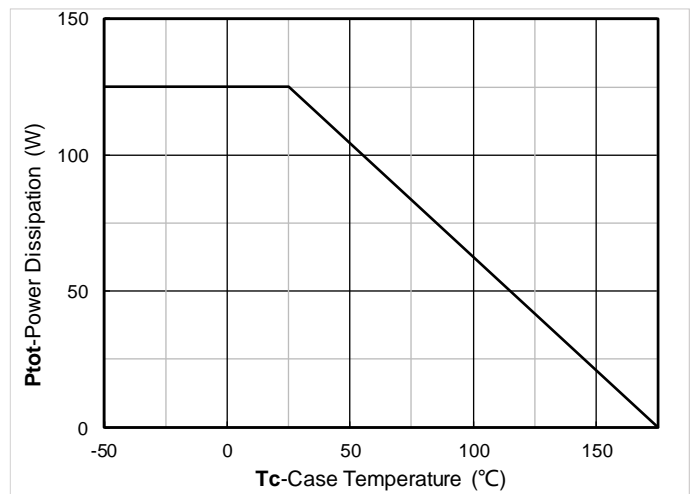


Figure 12. Power dissipation

Figure 11. Current dissipation



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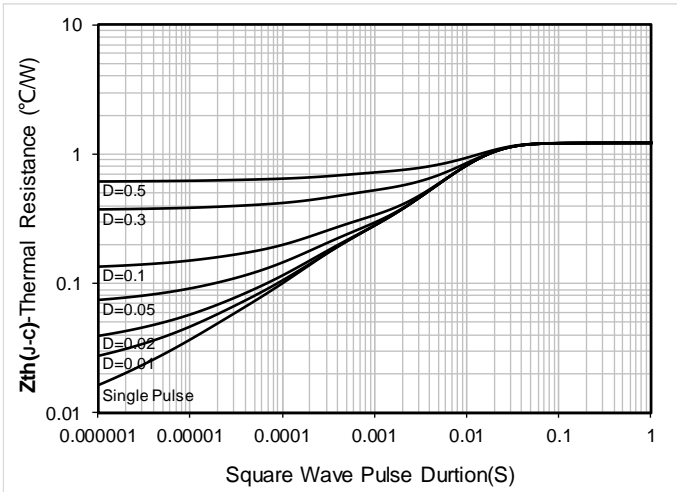


Figure 13. Maximum Transient Thermal Impedance

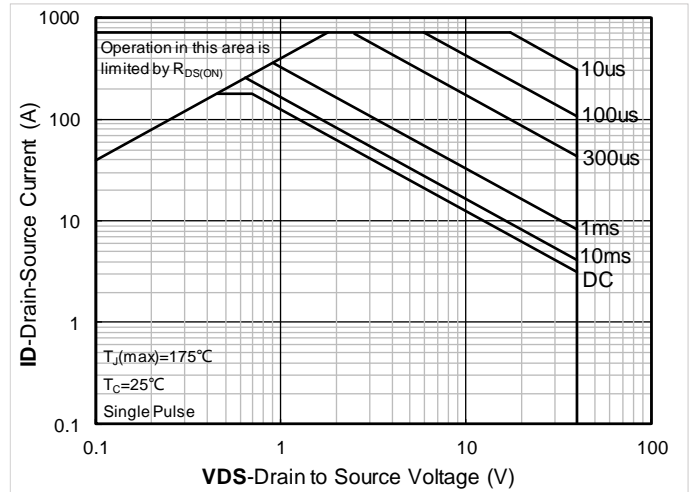


Figure 14. Safe Operation Area

Test Circuits & Waveforms

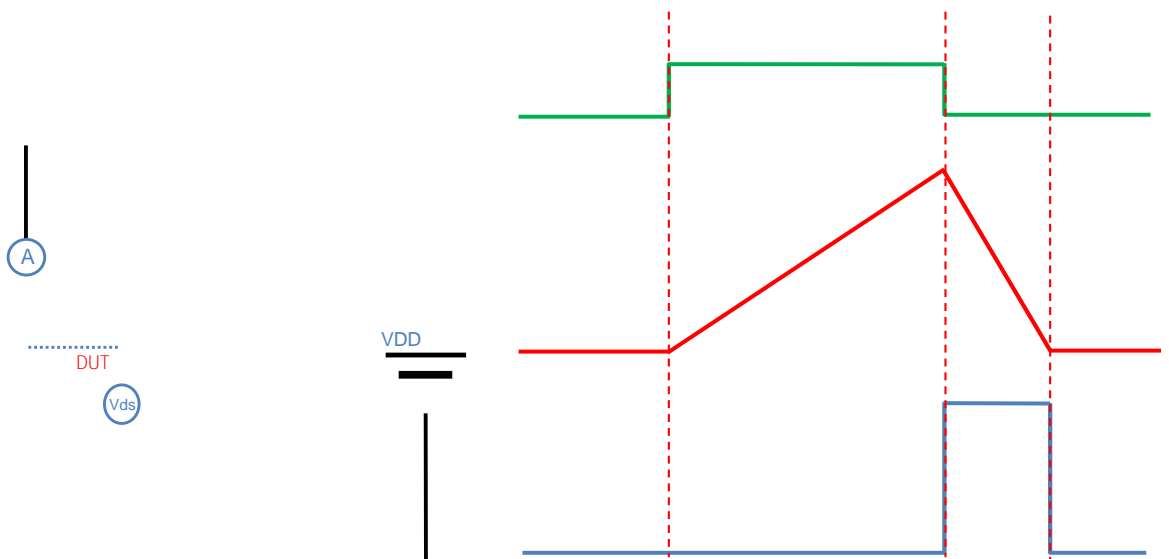


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

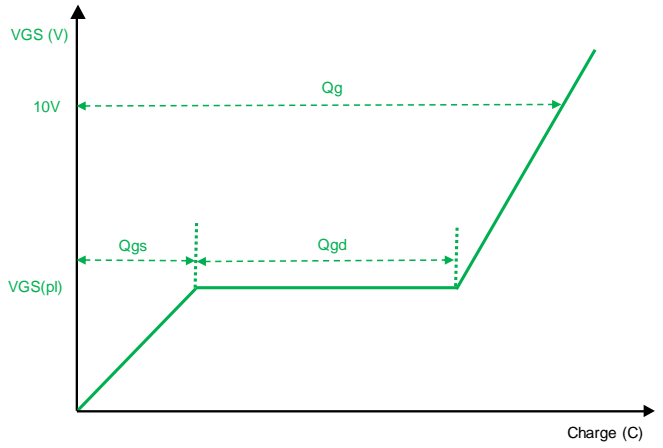
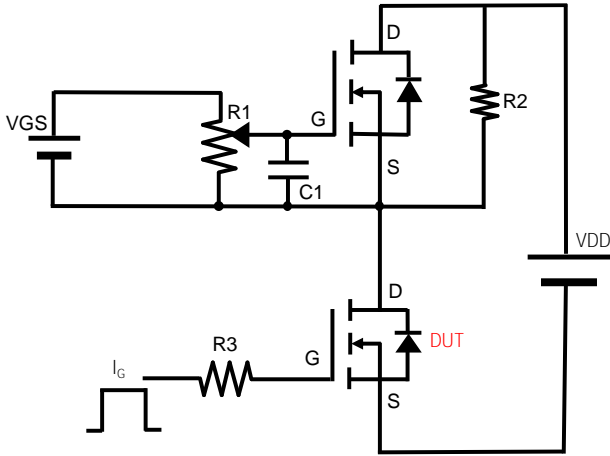


Figure B. Gate Charge Test Circuit & Waveform

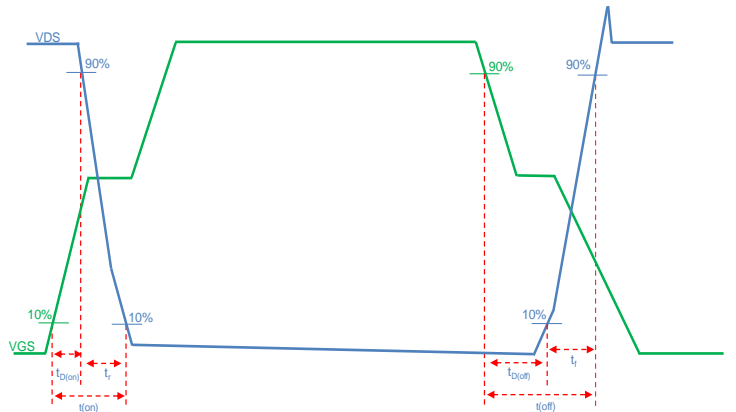
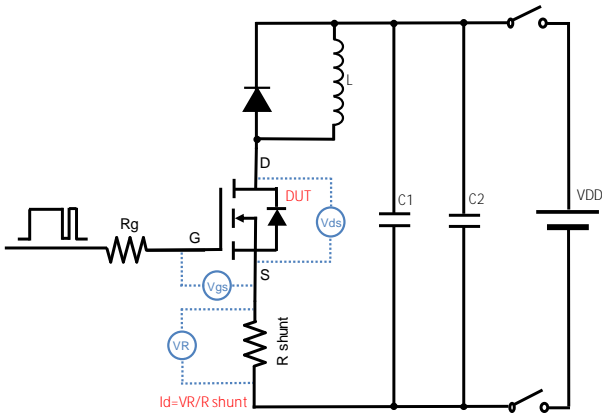


Figure C. Resistive Switching Test Circuit & Waveform

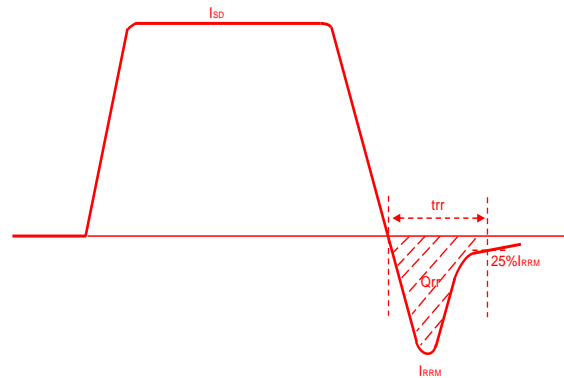
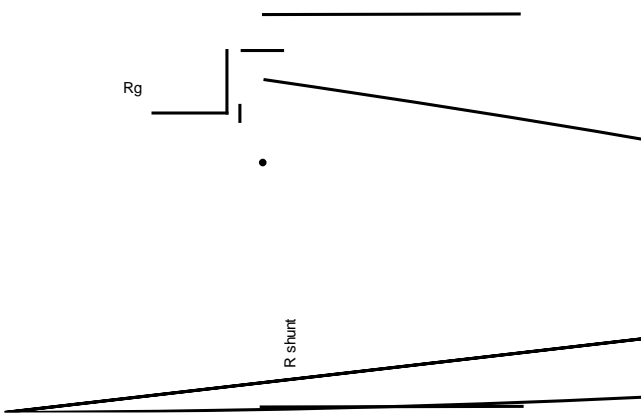
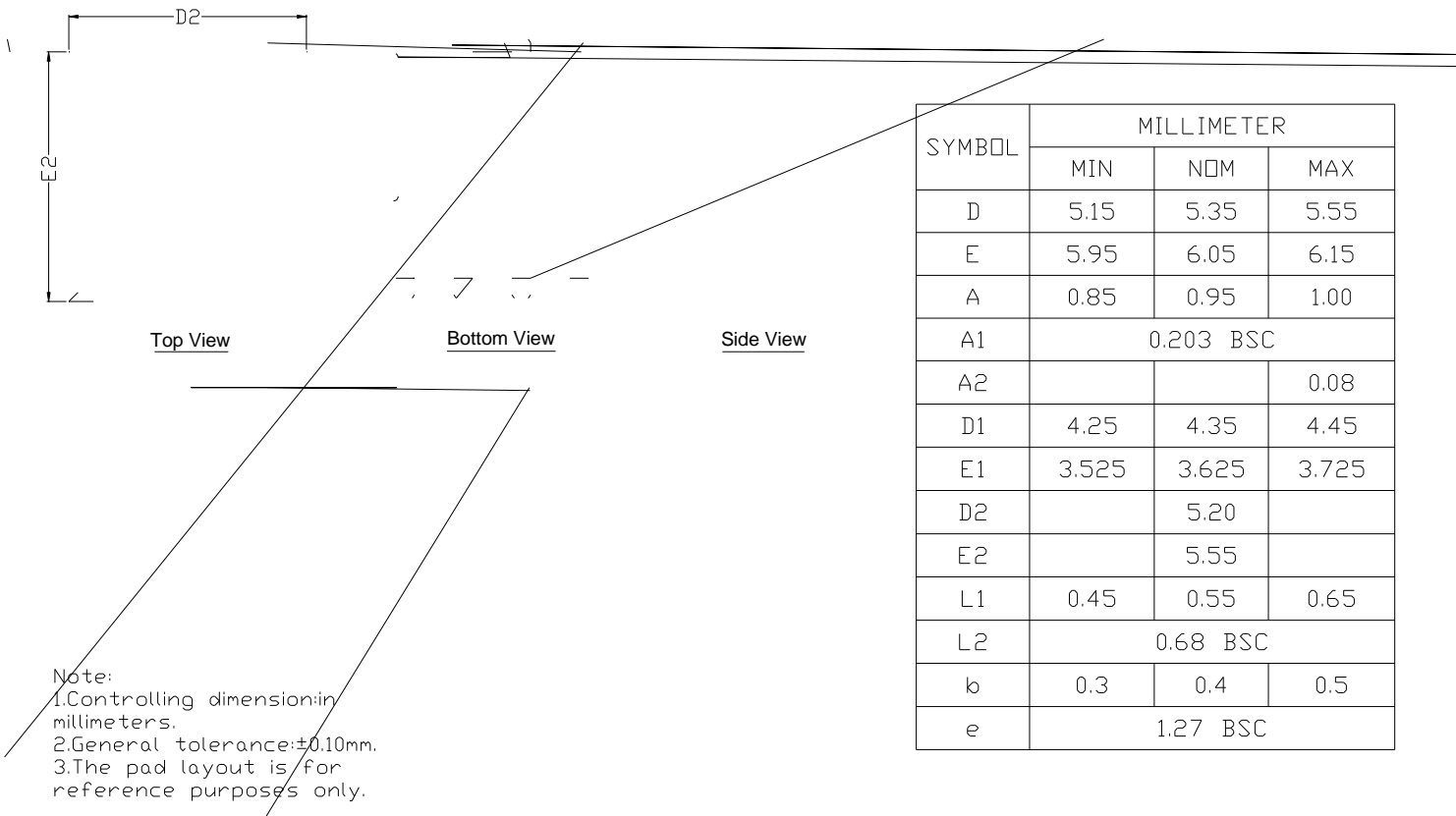


Figure D. Diode Recovery Test Circuit & Waveform



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PDFN5060-8L-D-0.95MM Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.05	6.15
A	0.85	0.95	1.00
A1	0.203 BSC		
A2			0.08
D1	4.25	4.35	4.45
E1	3.525	3.625	3.725
D2		5.20	
E2		5.55	
L1	0.45	0.55	0.65
L2	0.68 BSC		
b	0.3	0.4	0.5
e	1.27 BSC		



YJG180G04HR

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