



# YJG18N10A

## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

DS JTJETQq295.08 656.35 266.5 92.904 r

DS ON( )-10as=10M0605I( )-10( )15( )15( )605I15( )605I( )-10

00% EAS estd

00% ds estd

### General Descripio

MV( )-10MO FET( )-10tchology

xcellent ackage( )15f reat JTJETQq295.08 574.73 266.5 81.62

gh( )15densitl --10design( --10f )-10or( 60I)--4(o)3(w)380( --10F

ist re( --10S)9(e)30(n)3(si)11(t)--10ivit( --10L)3(e)30(ve)30(I)--4

poxyl( )-10Me L( )1594( --10F)JTJETQq295.08750478(2)658C

logen ee

### pplicatios

DC DC overtrs

ower( 60m)-8(a)30agesent JTJETQq295.08 493.34 266.5 81.38

Backlightng

bs 60olute( )4(M)29(a)-8(x)-8(i)-4(m)19(u)--8(m)19(( )4(R)5(a)-8(t)70i)17(ng)5(s)13(5)JTJETQ EMC /P #CID 5

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Drain-source Volage 5JTJETQ EMC Qq287.88 438.36 103.25 19.704 r

	gs	20 JTJETQ EMC
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Drain Current 5JTJETQQ EMC q15



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## Electrical Characteristics ( $T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250$	100			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$			1	



Typical Performance Characteristics

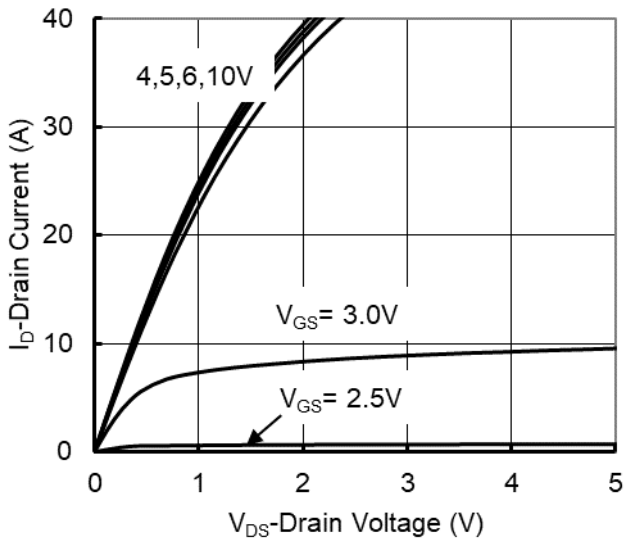


Figure 1. Output Characteristics

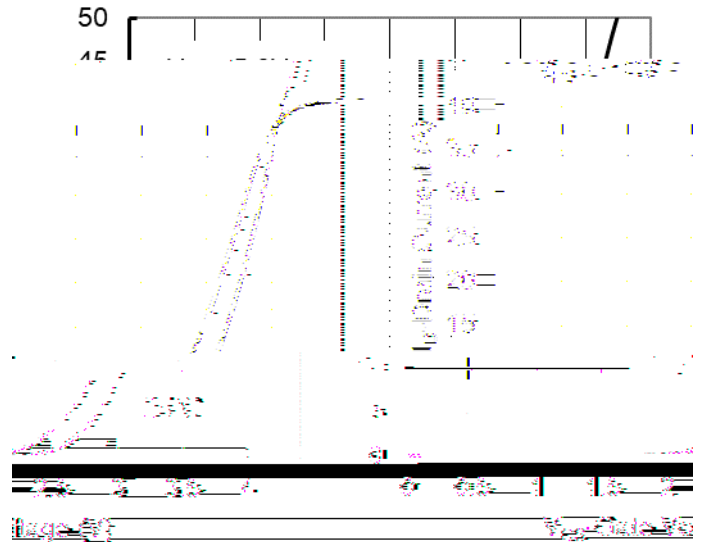


Figure 2. Transfer Characteristics

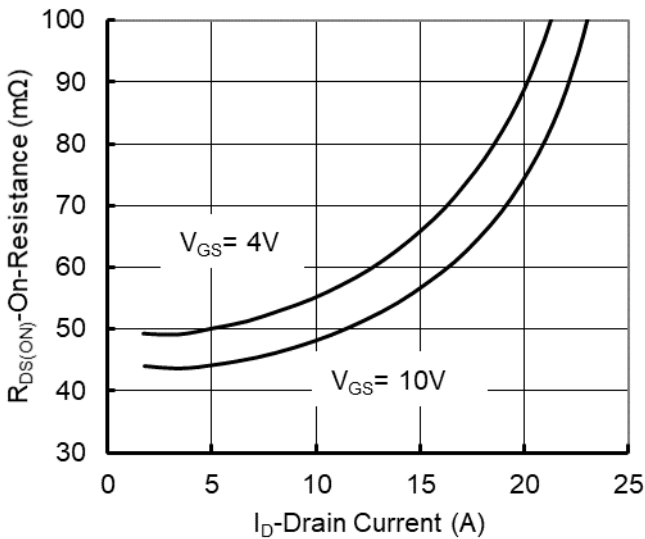


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

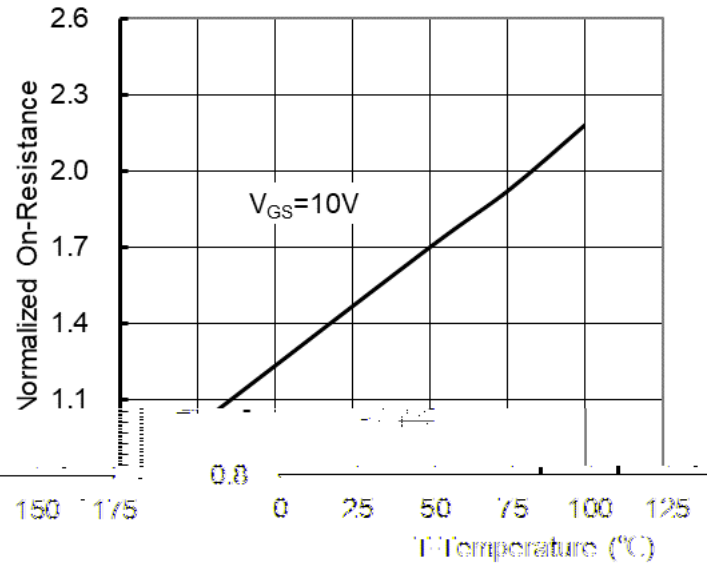


Figure 4. On-Resistance vs. Junction Temperature

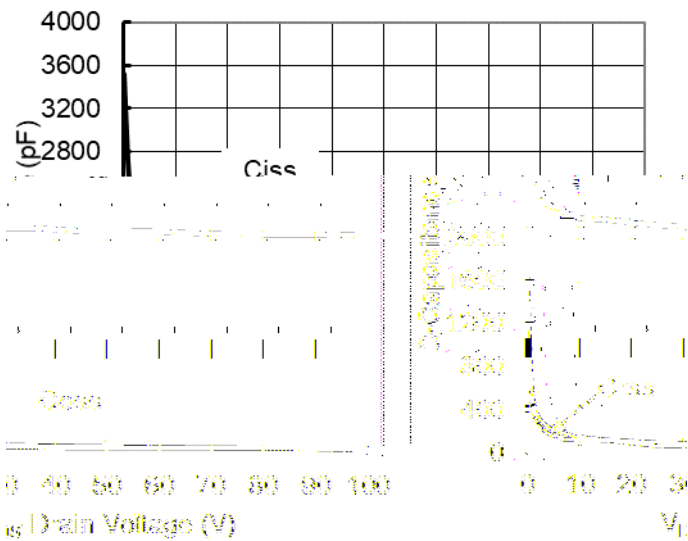


Figure 5. Capacitance Characteristics

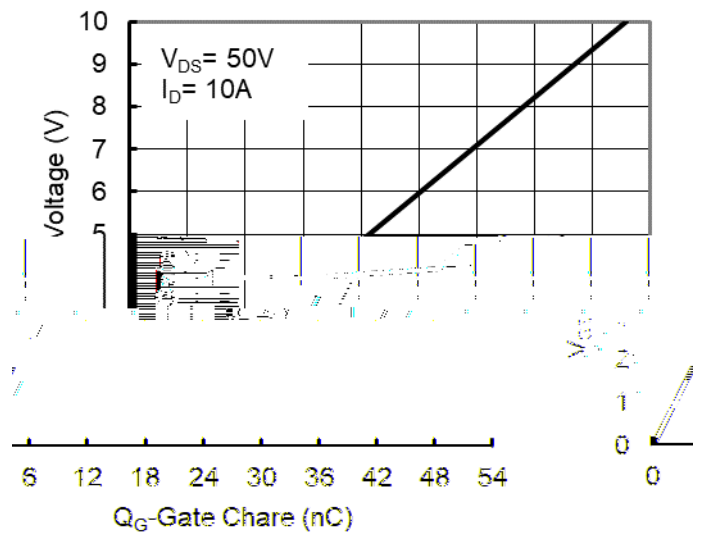


Figure 6. Gate Charge



# YJG18N10A

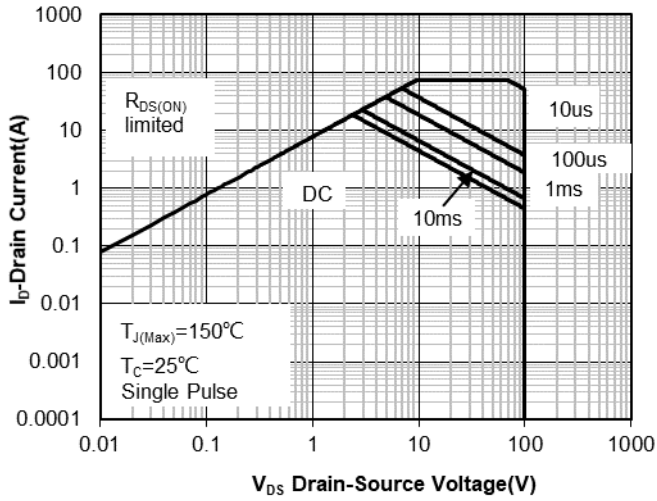


Figure 7. Safe Operation Area

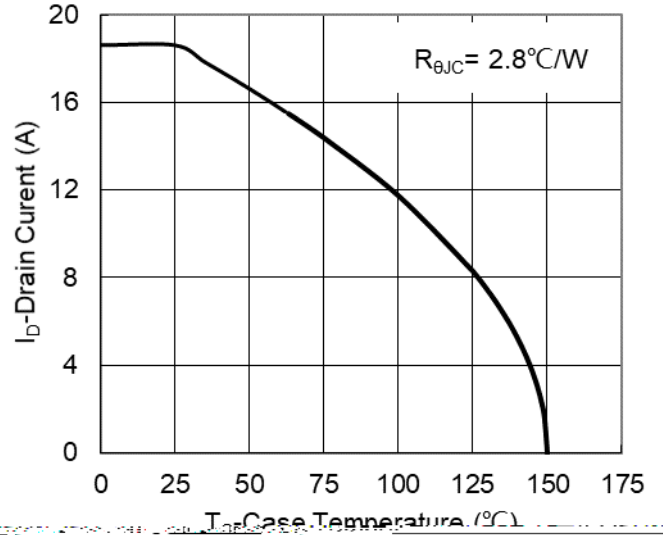


Figure 8. Maximum Continuous Drain Current vs Case Temperature

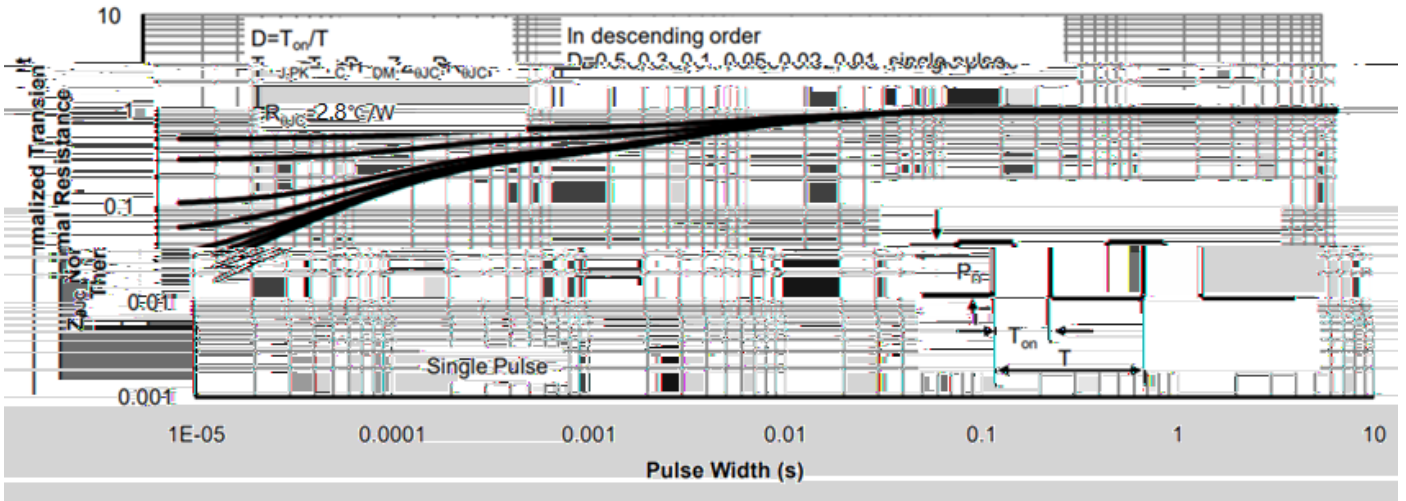
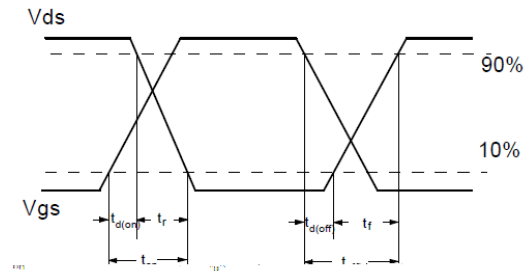
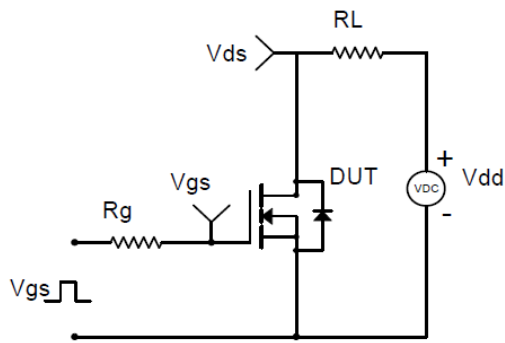
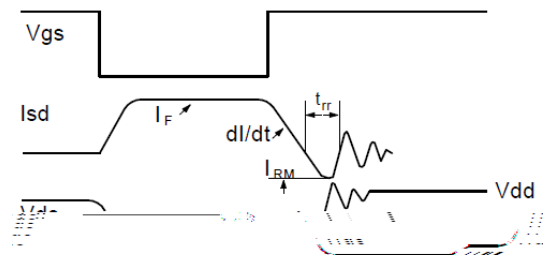
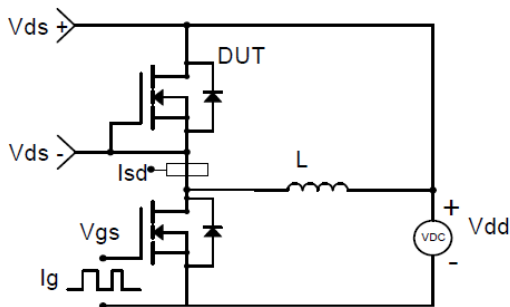


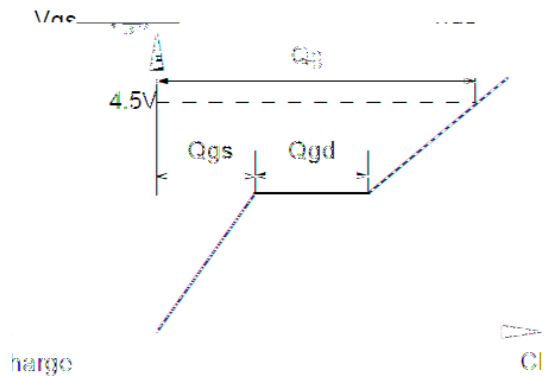
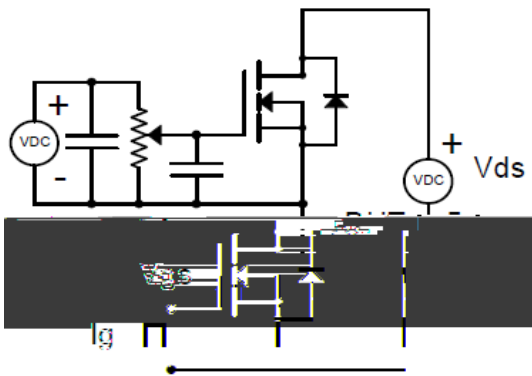
Figure 9. Normalized Maximum Transient Thermal Impedance



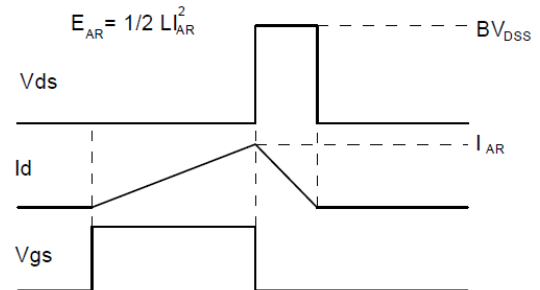
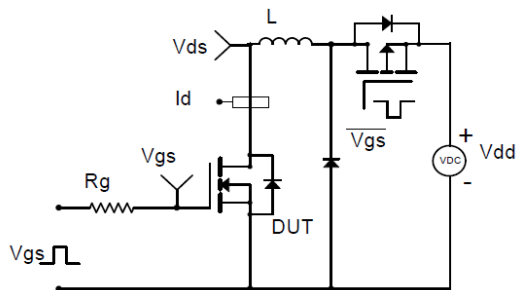
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

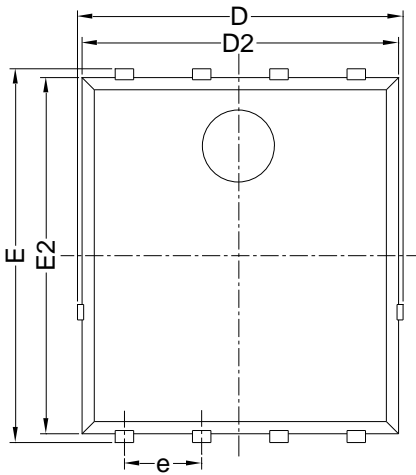


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

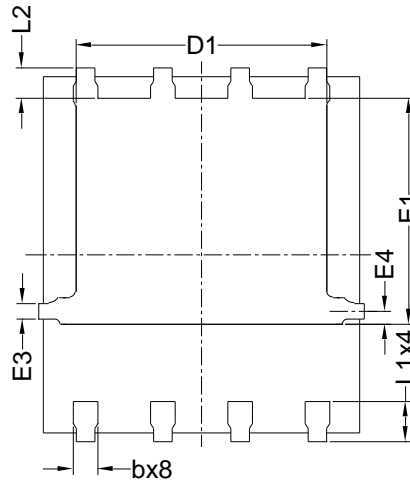


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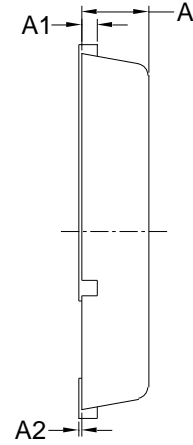
## PDFN5060-8L-B-1.1MM Package Information



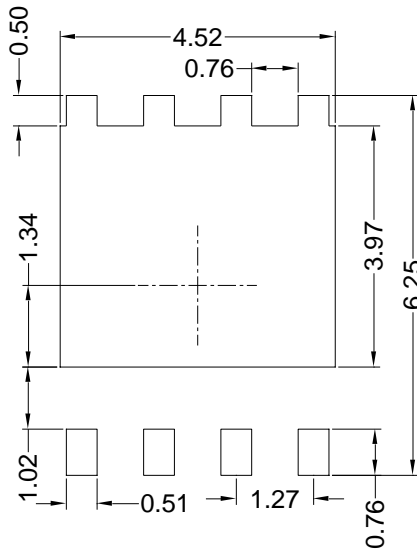
Top View



Bottom View



Side View



Suggested Solder Pad Layout  
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.

