



## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	60V
$I_D$	220A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	1.6m
$R_{DS(ON)}$ ( at $V_{GS}=4.5V$ )	2.4m
100% EAS Tested	
100% $V_{DS}$ Tested	

### General Description

Split gate trench MOSFET technology  
Excellent package for heat dissipation  
High density cell design for low  $R_{DS(ON)}$   
Moisture Sensitivity Level 3  
Epoxy Meets UL 94 V-0 Flammability Rating  
Halogen Free

### Applications

Power switching application  
Uninterruptible power supply  
DC-DC convertor

### Absolute Maximum Ratings ( $T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	60	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ C$	$I_D$	27	A
	$T_A=100^\circ C$		17	
	$T_C=25^\circ C$		220	
	$T_C=100^\circ C$		139	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	800	A
Avalanche energy <sup>B</sup>		EAS	676	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ C$	$P_D$	2.5	W
	$T_A=100^\circ C$		1	
	$T_C=25^\circ C$		147	
	$T_C=100^\circ C$		58	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 +150	$^\circ C$

### Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State	$R_{JA}$	40	50	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{JC}$	0.7	0.85	

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG220G06AR	F1	G220G06AR	5000	10000	100000	13" reel



# YJG220G06AR

RECOMMEND  
**YJG210G06AR**  
FOR NEW DESIGN

## Electrical Characteristics ( $T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V



Typical Electrical and Thermal Characteristics Diagrams

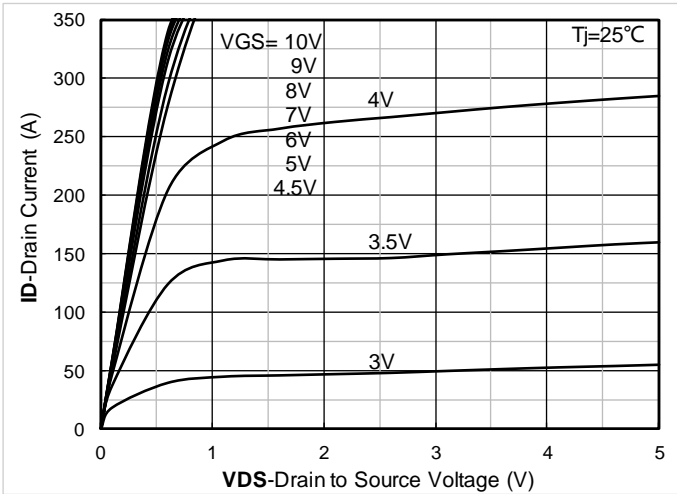


Figure 1. Output Characteristics

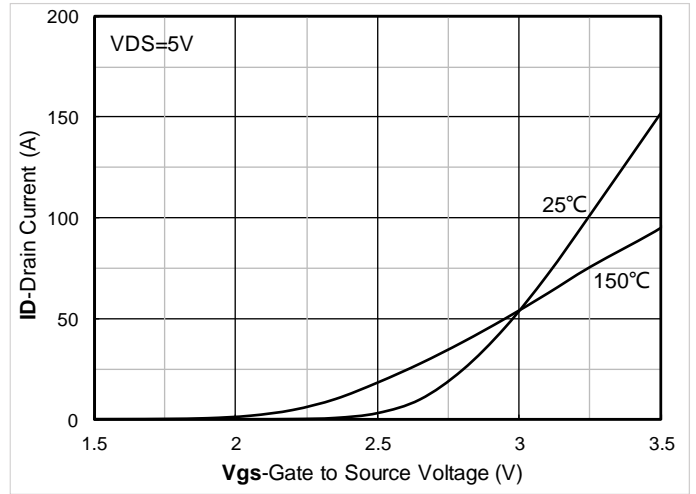


Figure 2. Transfer Characteristics

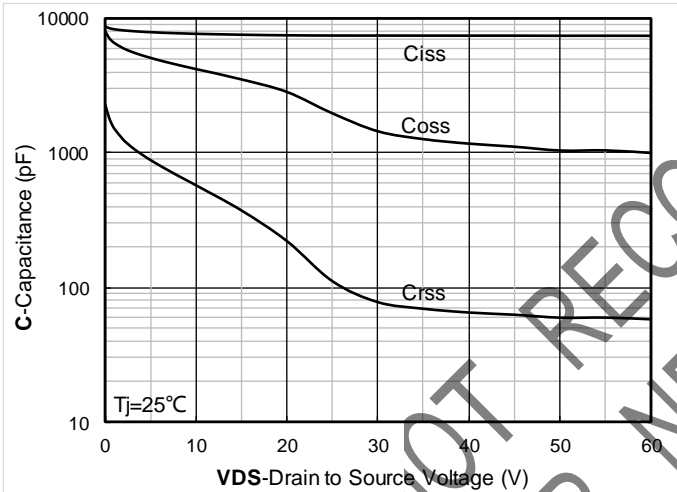


Figure 3. Capacitance Characteristics

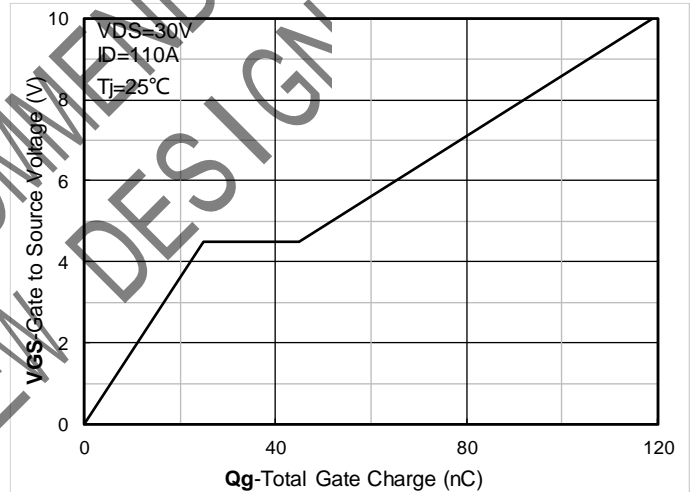


Figure 4. Gate Charge

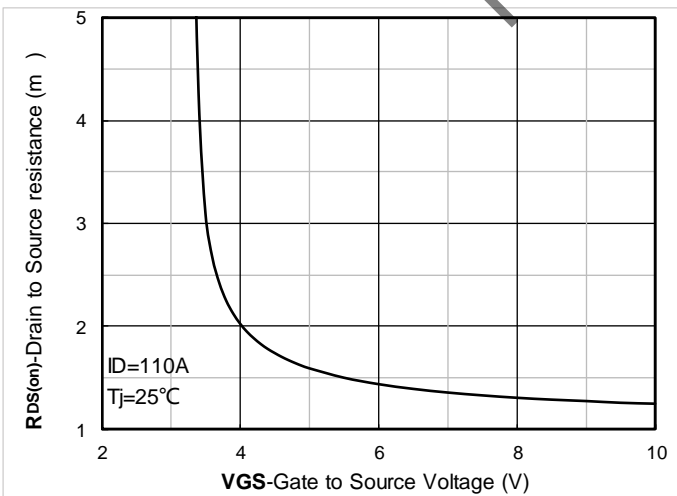


Figure 5. On-Resistance vs Gate to Source Voltage

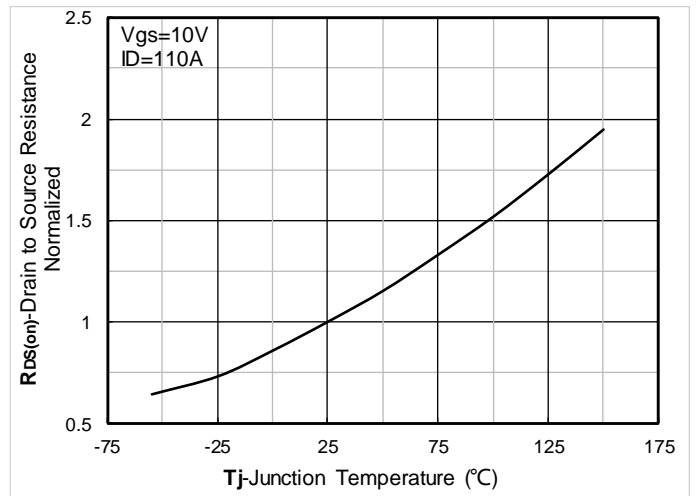


Figure 6. Normalized On-Resistance

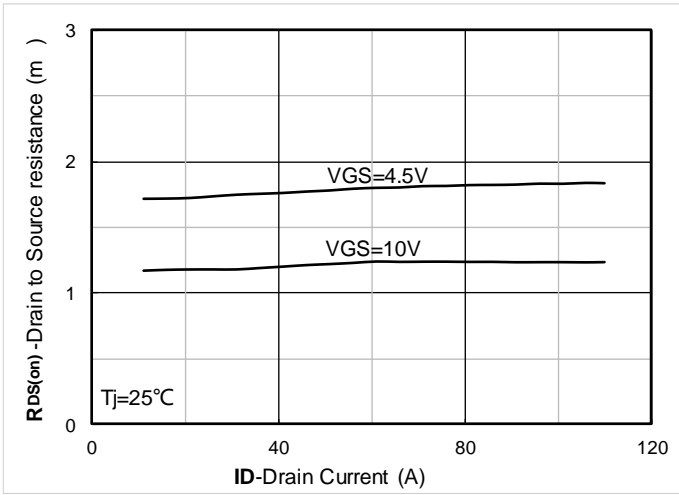


Figure 7. RDS(on) vs Drain Current

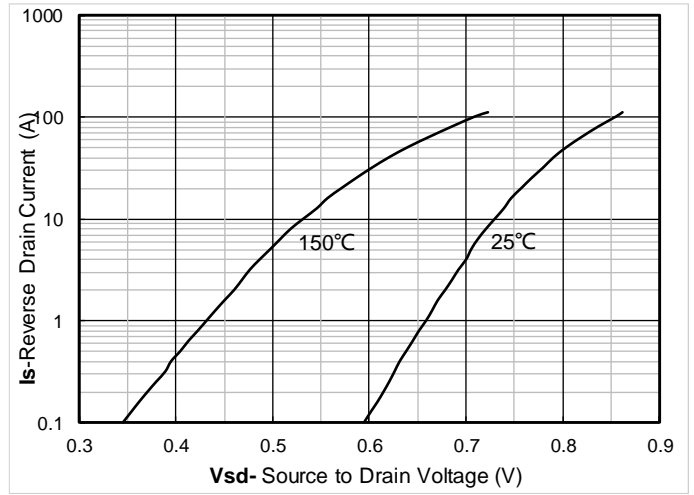


Figure 8. Forward characteristics of reverse diode

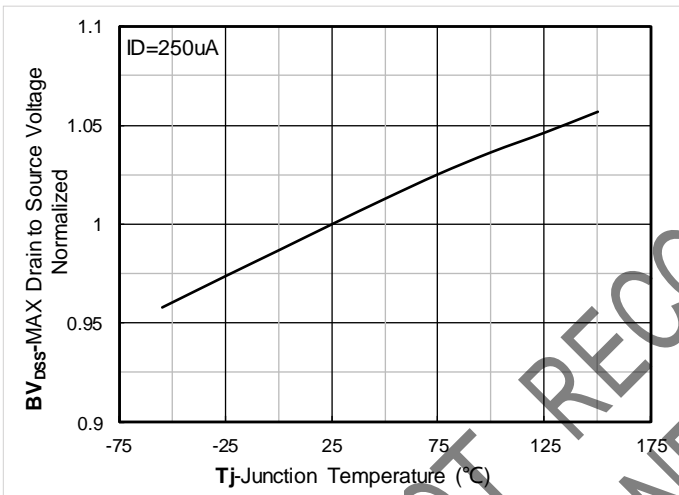


Figure 9. Normalized breakdown voltage



Figure 10. Normalized Threshold voltage

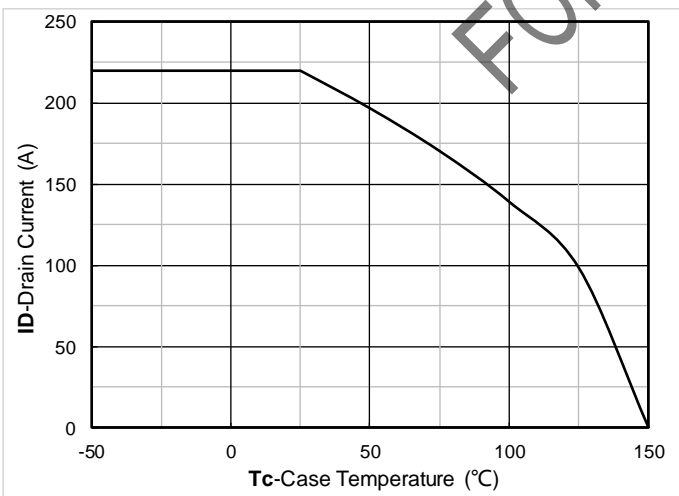


Figure 11. Current dissipation

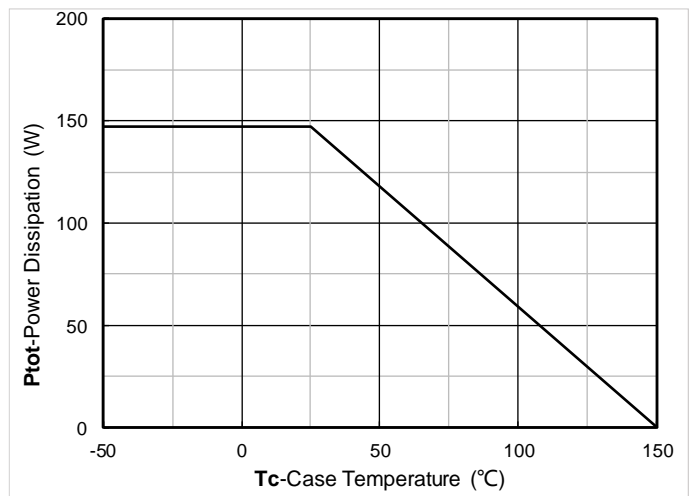


Figure 12. Power dissipation

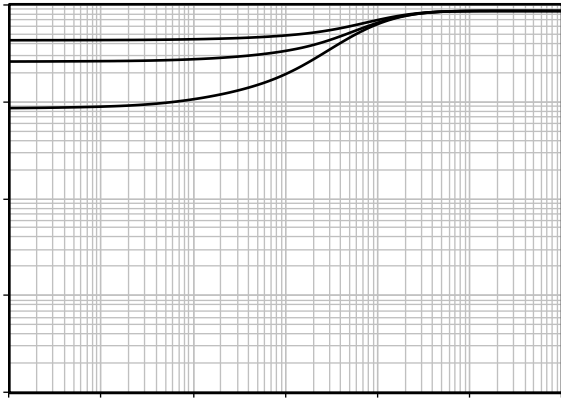


Figure 13. Maximum Transient Thermal Impedance

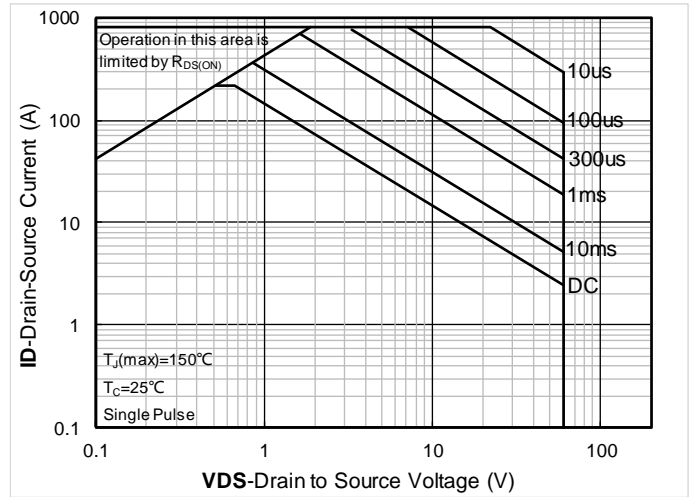


Figure 14. Safe Operation Area

## Test Circuits & Waveforms

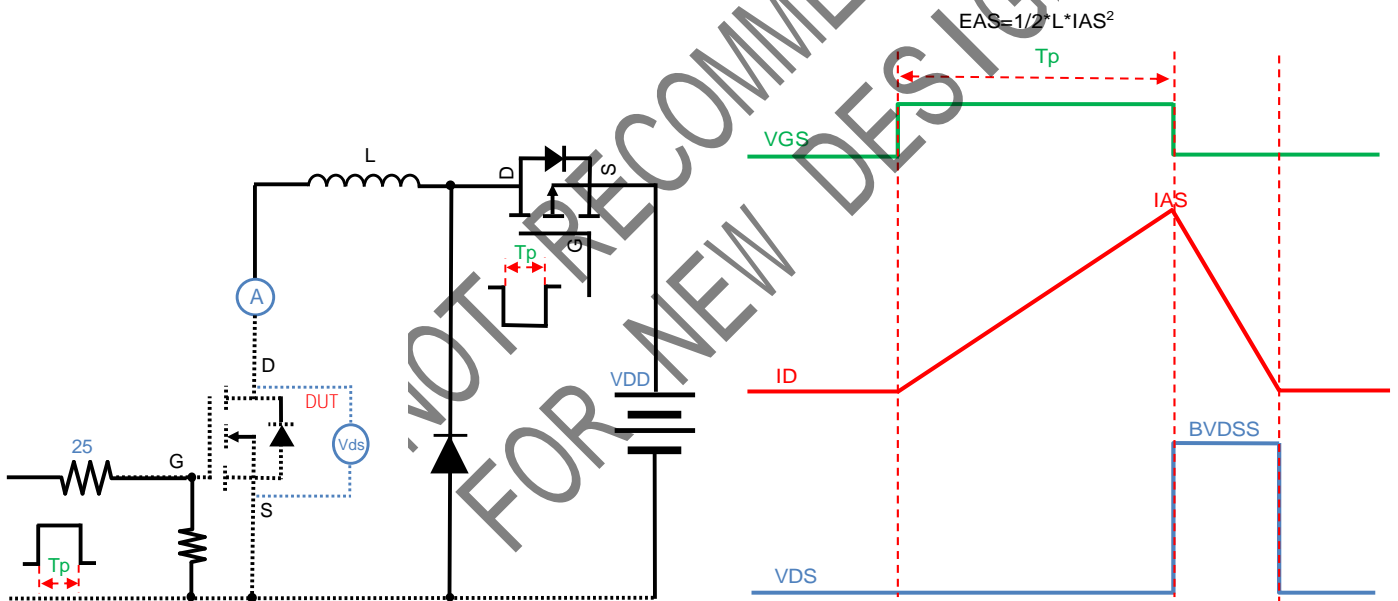


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

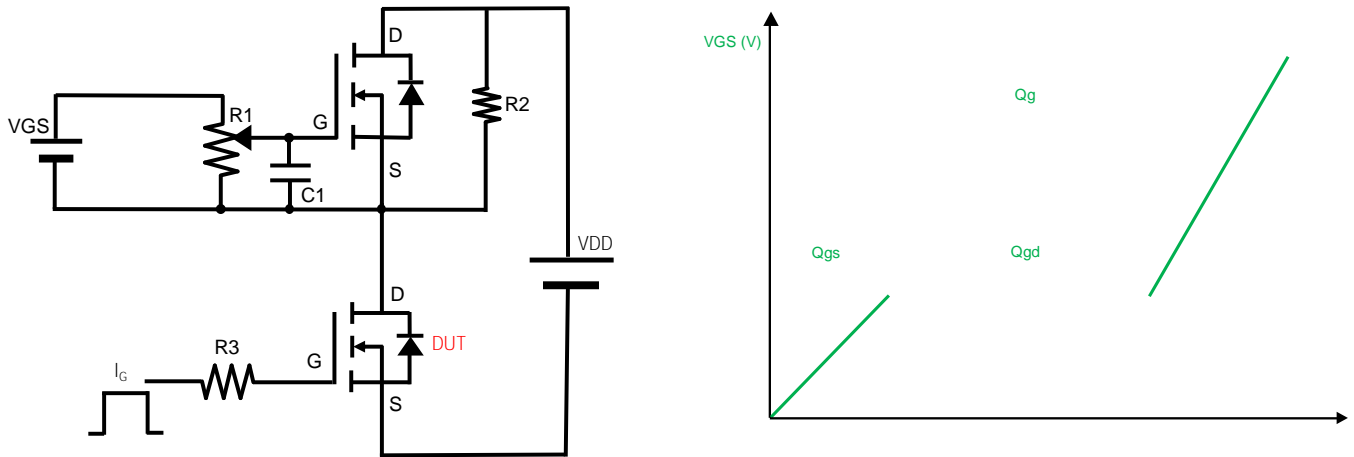


Figure B. Gate Charge Test Circuit & Waveform

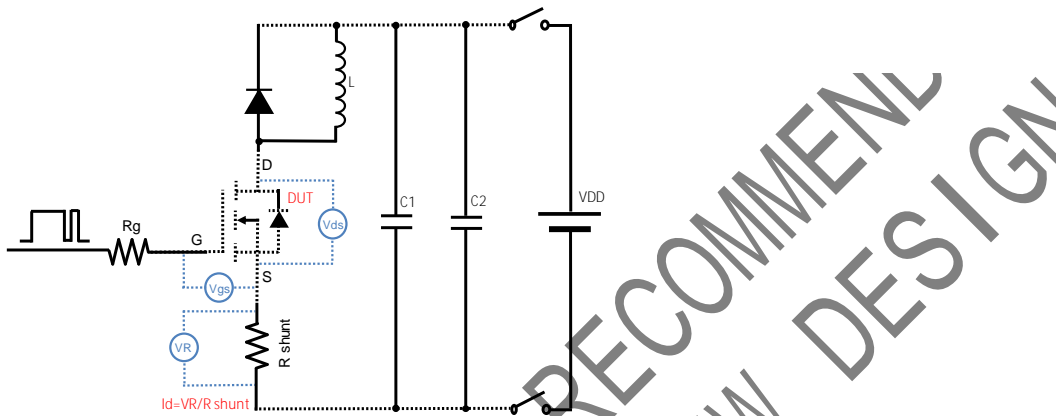


Figure C. Resistive Switching Test Circuit & Waveform

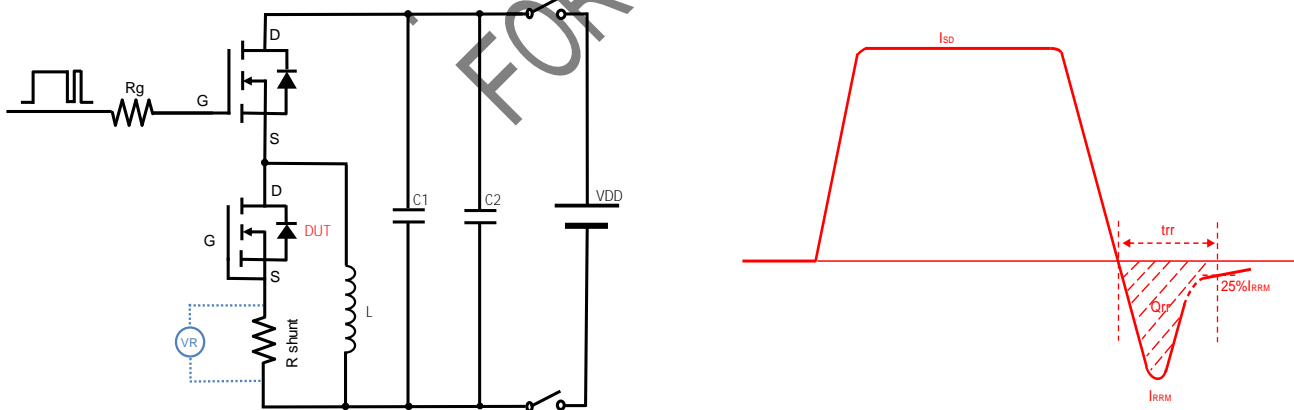
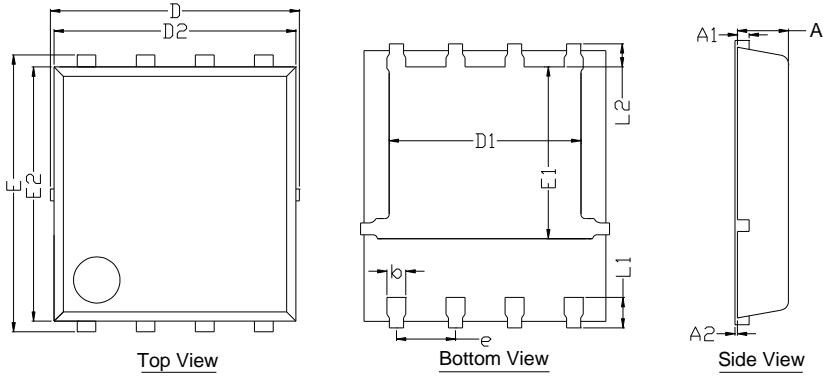


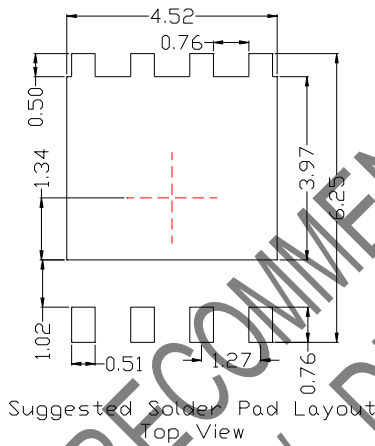
Figure D. Diode Recovery Test Circuit & Waveform



PDFN5060-8L-D-0.95MM Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.05	6.15
A	0.85	0.95	1.00
A1	0.203 BSC		
A2			0.08
D1	4.25	4.35	4.45
E1	3.525	3.625	3.725
D2		5.20	
E2		5.55	
L1	0.45	0.55	0.65
L2	0.68 BSC		
b	0.3	0.4	0.5
e	1.27 BSC		



Note:  
 1. Controlling dimension: in millimeters.  
 2. General tolerance:  $\pm 0.10\text{mm}$ .  
 3. The pad layout is for reference purposes only.

NOT RECOMMEND FOR NEW DESIGN



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