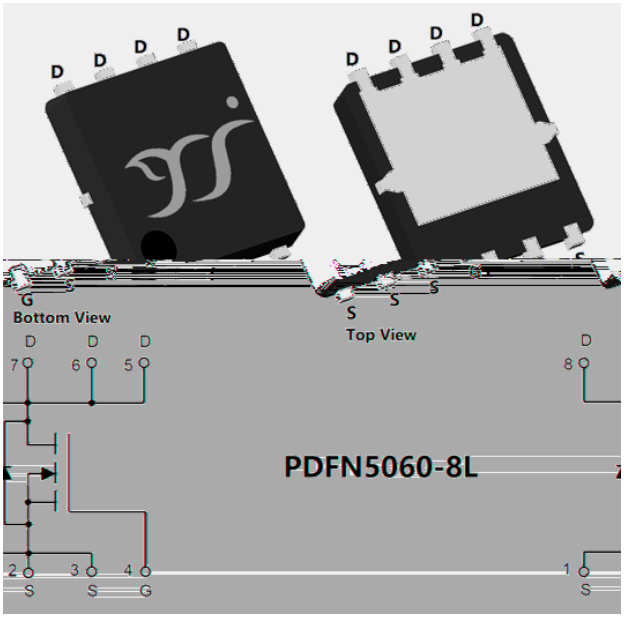
YJG300G04AR

RoHS
COMPLIANT



$_{DS(ON)}$(at V_{GS}=4.5V) 1.4mΩ

- 100% EAS Tested
- 100% VDS Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Moisture Sensitivity Level 1

Applications

- Power switching application T
- Uninterruptible power supply
- DC-DCDN | · rent

	$_A$=25	I_D	42	A
	T_A=100		29	
	T_C=25		300	
	T_C =100		212	
Pulsed Drain Current [A]		I_{DM}	1200	A
Avalanche energy [B]		EAS	1250	mJ
Total Power Dissipation [C]	T_A=25	P_D	3	W
	T_A=100		1.5	
	T_C=25		136	
	T_C =100		68	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +175	

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	Steady-State	$R_{\theta JA}$	40	50	/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.9	1.1	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG300G04AR	F1	G300G04AR	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=1mA	40	-	-	V
		V_{GS}= 0V, I_D=10mA	40	-		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1	μA
		V_{DS}=40V, V_{GS}=0V, Tj=100	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=50A	-	0.65	0.9	mΩ
		V_{GS}=10V, I_D=20A	-	0.65	0.9	
		V_{GS}=4.5V, I_D=20A	-	1	1.4	
Diode Forward Voltage	V_{SD}	I_S=50A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	2	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	300	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=20V, V_{GS}=0V, f=1MHz	-	6125	-	pF
Output Capacitance	C_{oss}		-	3250	-	
Reverse Transfer Capacitance	C_{rss}		-	150	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=20V, I_D=50A	-	101	-	nC
Gate-Source Charge	Q_{gs}		-	21	-	
Gate-Drain Charge	Q_{gd}		-	21	-	
Reverse Recovery Charge	Q_{rr}	I_F=50A, di/dt=100A/us	-	94	-	nC
Reverse Recovery Time	t_{rr}		-	69	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=20V, I_D=50A R_{GEN}=3Ω	-	16	-	ns
Turn-on Rise Time	t_r		-	44	-	
Turn-off Delay Time	$t_{D(off)}$		-	71	-	
Turn-off fall Time	t_f		-	45	-	

A. Repetitive rating; pulse width limited by max. junction temperature.
B. T_J=25 , V_G=10V, R_G=25Ω, L=4mH, IAS=25A.
C. P_d is based on max. junction temperature, using junction-case thermal resistance.
D. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in the still air environment with T_A =25 . The maximum allowed junction temperature of 175 . The value in any given application depends on the user's specific board design.

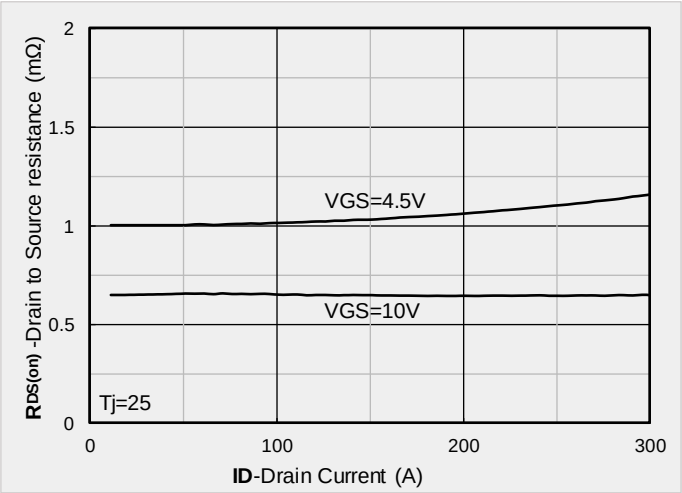


Figure 7. $R_{DS(on)}$ VS Drain Current

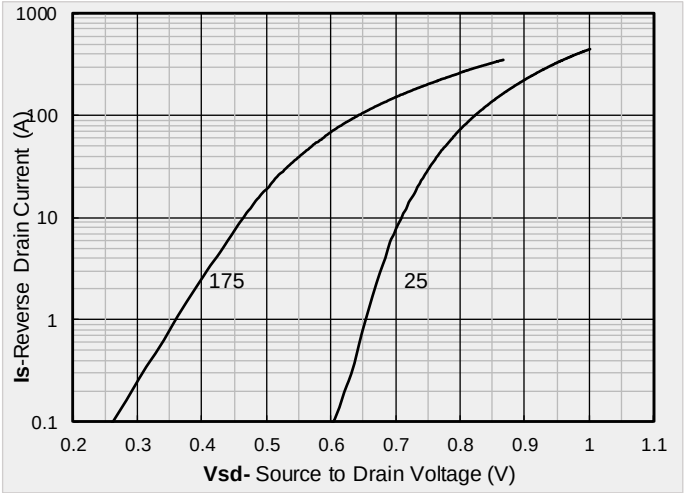
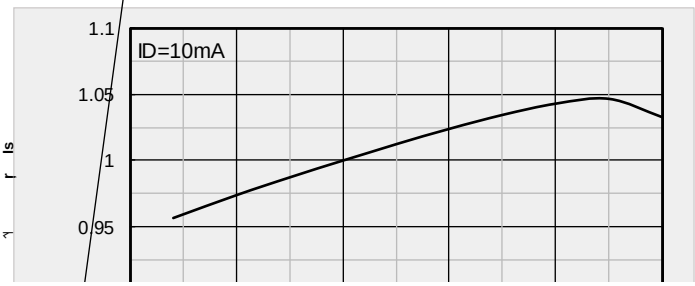


Figure 8. Forward characteristics of reverse diode



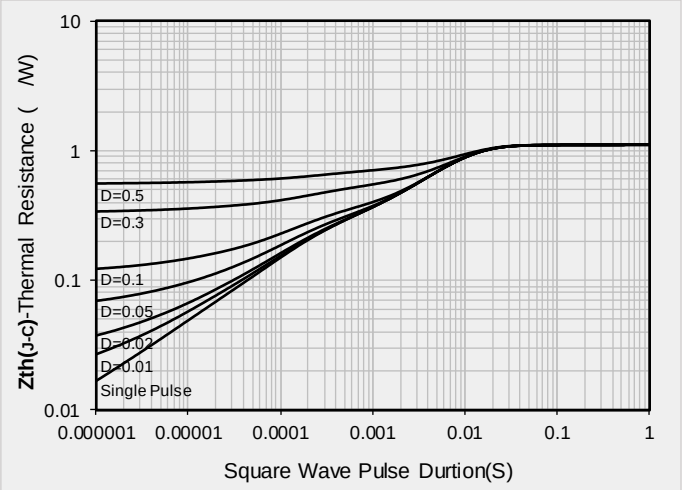


Figure 13. Maximum Transient Thermal Impedance

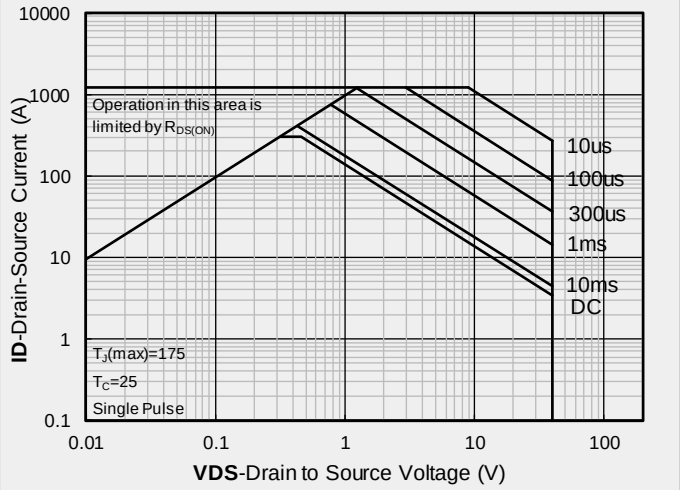
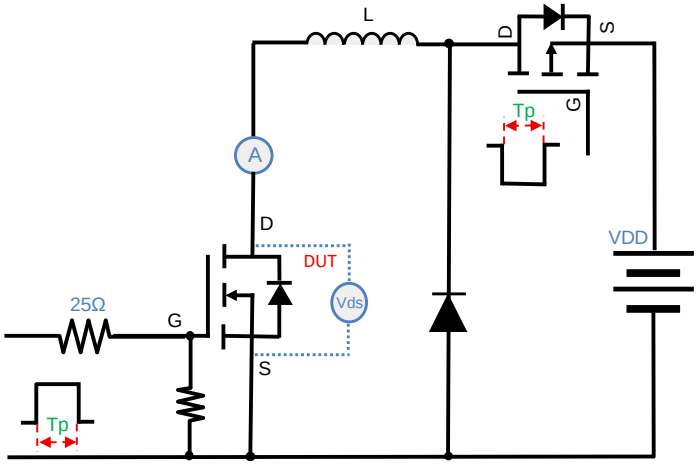
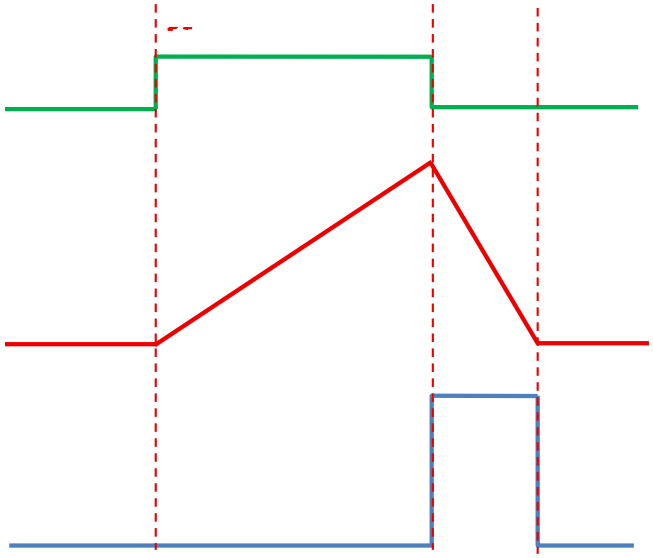


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms





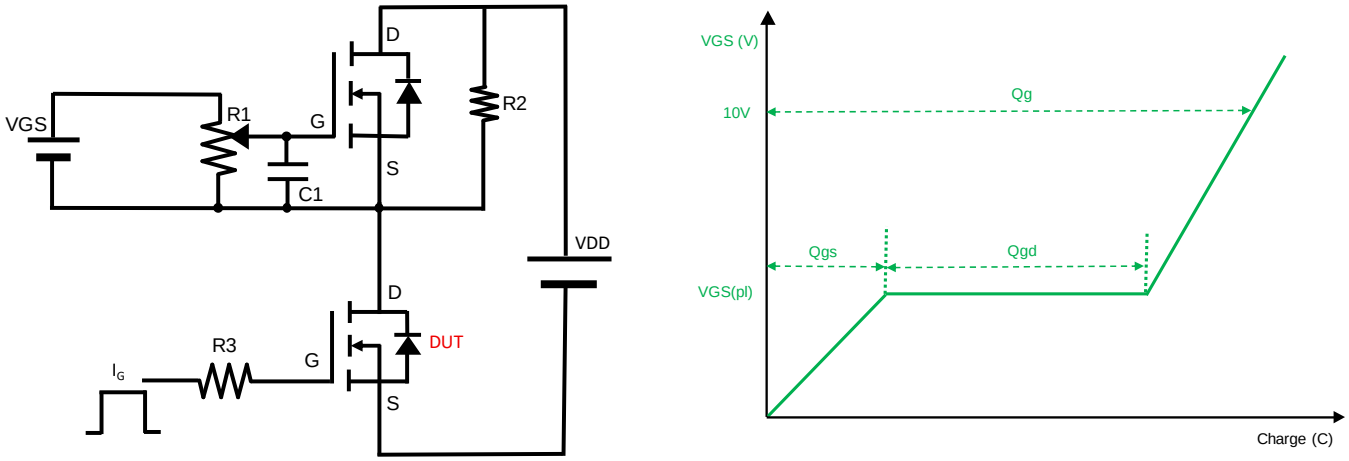


Figure B. Gate Charge Test Circuit & Waveform

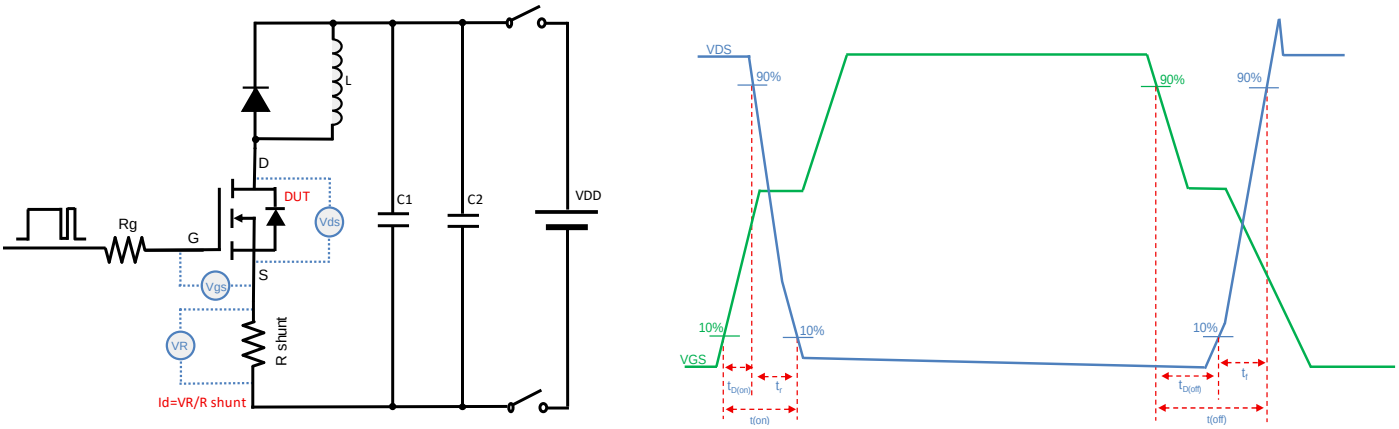


Figure C. Resistive Switching Test Circuit & Waveform

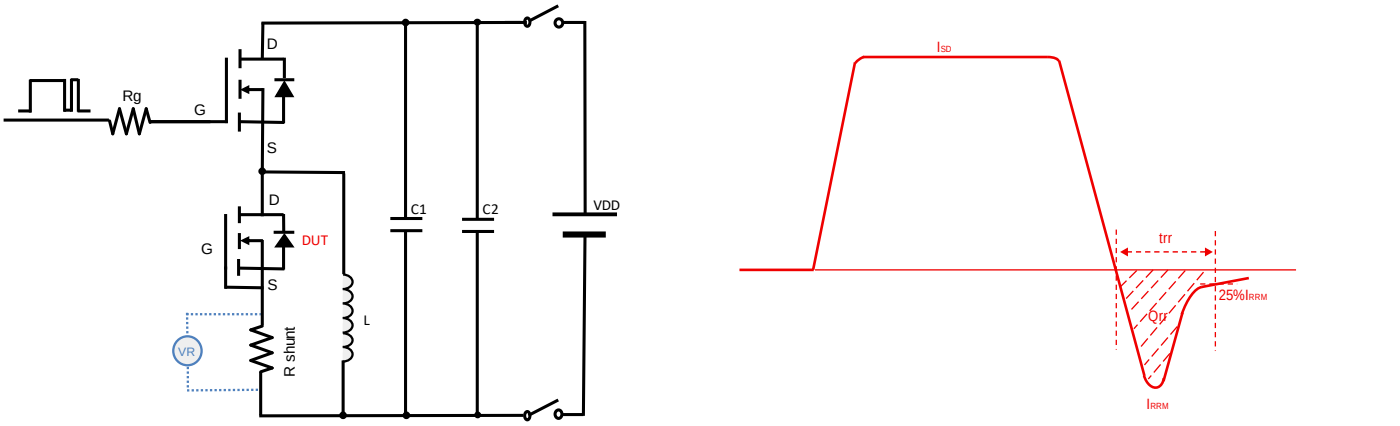
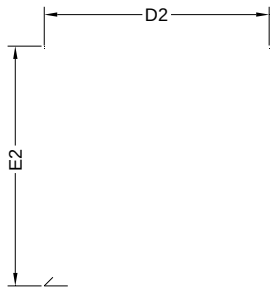
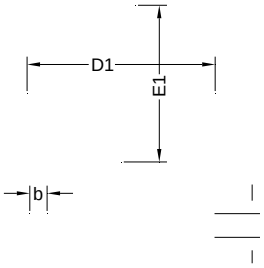


Figure D. Diode Recovery Test Circuit & Waveform

■ PDFN5060-8L-D-0.95MM Package information



Top View



Bottom View

Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.05	6.15
A	0.85	0.95	1.00
A1		0.203 BSC	
A2			0.08
D1	4.25	4.35	4.45
E1	3.525	3.625	3.725
D2		5.20	
E2		5.55	
L1	0.45	0.55	0.65
L2		0.68 BSC	
b	0.3	0.4	0.5
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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