P-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	-60V
I_D	-40A
$R_{DS(ON)}$(at V_{GS}=-10V)	25 mohm
$R_{DS(ON)}$(at V_{GS}=-4.5V)	30 mohm

100% EAS Tested
100% V_{DS} Tested

General Description

Split gate trench MOSFET technology
Low $R_{DS(on)}$ & FOM
Low Crss
Extremely low switching loss
Excellent stability and uniformity
Moisture Sensitivity Level 1
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

Load Switch
Industrial DC/DC Conversion Circuits

Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	V_{DS}		

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250		-60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-60V,V_{GS}=0V	T_J=25			-1	
			T_J=55			-5	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= 20V, V_{DS}=0V				100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250		-1.3	-1.8	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -10V, I_D=-20A			16	25	m
		V_{GS}= -4.5V, I_D=-10A			23	30	
Gate Resistance	Rg	f=1MHz			6		
Diode Forward Voltage	V_{SD}	I_S=-20A,V_{GS}=0V			-0.85	-1.3	V
Maximum Body-Diode Continuous Current	I_S					-40	A
Dynamic Parameters							
Input Capacitance	C_{iss}	V_{DS}=-30V,V_{GS}=0V,f=1MHZ			2200		pF
Output Capacitance	C_{oss}				700		
Reverse Transfer Capacitance	C_{rss}				56		
Switching Parameters							
Total Gate Charge	$Q_{g(-10V)}$	V_{GS}=-10V,V_{DS}					

■ Typical Performance Characteristics

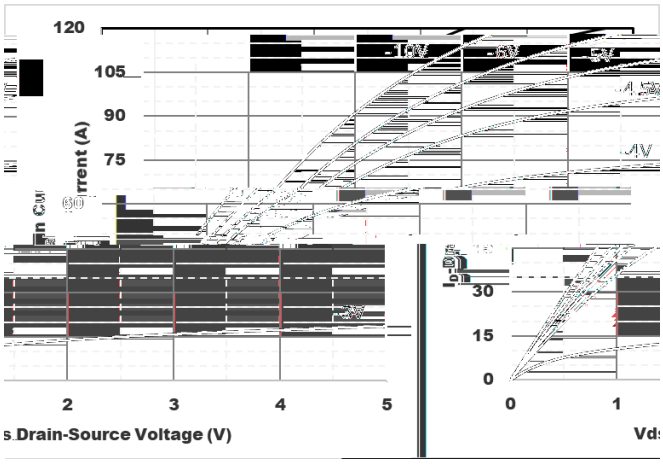


Figure1. Output Characteristics

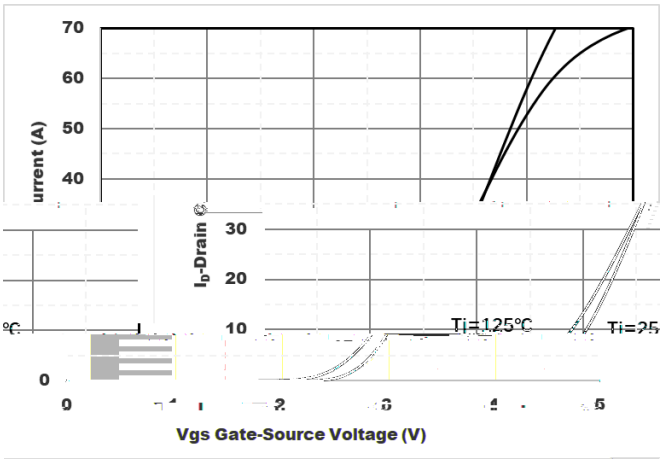


Figure2. Transfer Characteristics

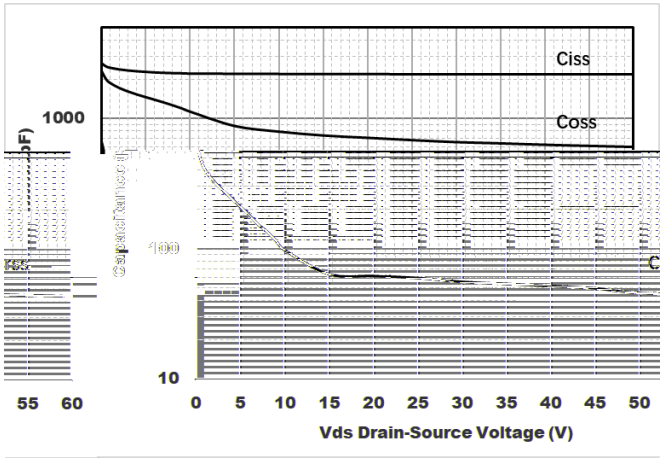


Figure3. Capacitance Characteristics

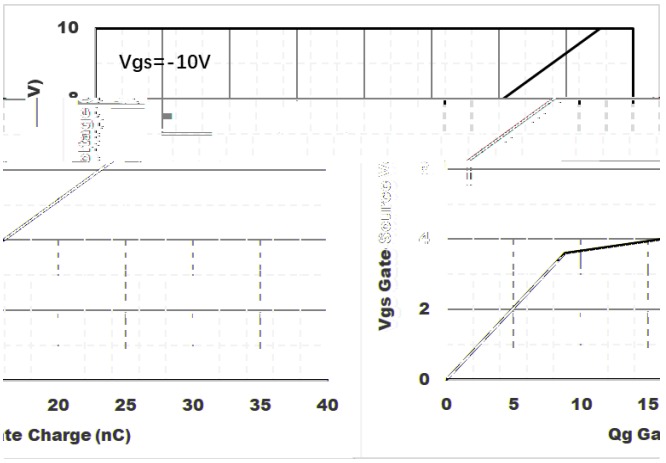


Figure4. Gate Charge

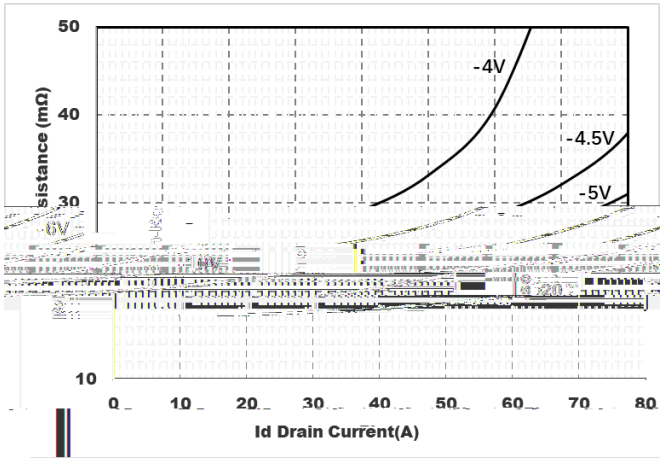


Figure5. : On-Resistance vs. Gate to Source Voltage

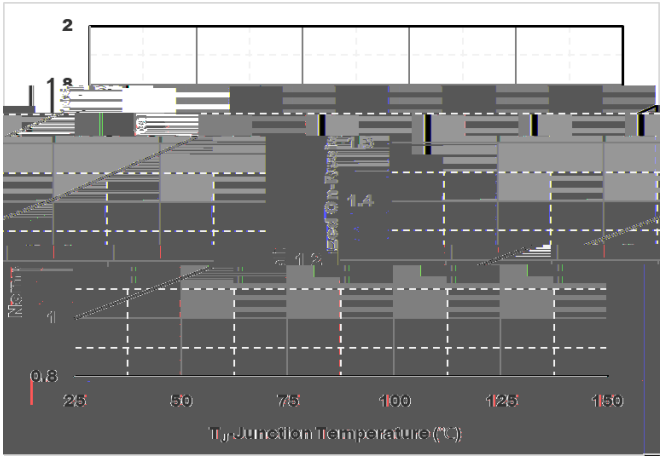


Figure6.Normalized On-Resistance

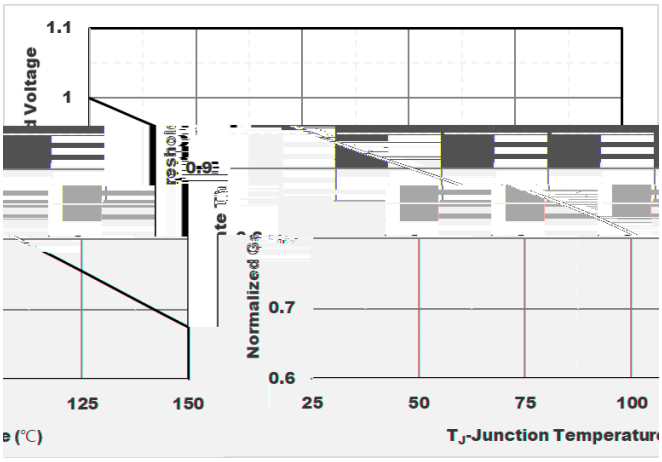


Figure7. Normalized Gate Threshold Voltage

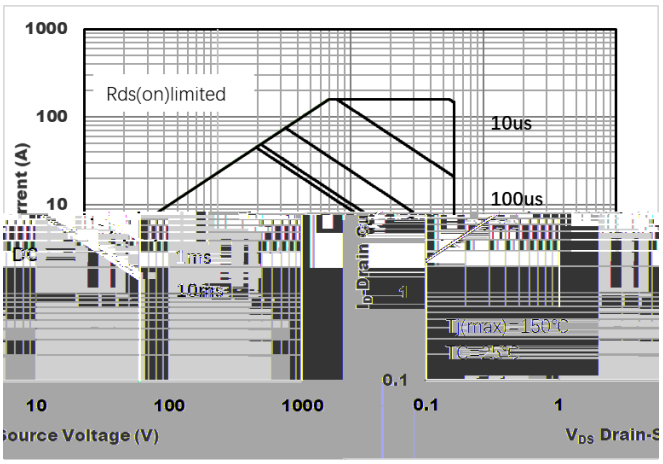


Figure8.Safe Operation Area

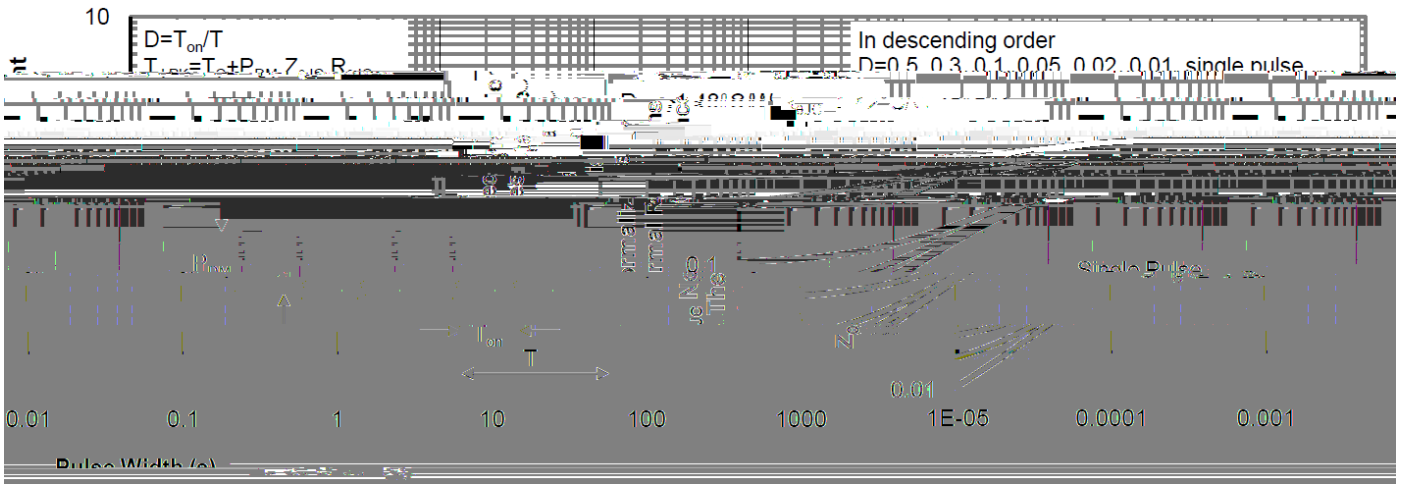
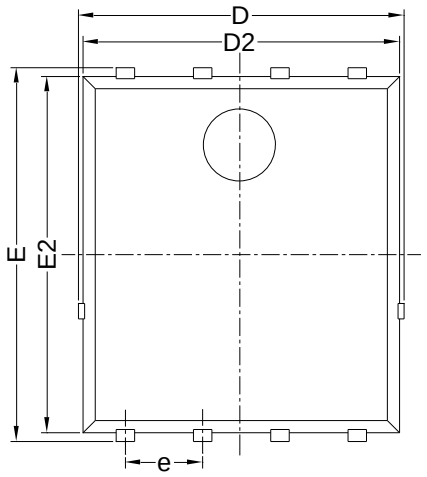
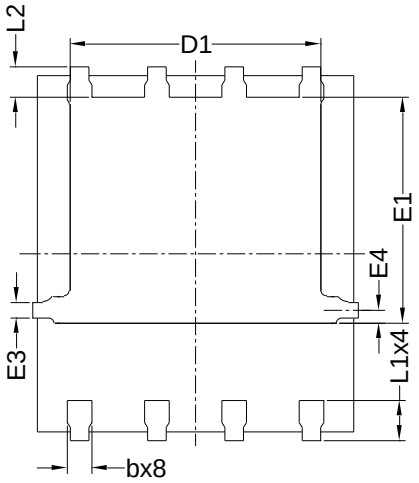


Figure9.Normalized Maximum Transient thermal impedance

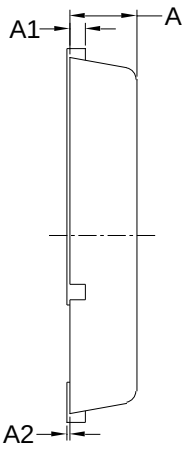
PDFN5060-8L-B-1.1MM Package information



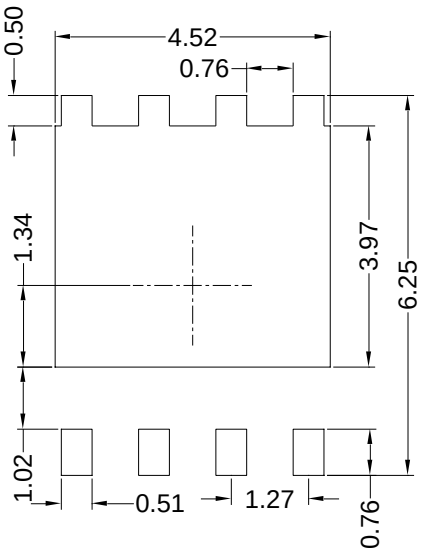
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254 REF	
E4		0.21 REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

Disclaimer

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