



N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	30V
I_D	50A
R	



YJG50N03B

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ± 20V, V _{DS} =0V			± 100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		3.9	6.0	m
		V _{GS} = 4.5V, I _D =15A		6.0	8.0	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.85	1.2	V
Maximum Body-Diode Continuous Current	I _S				80	A
Gate Resistance	R _g	f =1 MHz		2.3		
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ		2191		pF
Output Capacitance	C _{oss}			300		
Reverse Transfer Capacitance	C _{rss}			247		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =20A		46.3		nC
Gate-Source Charge	Q _{gs}			8.8		
Gate-Drain Charge	Q _{gd}			9.2		
Reverse Recovery Chrage	Q _{rr}	I _F =20A, di/dt=100A/us		1.6		
Reverse Recovery Time	t _{rr}			11		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =15V, R _L =0.75 R _{GEN} =3		11		ns
Turn-on Rise Time	t _r			80		
Turn-off Delay Time	t _{D(off)}			39		

Turn-off fall Time



Typical Performance Characteristics

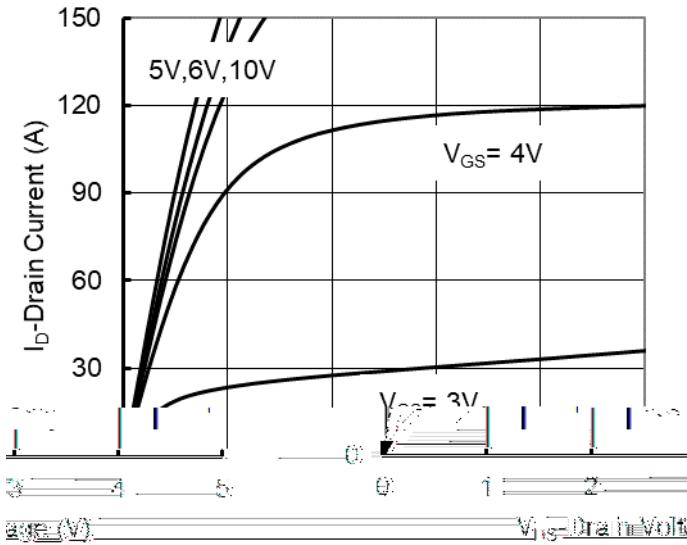


Figure 1. Output Characteristics

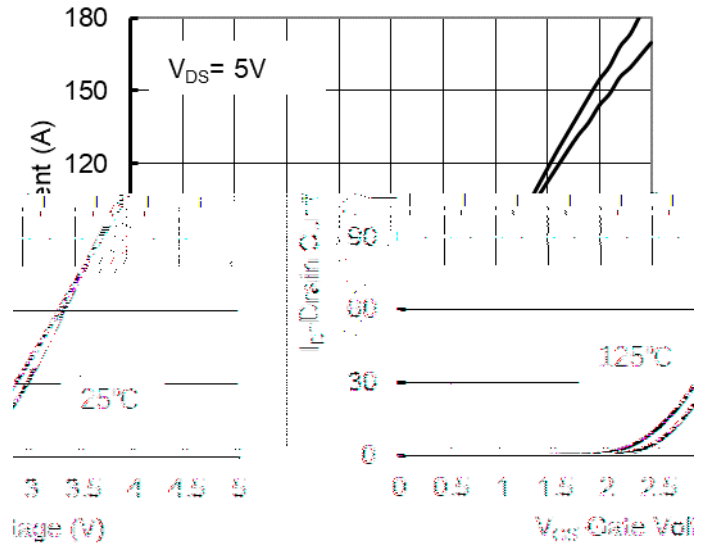


Figure 2. Transfer Characteristics

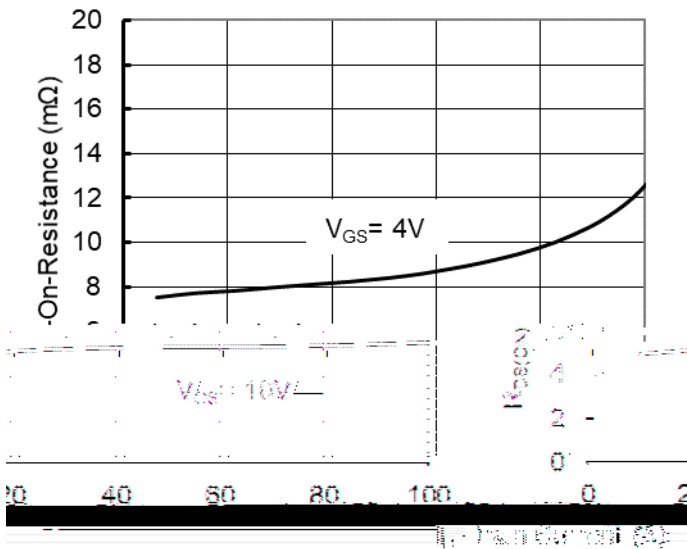


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

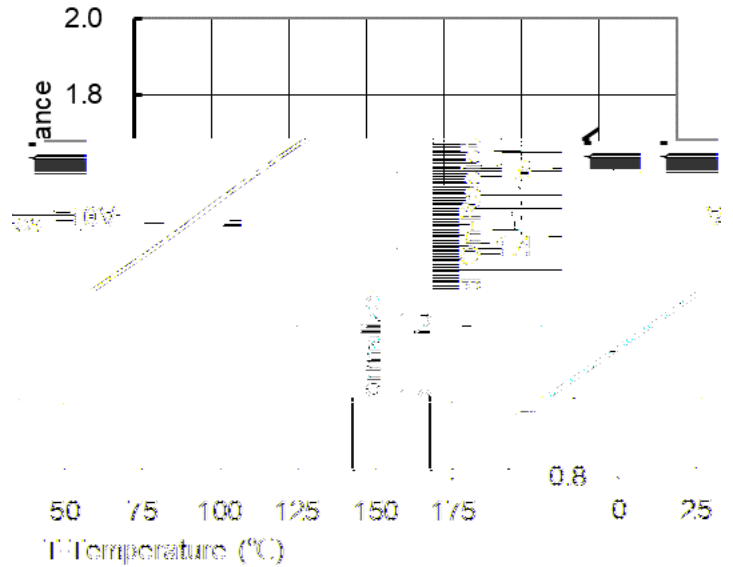


Figure 4. On-Resistance vs. Junction Temperature

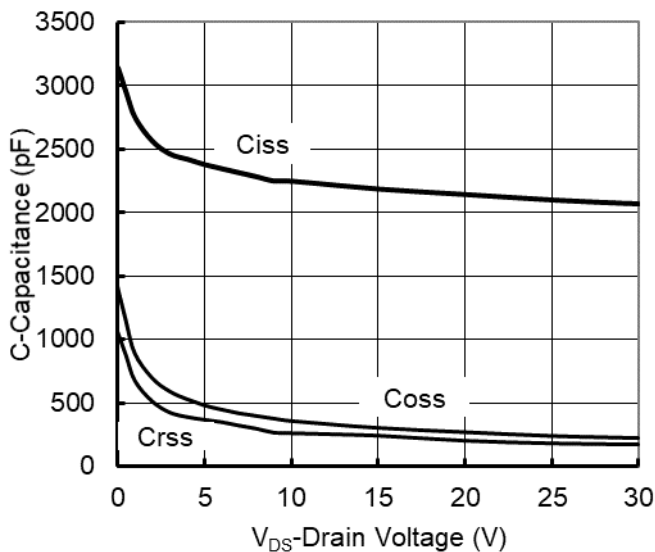


Figure 5. Capacitance Characteristics

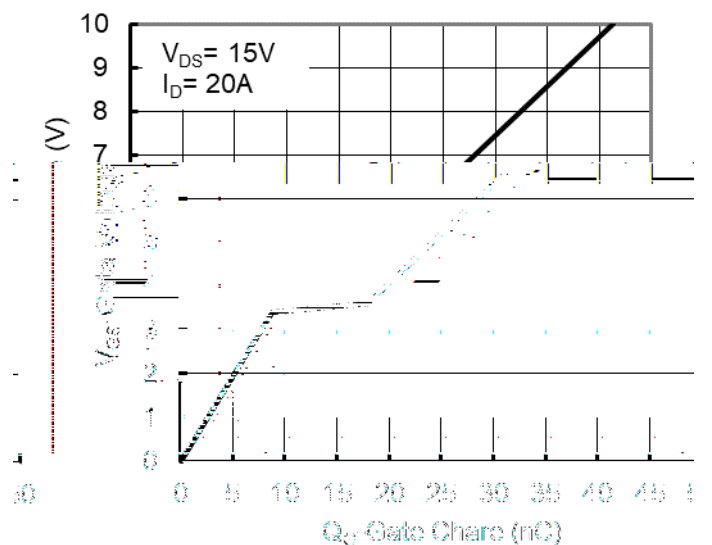
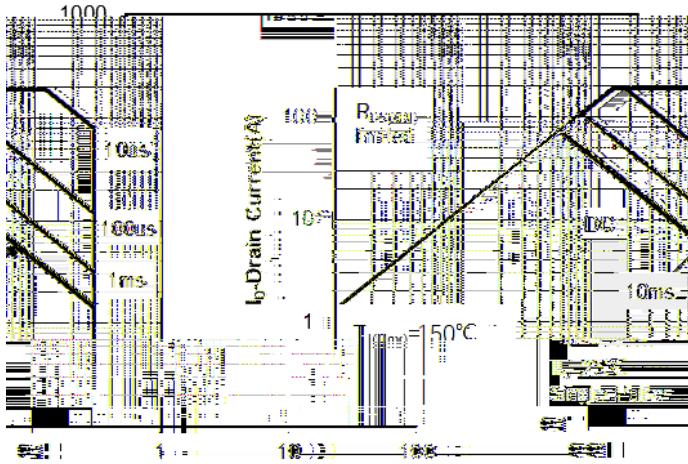


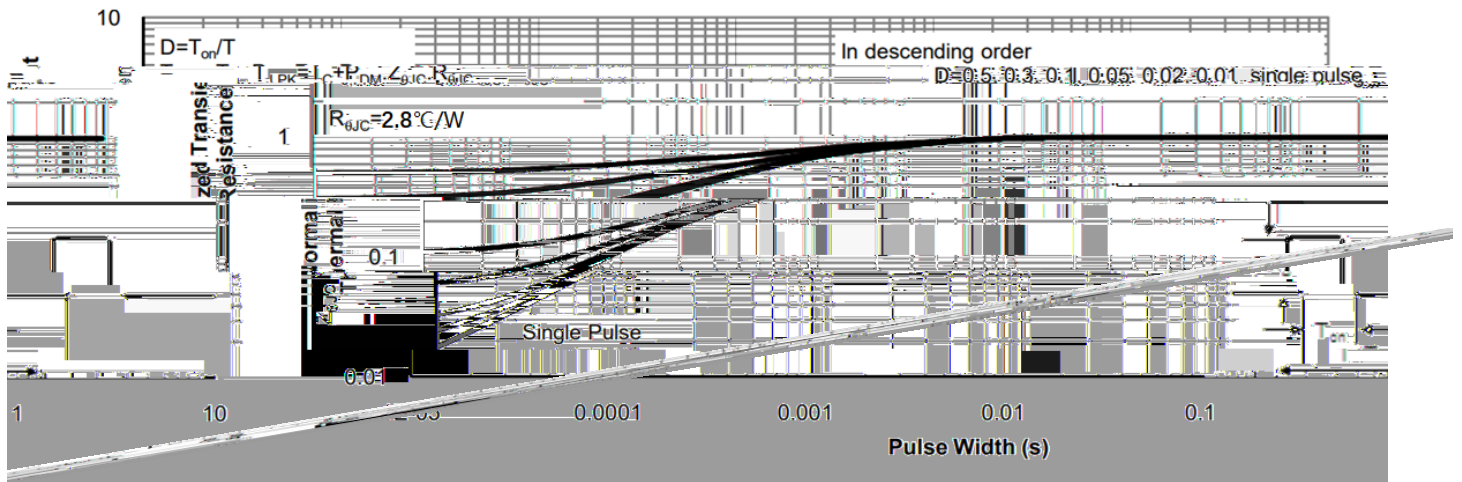
Figure 6. Gate Charge

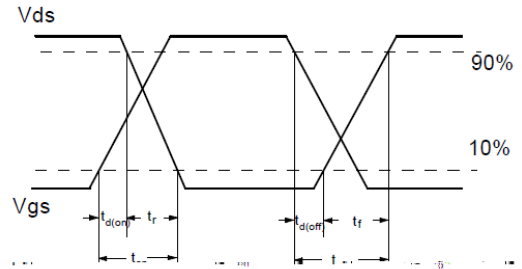
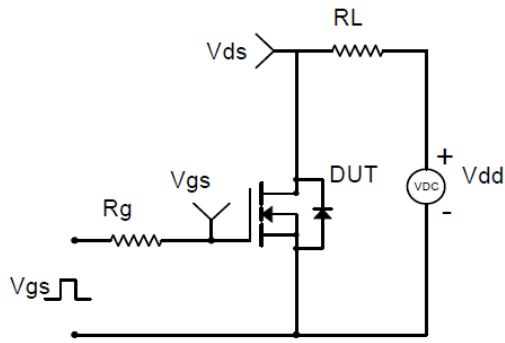


V_{DS} Drain-Source Voltage(V)

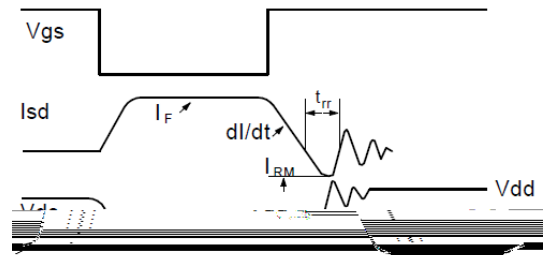
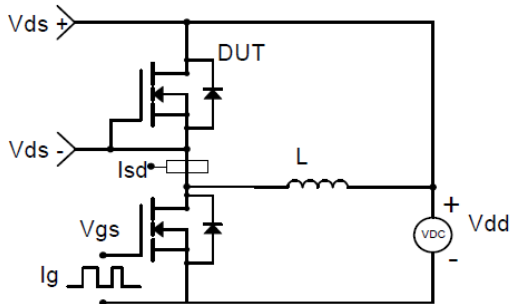
Figure 7. Safe Operation Area

Figure 8. Maximum Continuous Drain Current vs Case Temperature

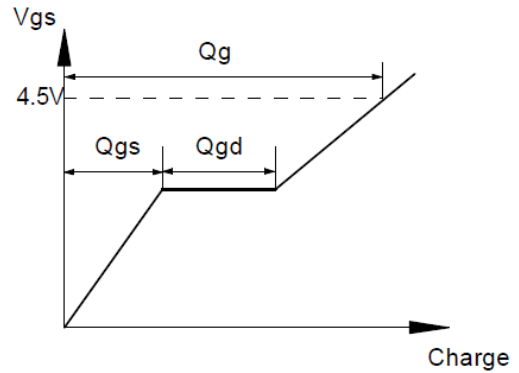
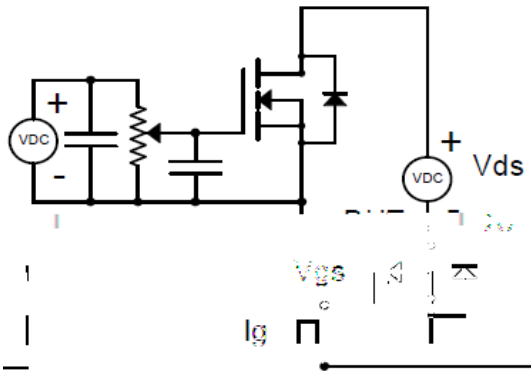




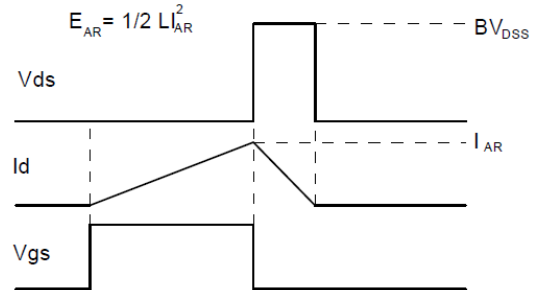
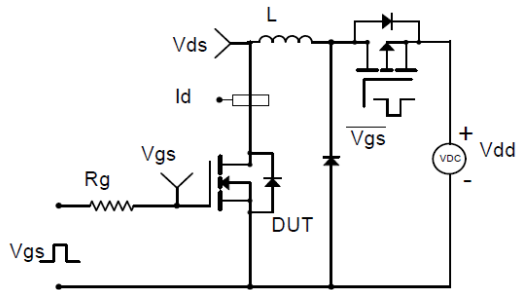
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

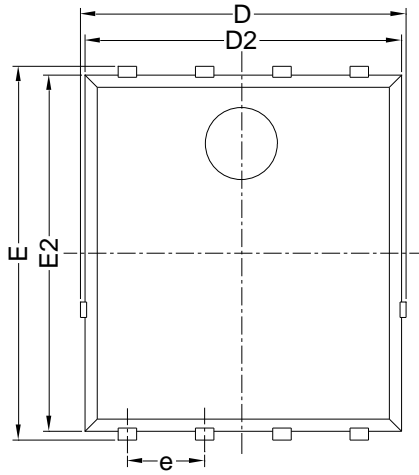


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

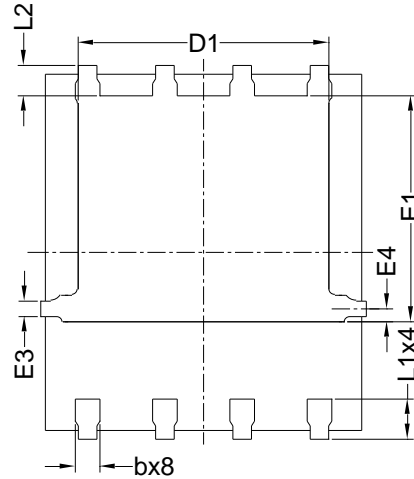


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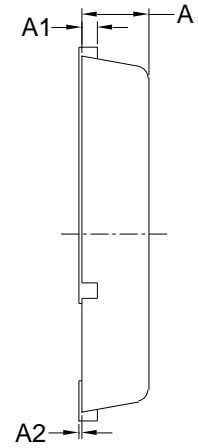
PDFN5060-8L-B-1.1MM Package Information



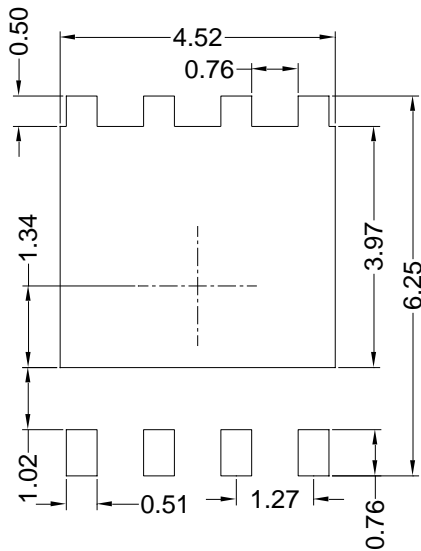
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



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