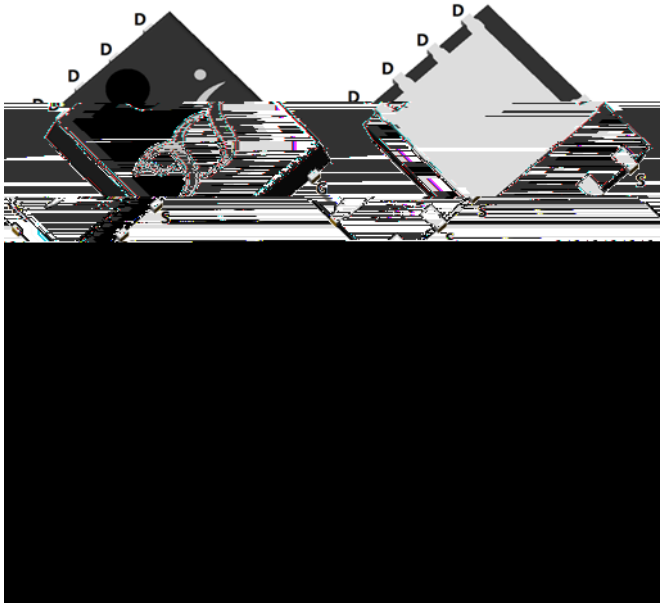
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 100V
- I_D 58A
- $R_{DS(ON)}$(at V_{GS}=10V) 12mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) 17mΩ
- 100% EAS Tested
- 100% V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25	I_D	9.5	A
	T_A=100		6.5	
	T_C=25		58	
	T_C =100		41	
Pulsed Drain Current [A]		I_{DM}	200	A
Avalanche energy [B]		EAS	81	mJ
Total Power Dissipation [C]	T_A=25	P_D	2.7	W
	T_A=100		1.3	
	T_C=25		100	
	T_C =100		50	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +175	

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	Steady-State	$R_{\theta JA}$	45	55	/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.2	1.5	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG58G10B	F1	YJG58G10B	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=1mA	100	-	-	V
		V_{GS}= 0V, I_D=10mA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	μA
		V_{DS}=100V, V_{GS}=0V, Tj=125	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1	1.7	3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	9	12	mΩ
		V_{GS}=4.5V, I_D=20A	-	12	17	
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	1.3	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	58	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	1390	-	pF
Output Capacitance	C_{oss}		-	325	-	
Reverse Transfer Capacitance	C_{rss}		-	11	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=50V, I_D=27.5A	-	27.9	-	nC
Gate-Source Charge	Q_{gs}		-	5	-	
Gate-Drain Charge	Q_{gd}		-	7.8	-	
Reverse Recovery Charge	Q_{rr}	I_F=27.5A, di/dt=100A/us	-	60	-	nC
Reverse Recovery Time	t_{rr}		-	44	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=50V, I_D=27.5A R_{GEN}=2.2Ω	-	8.4	-	ns
Turn-on Rise Time	t_r		-	56	-	
Turn-off Delay Time	$t_{D(off)}$		-	24.4	-	
Turn-off fall Time	t_f		-	7	-	

A. Repetitive rating; pulse width limited by max. junction temperature.
B. T_J=25 , V_G=10V, R_G=25Ω, L=0.5mH, IAS=18A.
C. P_d is based on max. junction temperature, using junction-case thermal resistance.
D. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in the still air environment with T_A =25 . The maximum allowed junction temperature of 175 . The value in any given application depends on the user's specific board design.

Typical Electrical and Thermal Characteristics Diagrams

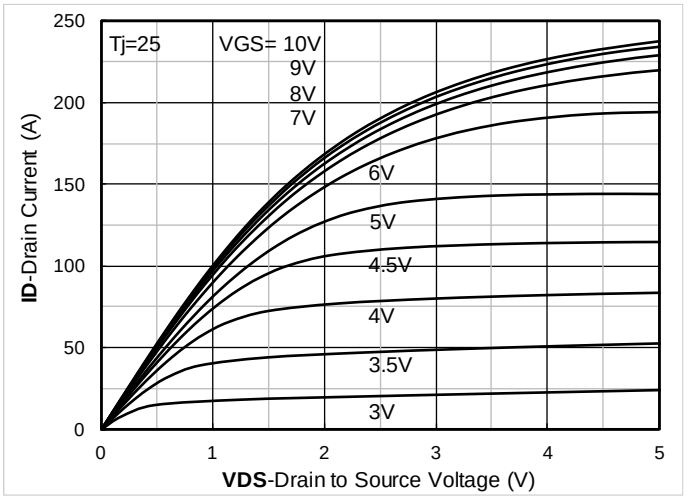


Figure 1. Output Characteristics

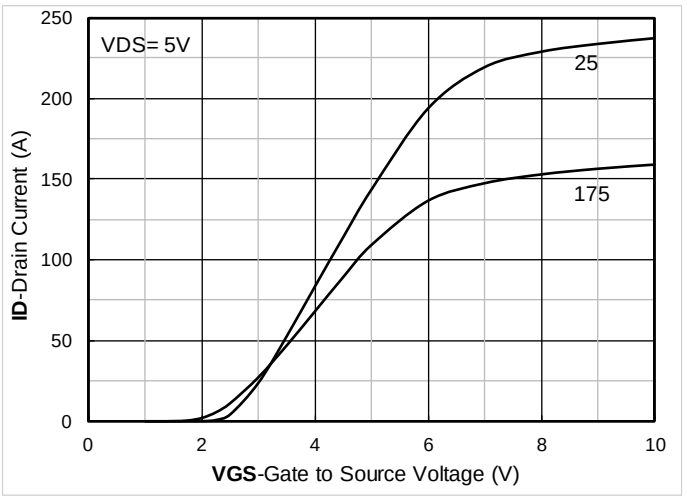


Figure 2. Transfer Characteristics

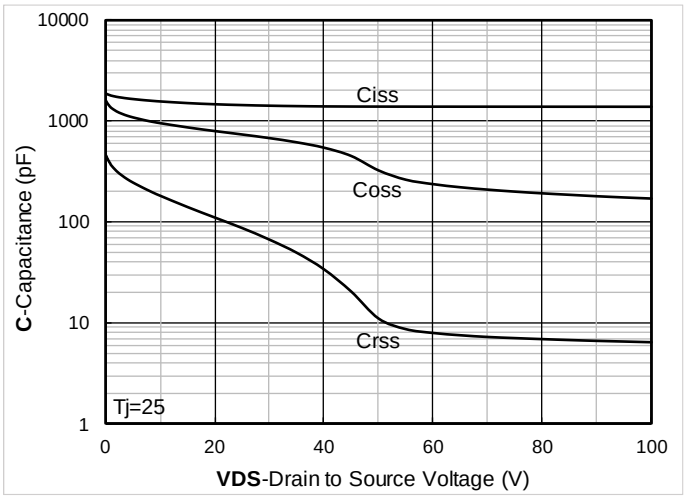


Figure 3. Capacitance Characteristics

Figure 4. Gate Charge

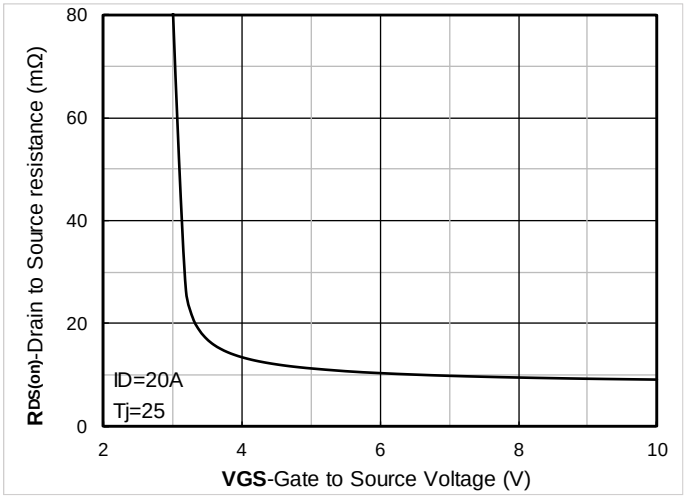


Figure 5. On-Resistance vs Gate to Source Voltage

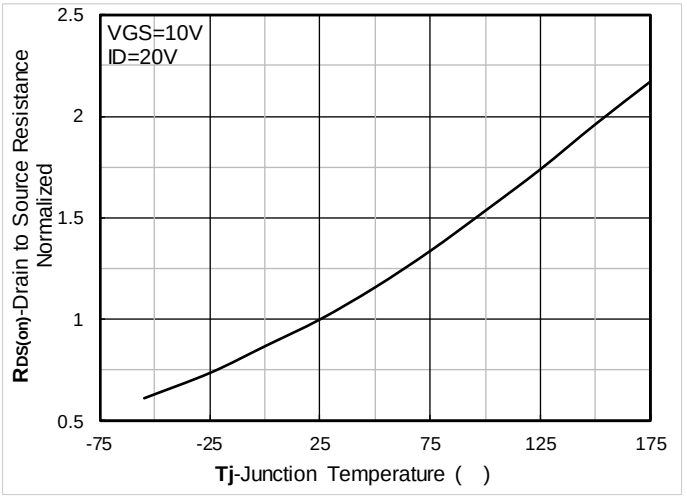


Figure 6. Normalized On-Resistance

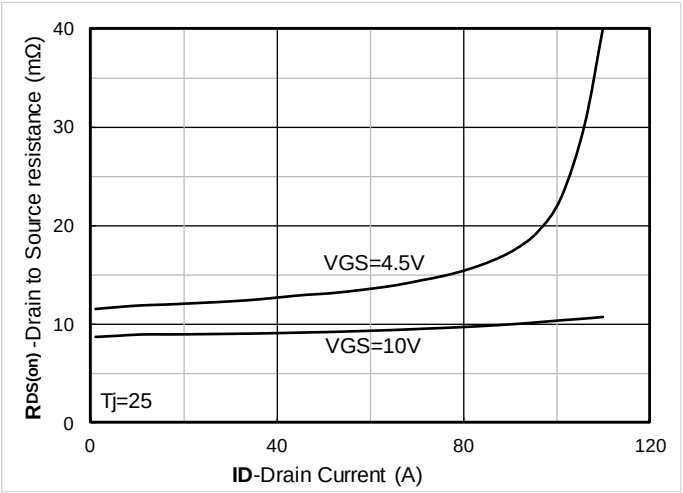


Figure 7. $R_{DS(on)}$ VS Drain Current

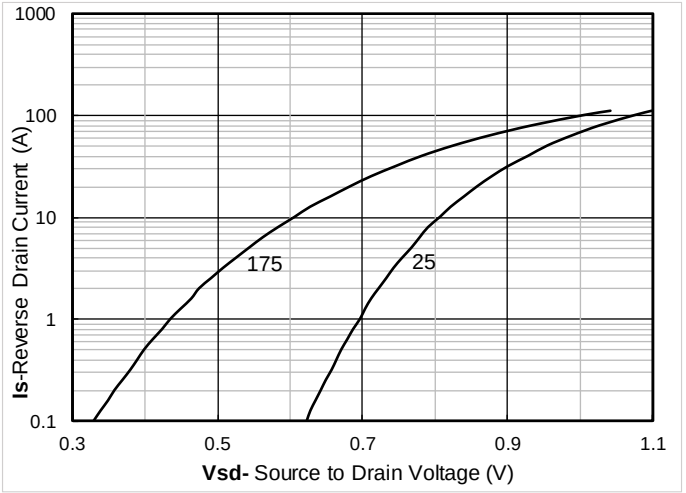
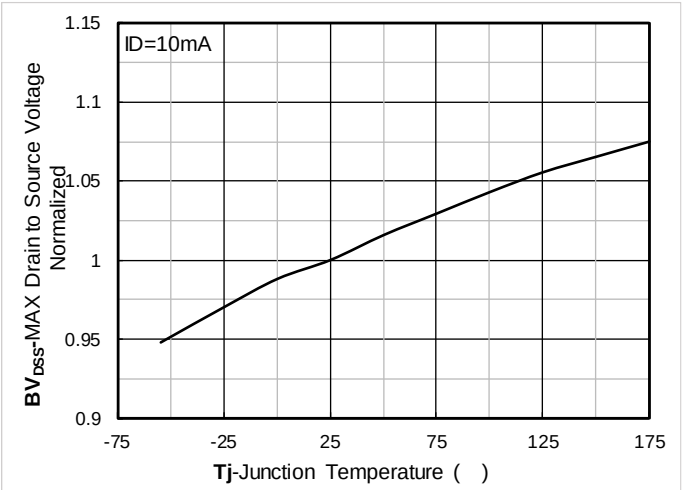
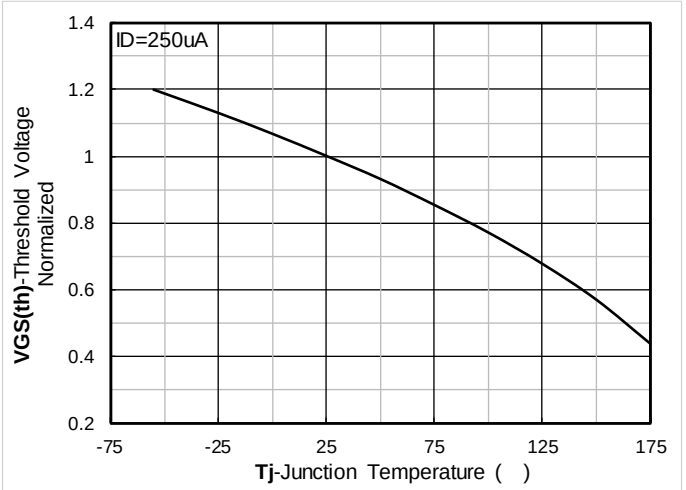


Figure 8. Forward characteristics of reverse diode





. Figure 9. Normalized Breakdown Voltage 882 0 596.04 842.04 reW* nBT/F5 9.96 Tf1 0 0 14586.98 336.05 Tm0 g0 G[ )]T

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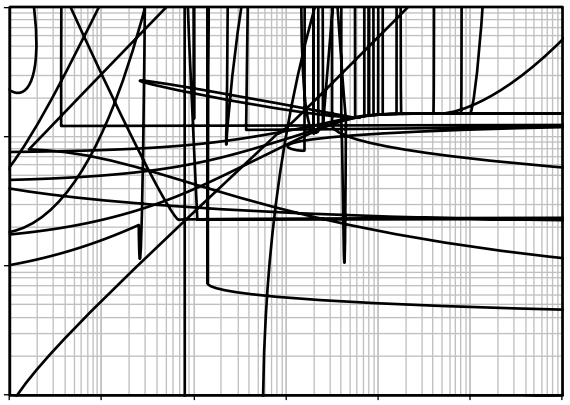


Figure 13. Maximum Transient Thermal Impedance

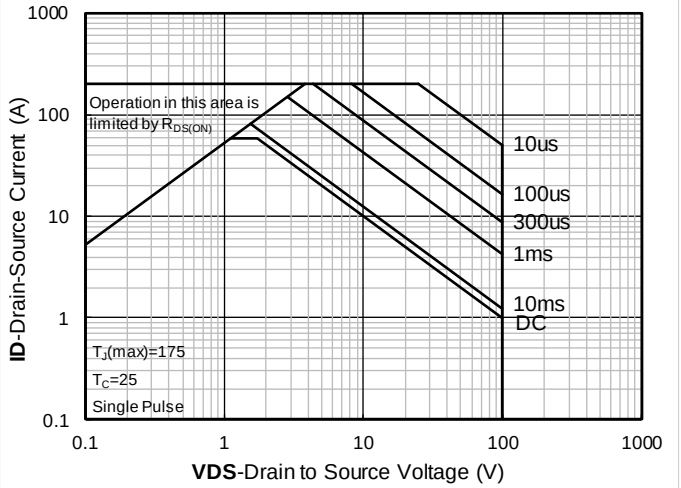


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

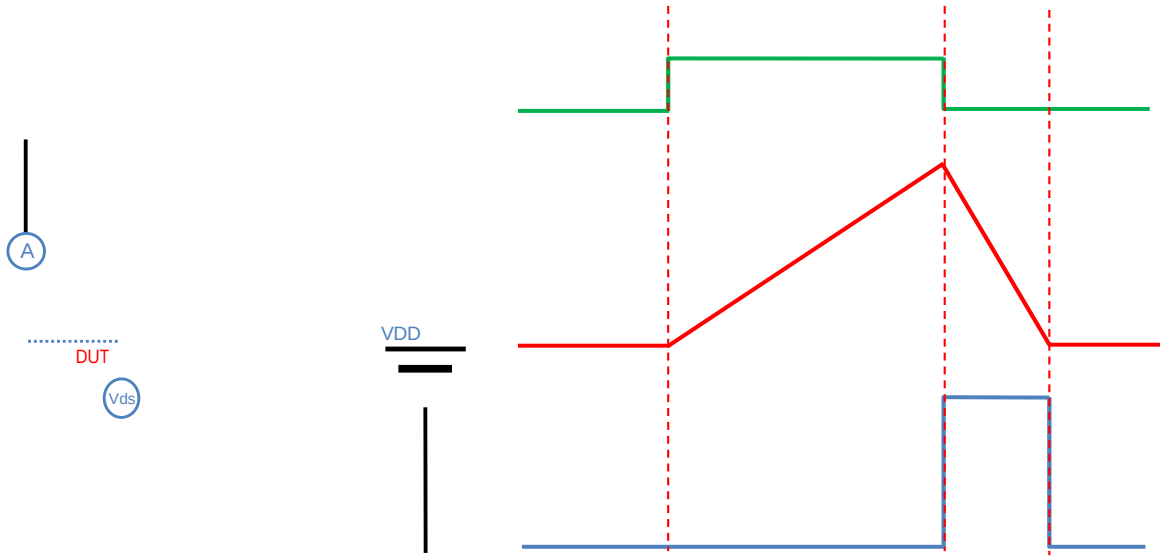


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

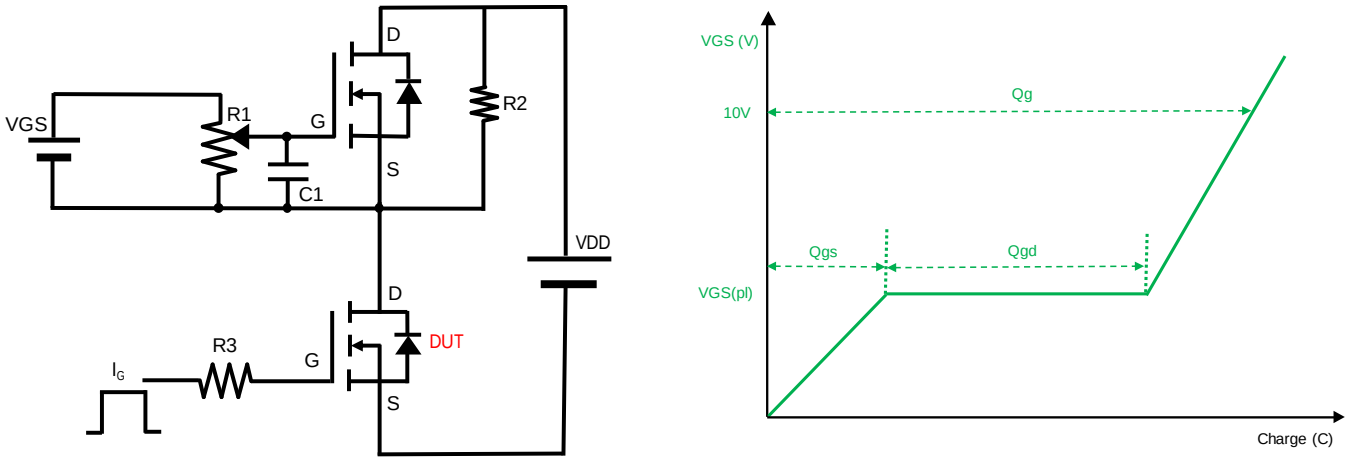


Figure B. Gate Charge Test Circuit & Waveform

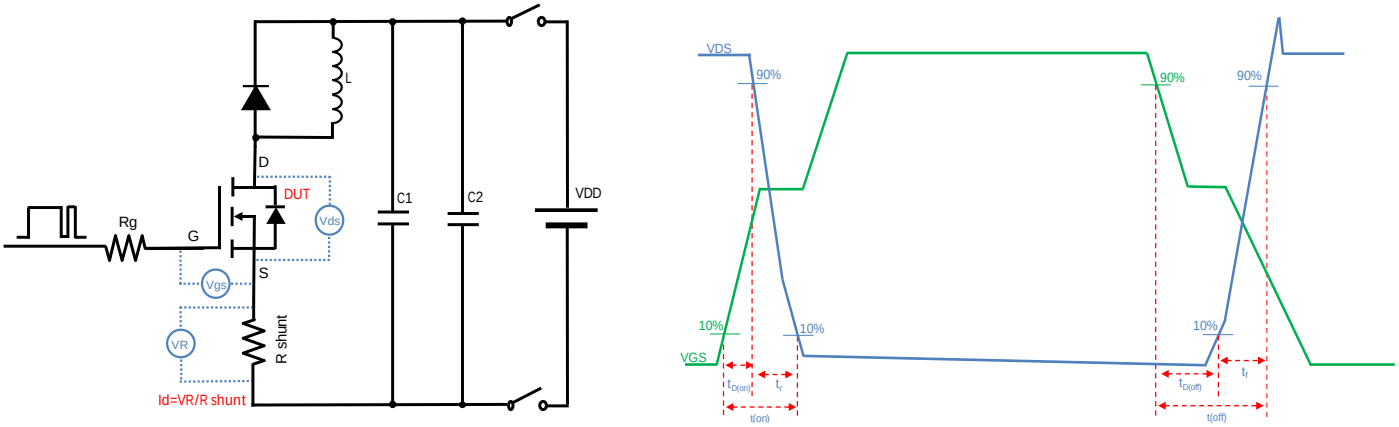


Figure C. Resistive Switching Test Circuit & Waveform

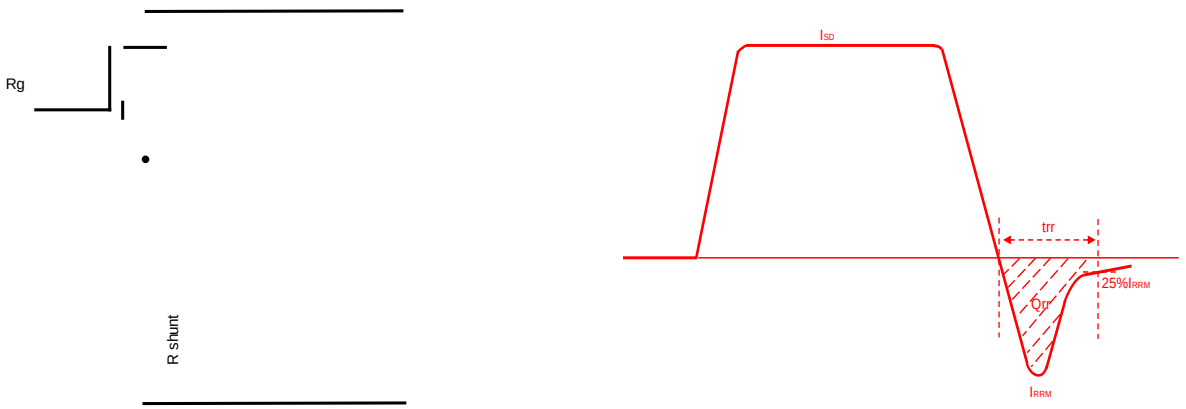
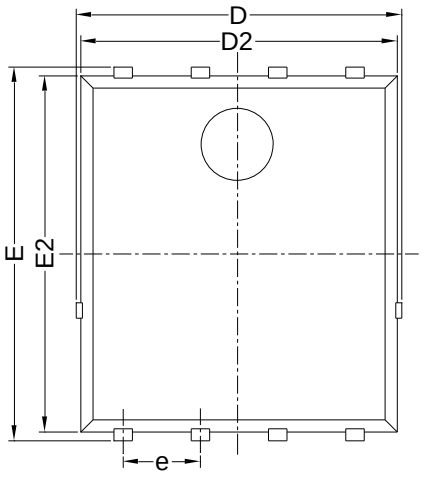
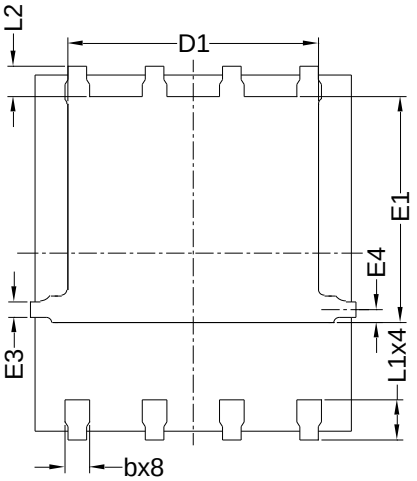


Figure D. Diode Recovery Test Circuit & Waveform

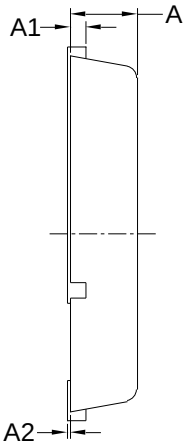
■ PDFN5060-8L-B-1.1MM Package information



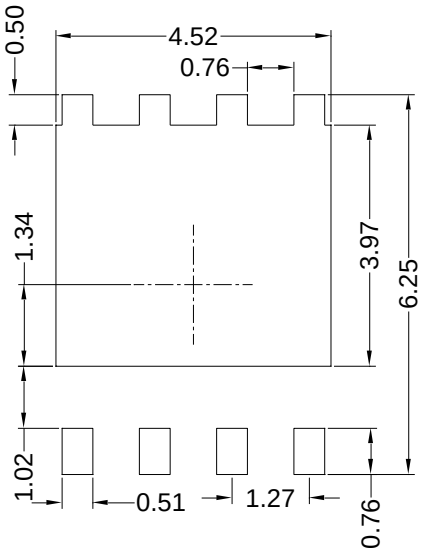
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254 REF	
E4		0.21 REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

Disclaimer

The information presented in this document is for reference only. Yangzhou Yangjie Electronic Technology Co., Ltd. reserves the right to make changes without notice for the s-41(1(e)951.1-3(o)-3(l)9(o)-3(g)-3(y)[-)]TJETQq1743(te(i)-4)9(n)-3(te)-5(d)-g)-3(y)df1(f)11(2(m)6