N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	30V
I_D	55A
$R_{DS(ON)}$(at V_{GS}=10V)	5.5m
$R_{DS(ON)}$(at V_{GS}=4.5V)	12m
100% EAS Tested	
100%	

” DS

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V	-	-	1	
		V_{DS}=30V, V_{GS}=0V, Tj=150℃	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D	1.2	1.7	2.2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=15A	-	4.2	5.5	
		V_{GS}=4.5V, I_D=8A	-	8.2	12	
Diode Forward Voltage	V_{SD}	I_S=15A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	1.2	-	
Maximum Body-Diode Continuous Current	I_S		-	-	55	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, f=1MHz	-	560	-	pF
Output Capacitance	C_{oss}		-	500	-	
Reverse Transfer Capacitance	C_{rss}		-	50	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=15V, I_D=15A	-	12.4	-	nC
Gate-Source Charge	Q_{gs}		-	2	-	

Typical Electrical and Thermal Characteristics Diagrams

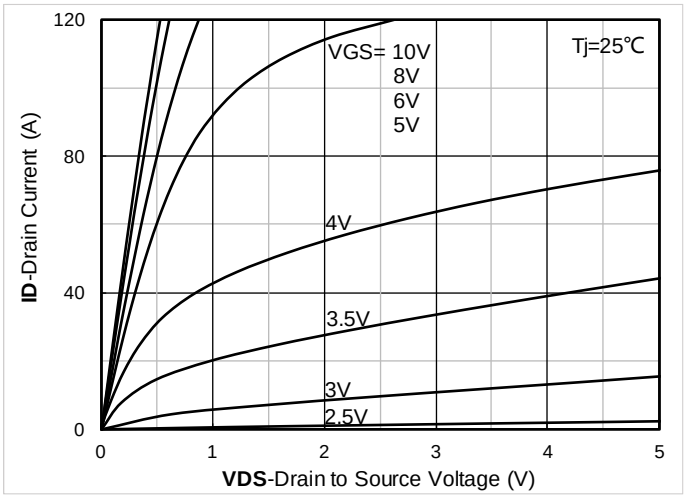


Figure 1. Output Characteristics

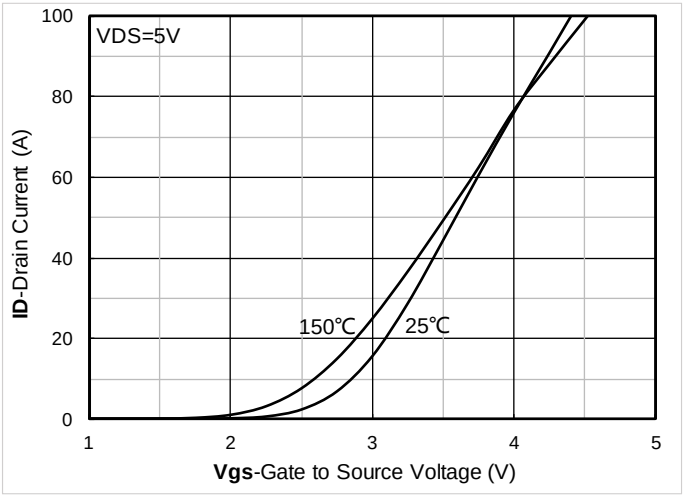


Figure 2. Transfer Characteristics

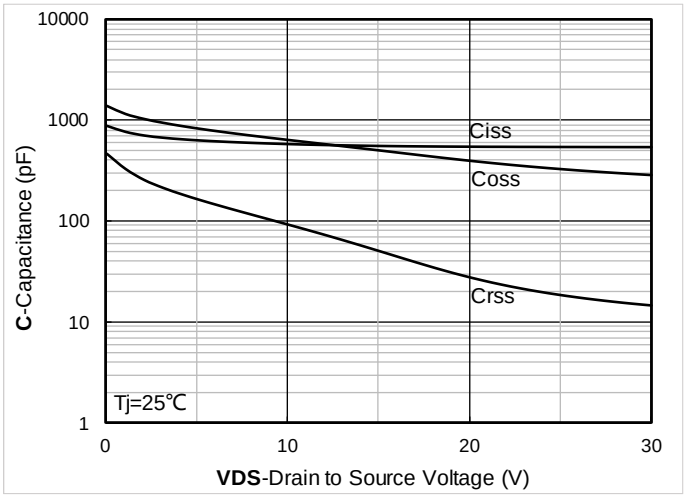


Figure 3. Capacitance Characteristics

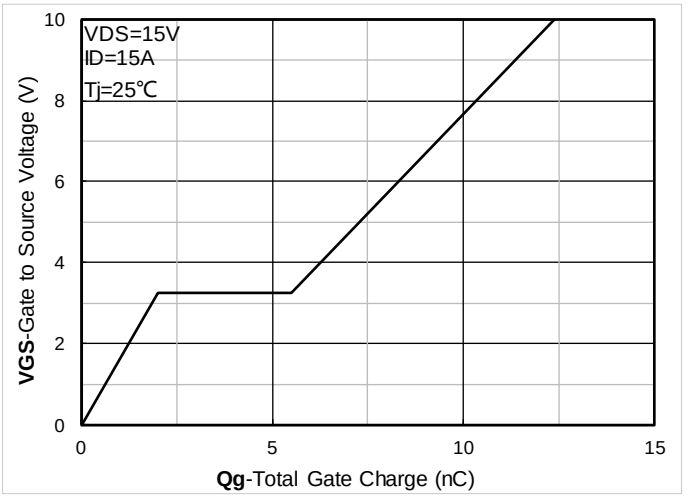


Figure 4. Gate Charge

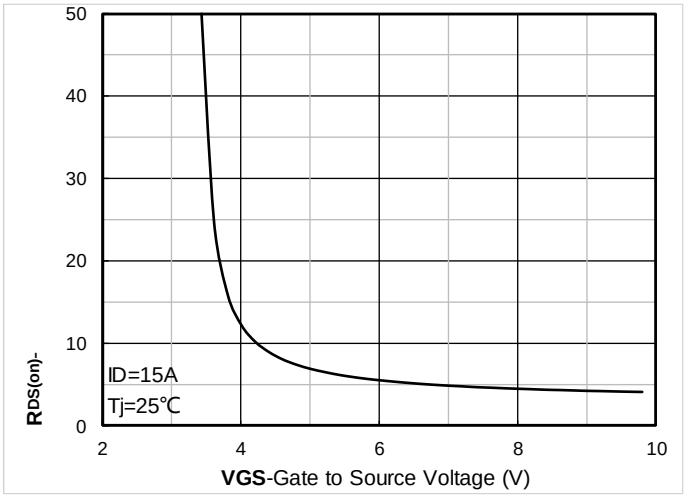


Figure 5. On-Resistance vs Gate to Source Voltage

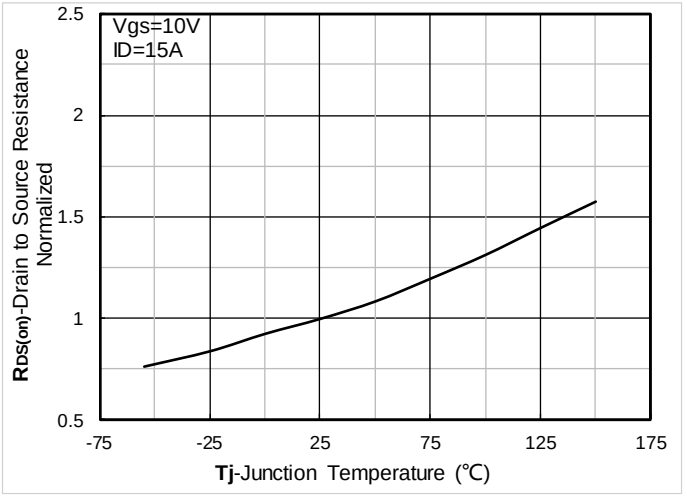


Figure 6. Normalized On-Resistance

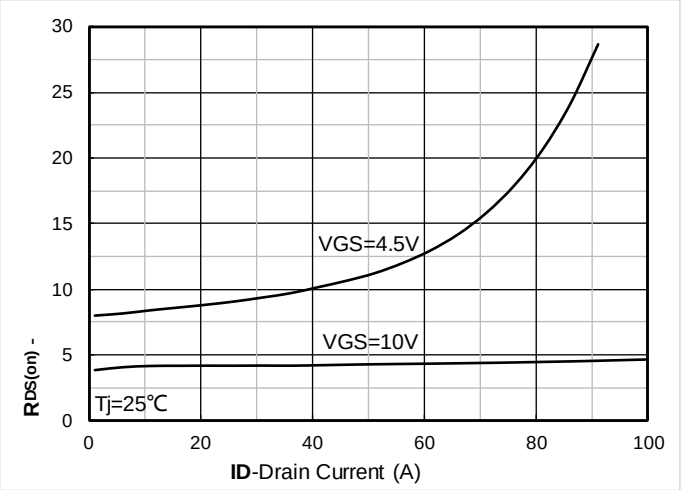


Figure 7. $R_{DS(on)}$ VS Drain Current

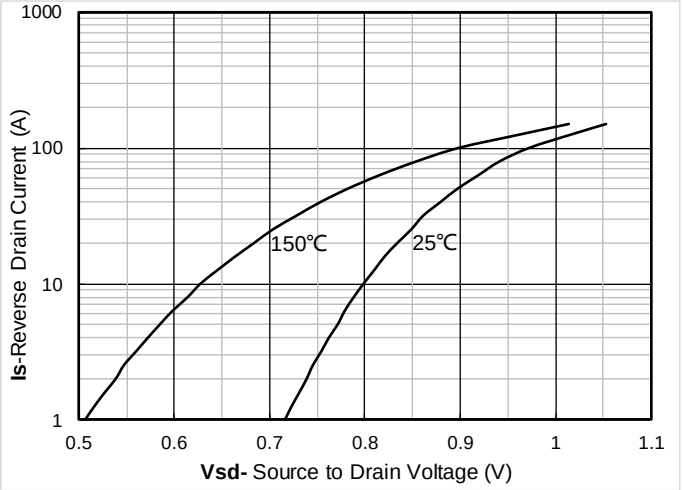


Figure 8. Forward characteristi

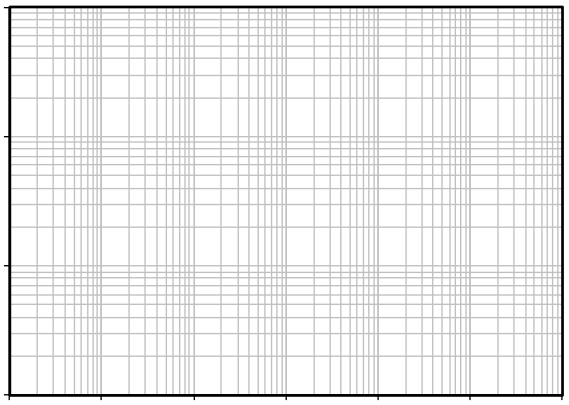


Figure 13. Maximum Transient Thermal Impedance

Figure 14. Safe Operation Area

Test Circuits & Waveforms

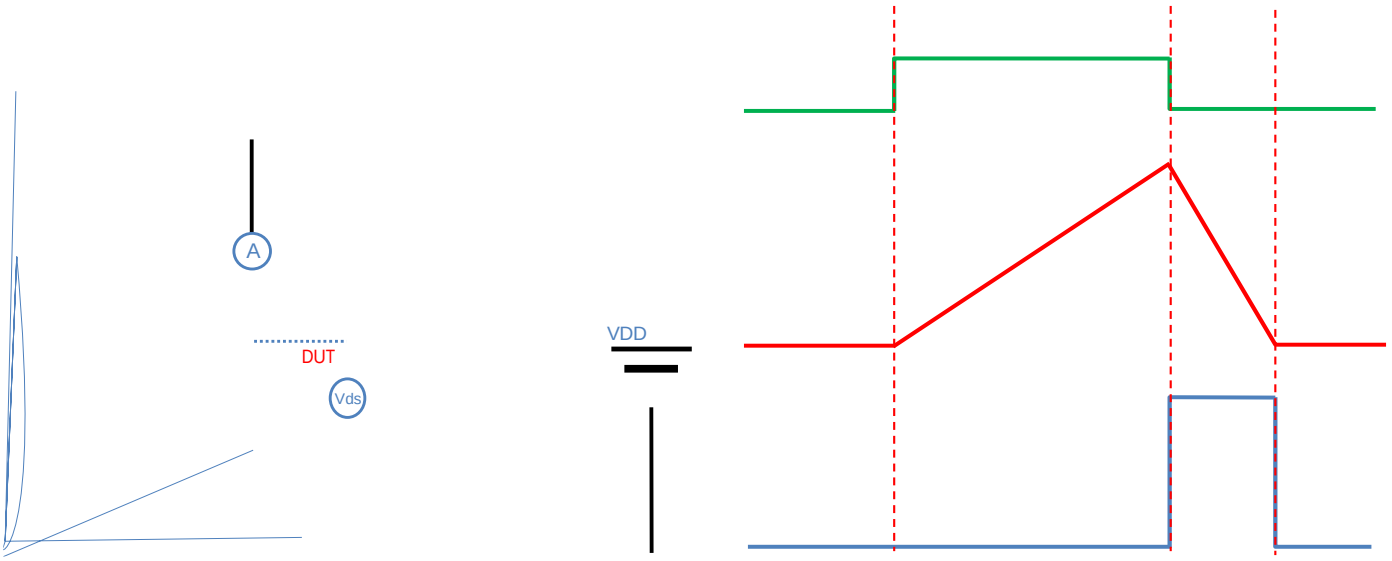


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

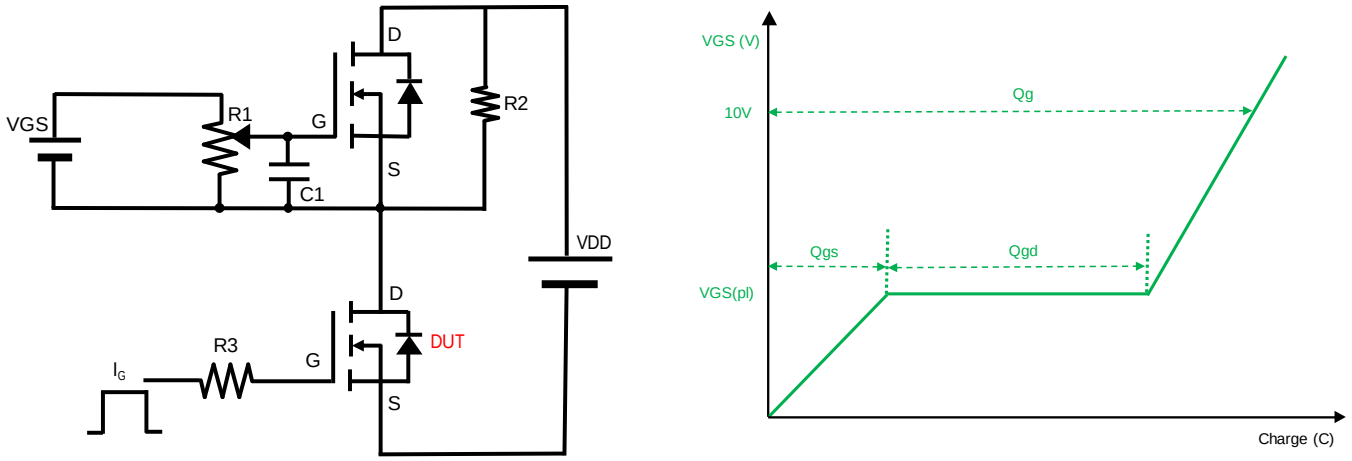


Figure B. Gate Charge Test Circuit & Waveform

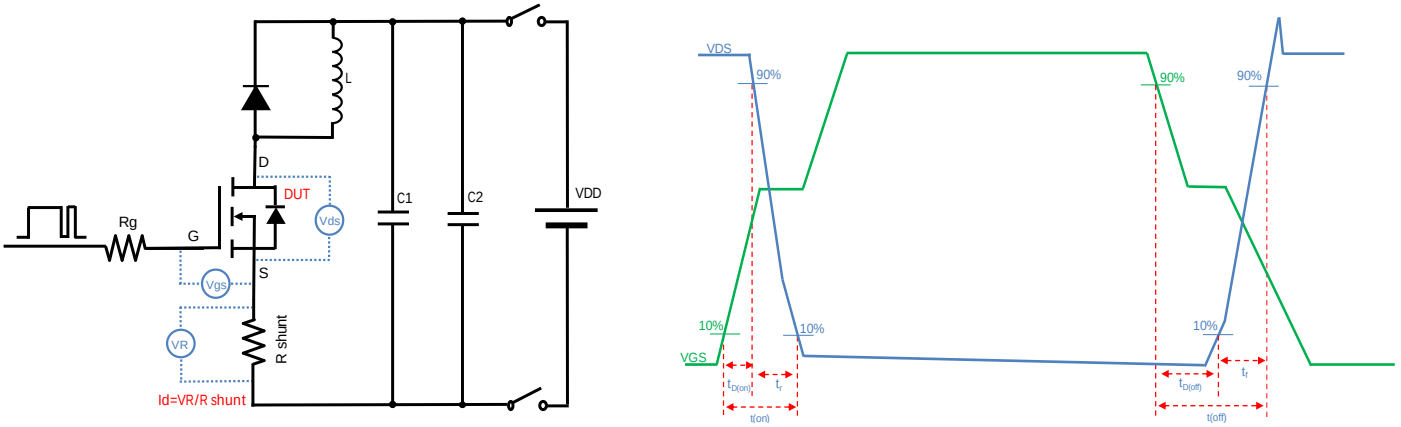


Figure C. Resistive Switching Test Circuit & Waveform

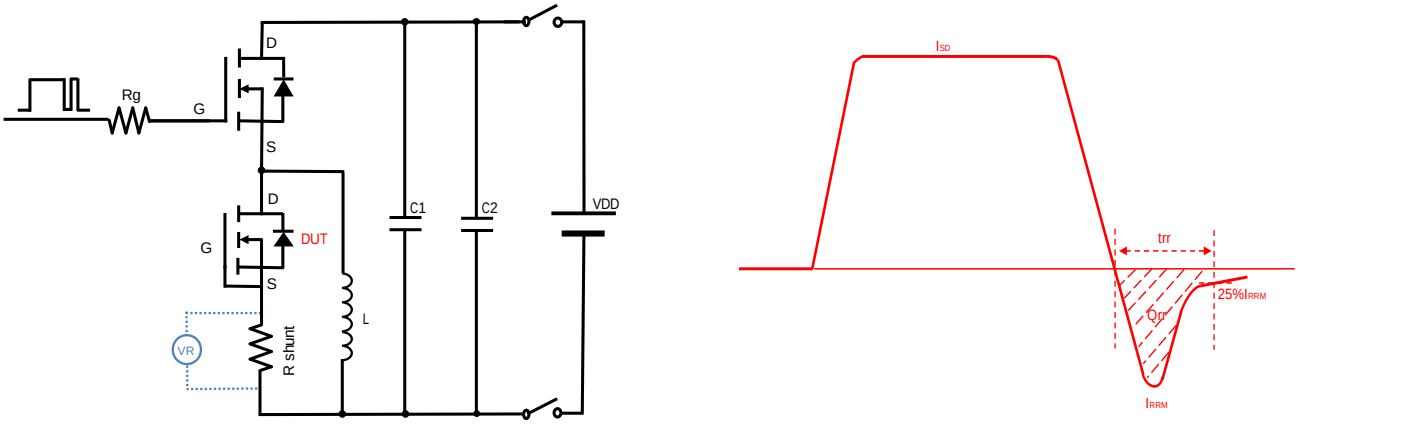
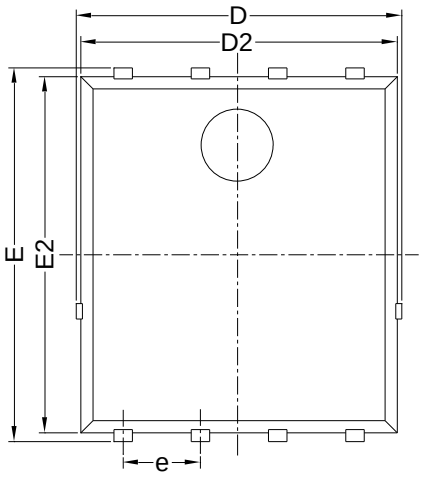
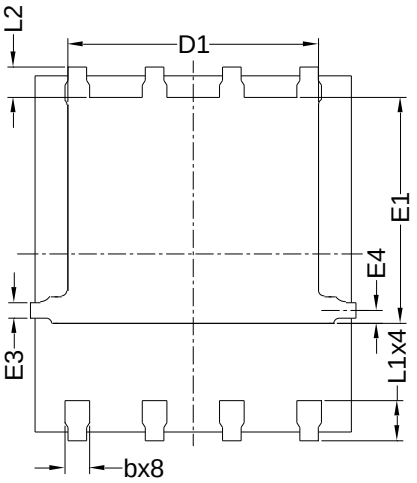


Figure D. Diode Recovery Test Circuit & Waveform

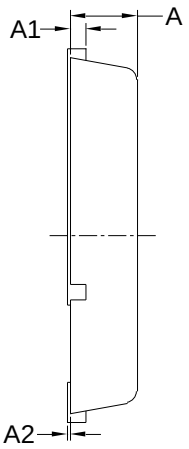
PDFN5060-8L-B-1.1MM Package information



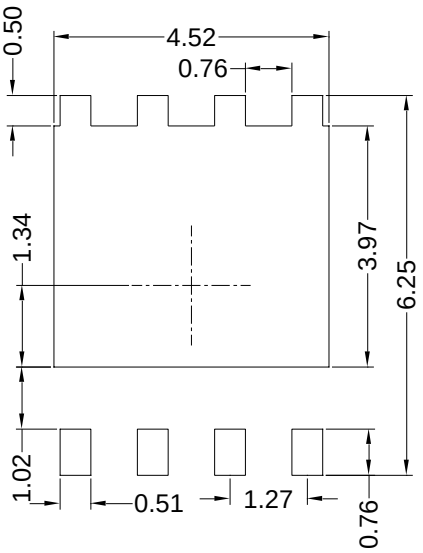
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254 REF	
E4		0.21 REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

Disclaimer