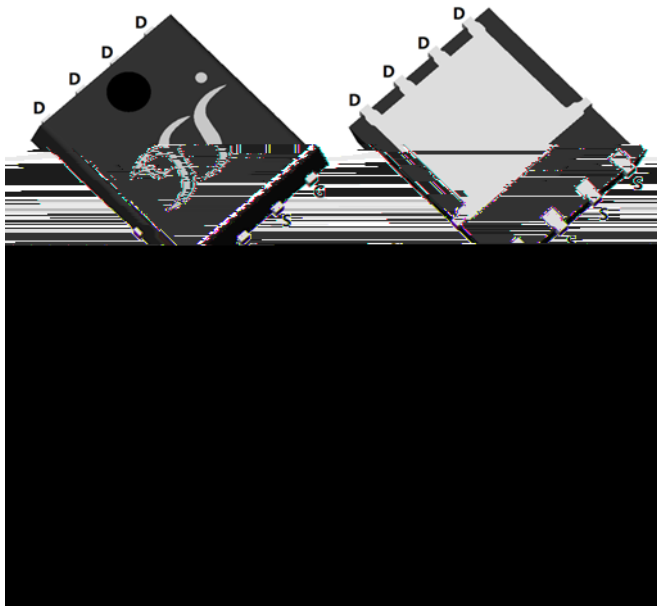




N-Channel Enhancement Mode Field Effect Transistor



Product Summary

V_{DS}	40V
I_D	60A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	6.8m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Split gate trench MOSFET technology
 Excellent package for heat dissipation
 High density cell design for low $R_{DS(ON)}$
 Moisture Sensitivity Level 1
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

Power switching application
 Uninterruptible power supply
 DC-DC convertor

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25$	I_D	14	A
	$T_A=100$		9.5	
	$T_C=25$		60	
	$T_C=100$		42	
Pulsed Drain Current ^A		I_{DM}	240	A
Avalanche energy ^B		EAS	84.5	mJ
Total Power Dissipation ^C	$T_A=25$	P_D	2.7	W
	$T_A=100$		1.3	
	$T_C=25$		75	
	$T_C=100$		37	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +175	

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	R_{JA}	46	55	/W
Thermal Resistance Junction-to-Case	Steady-State	R_{JC}	1.7	2	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG60G04H	F1	YJG60G04H	5000	10000	100000	13" reel

YJG60G04H

$I_D=25$ unless otherwise noted)

Symbol	Conditions	Typ	Max
BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	-	-
I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	1
	$V_{DS}=40V, V_{GS}=0V, T_j=175$	-	100
I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	± 100
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	3	4
$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	5.2	6.8
V_{SD}	$I_S=20A, V_{GS}=0V$	-	1.2
R_G	$f=1MHz$	2	-
I_S		-	60

Dynamic Parameters

Input Capacitance	C_{iss}	-	965	-
Output Capacitance	$C_{osETQq243}$	$V_{DS}=20V, V_{GS}=0V, f=1MHz$		pF



Typical Electrical and Thermal Characteristics Diagrams

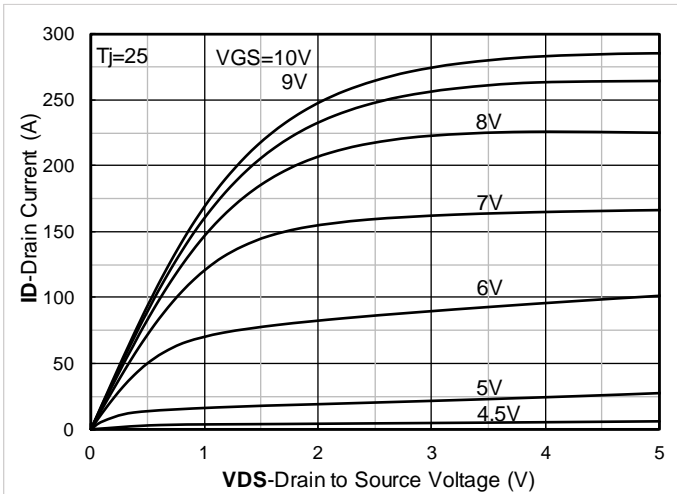


Figure 1. Output Characteristics

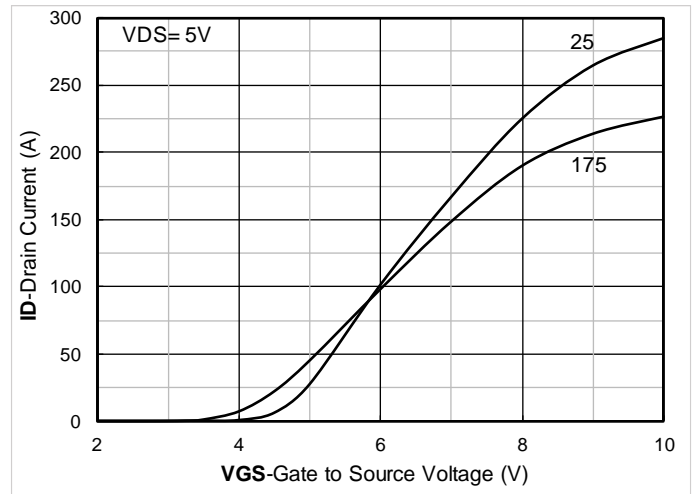


Figure 2. Transfer Characteristics

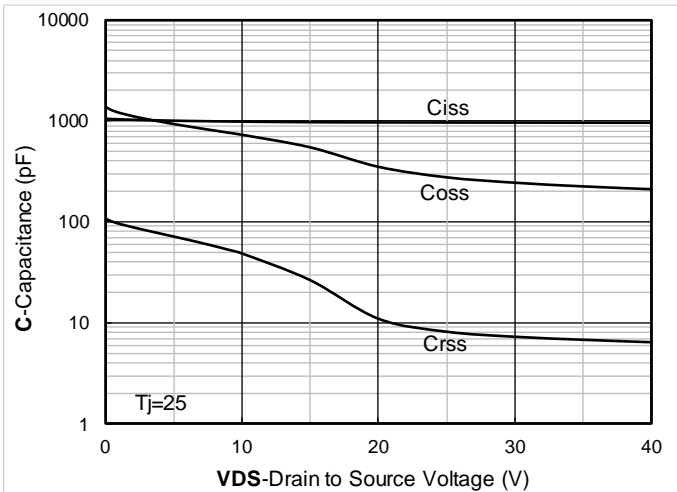


Figure 3. Capacitance Characteristics

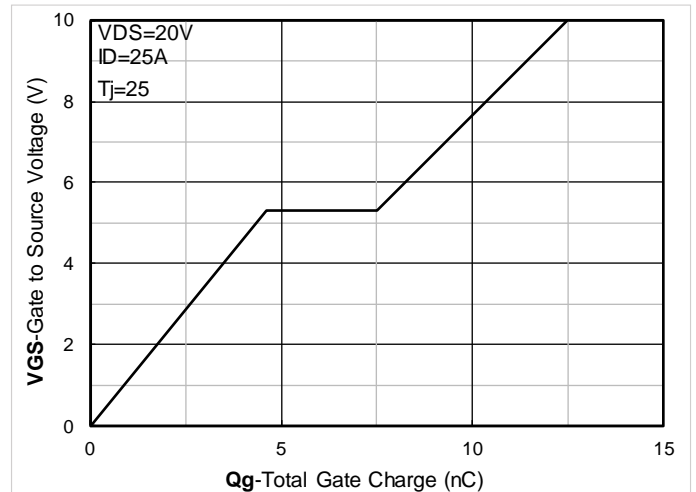


Figure 4. Gate Charge

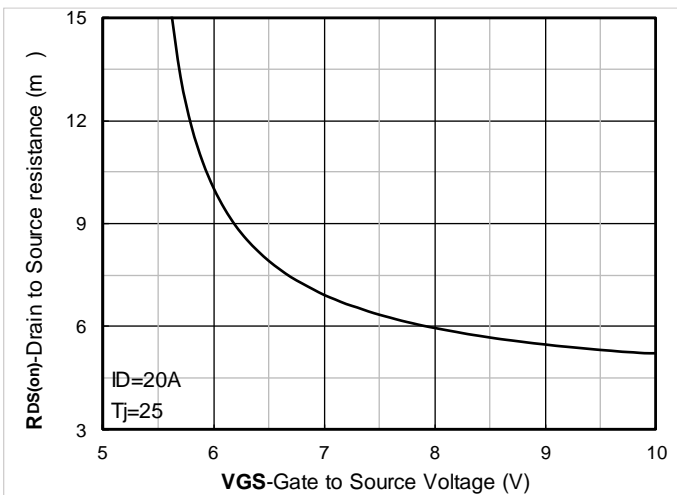


Figure 5. On-Resistance vs Gate to Source Voltage

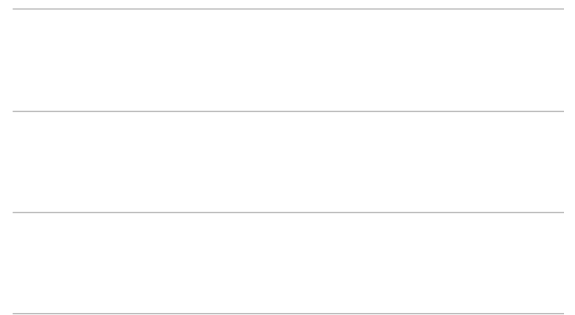


Figure 6. Normalized On-Resistance



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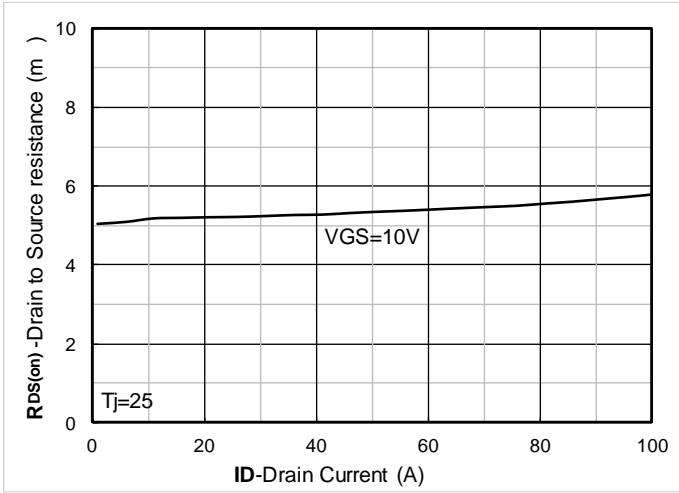


Figure 7. RDS(on) VS Drain Current

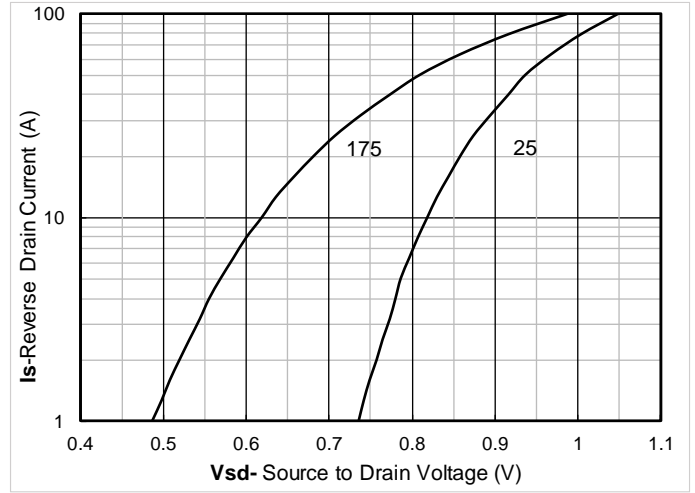


Figure 8. Forward characteristics of reverse diode

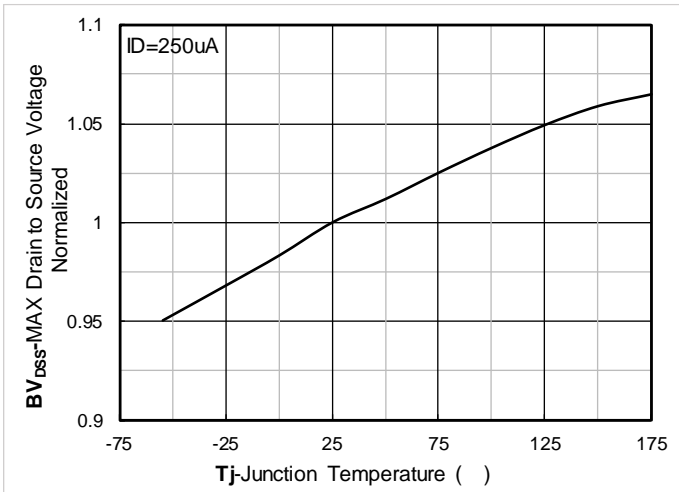


Figure 9. Normalized breakdown voltage

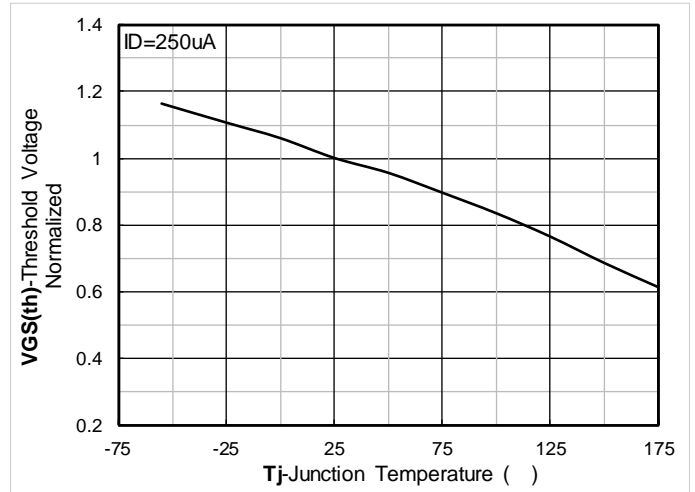


Figure 10. Normalized Threshold voltage

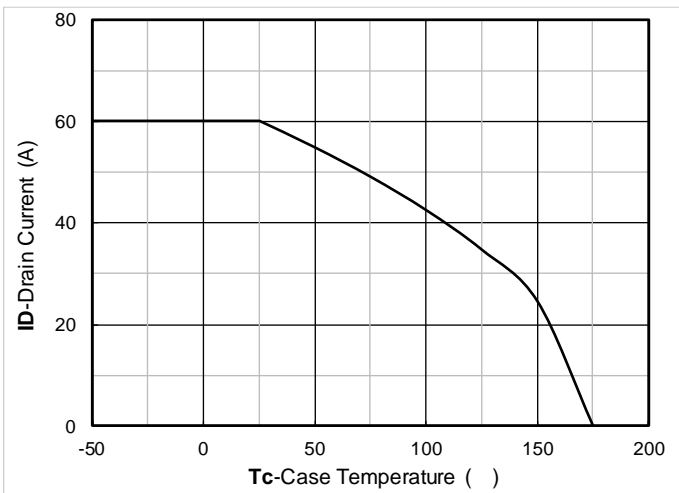


Figure 11. Current dissipation

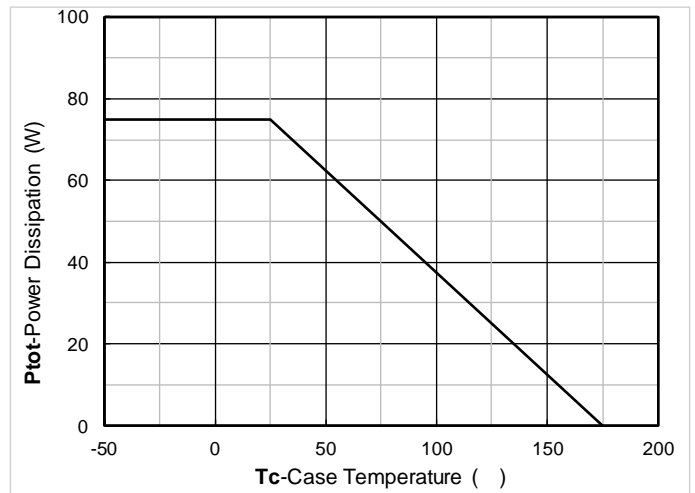


Figure 12. Power dissipation



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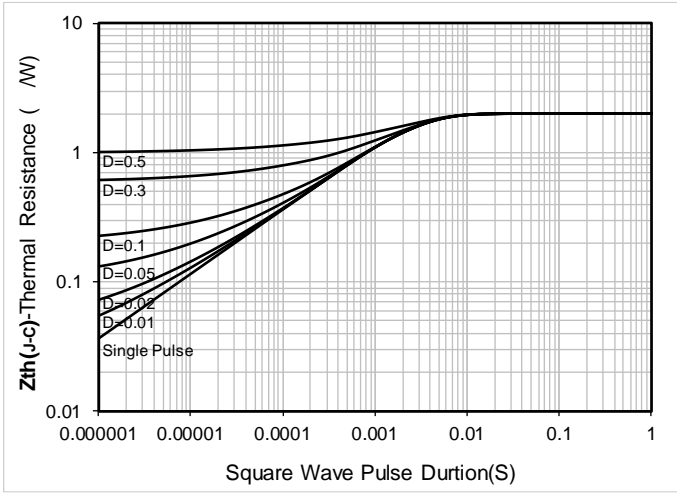


Figure 13. Maximum Transient Thermal Impedance

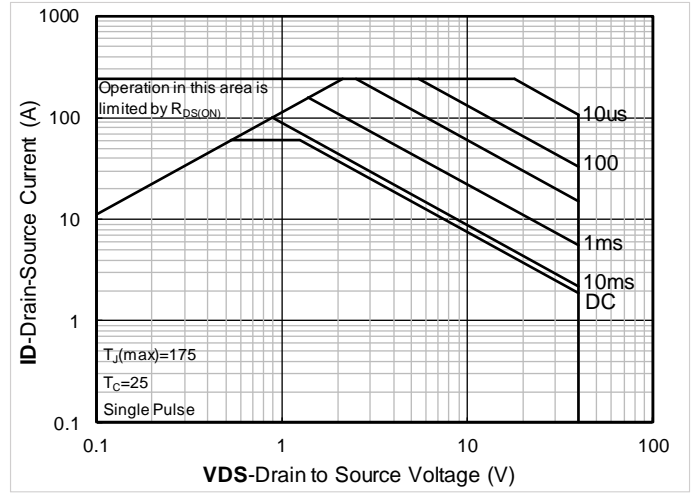


Figure 14. Safe Operation Area

Test Circuits & Waveforms

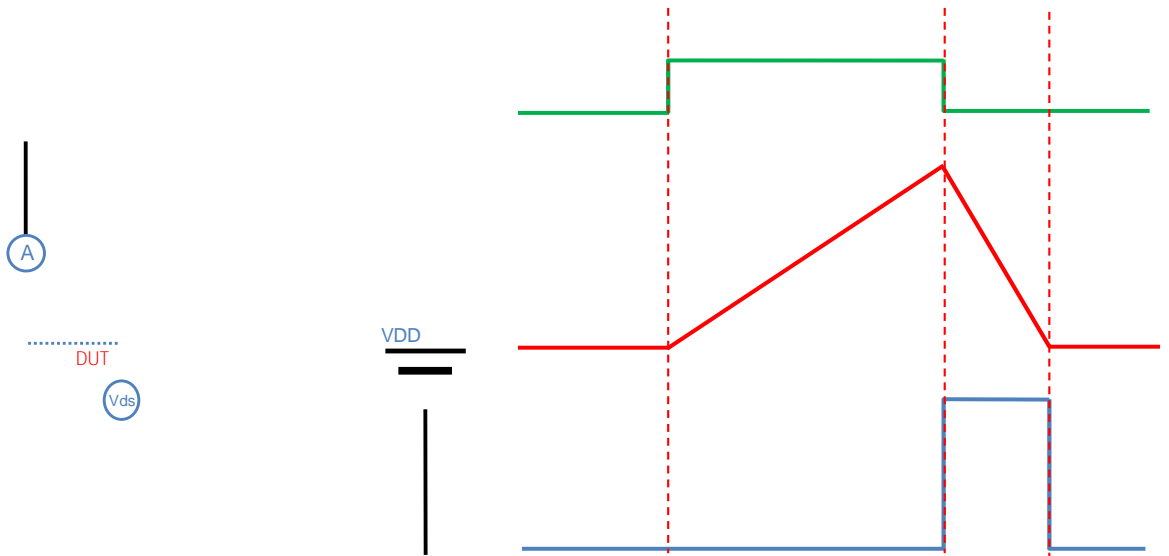


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

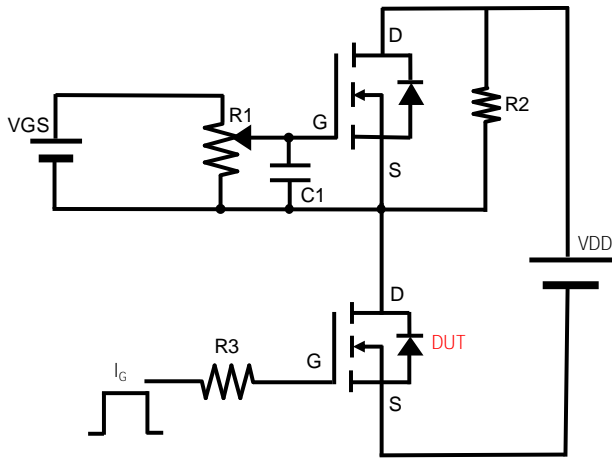


Figure B. Gate Charge Test Circuit & Waveform

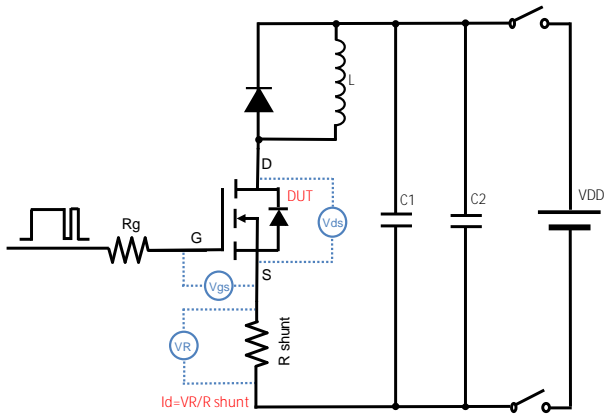


Figure C. Resistive Switching Test Circuit & Waveform

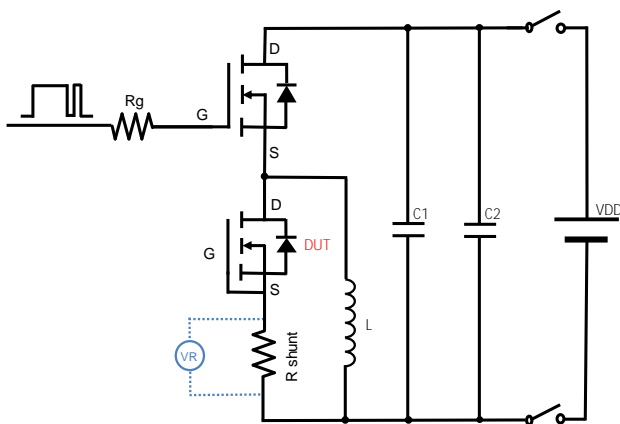
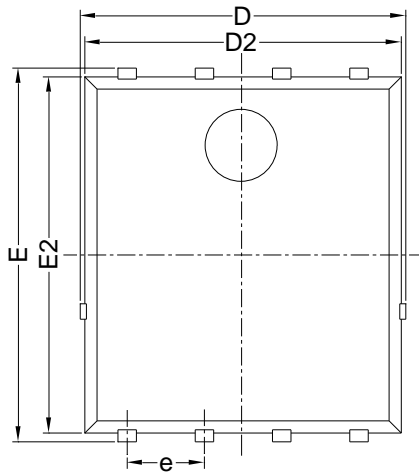


Figure D. Diode Recovery Test Circuit & Waveform

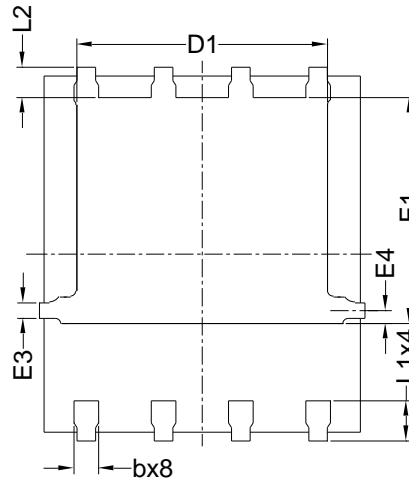


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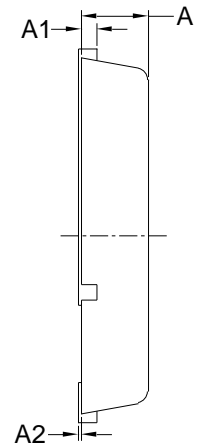
PDFN5060-8L-B-1.1MM Package information



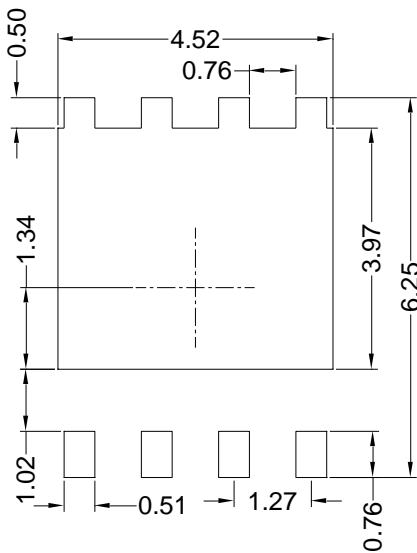
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



YJG60G04H

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