



N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	60V
I_D	70A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	7.5 mohm
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	9.5 mohm
100% EAS Tested	
100% V_{DS} Tested	

General Description

Split Gate Trench MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Moisture Sensitivity Level 1
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

DC-DC Converters
Power management functions
Industrial and Motor Drive application

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current (Silicon limited)	$T_C=25$	I_D	70	A
	$T_C=100$		44	
Pulsed Drain Current ^A		I_{DM}	210	A
Avalanche energy ^B		EAS	162	mJ
Total Power Dissipation ^C	$T_C=25$	P_D	70	W
	$T_C=100$		28	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	

Thermal resistance

Parameter	Symbol
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Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	T _J =25		1	
			T _J =55		5	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ± 20V, V _{DS} =0V			± 100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =20A		5.3	7.5	m
		V _{GS} = 4.5V, I _D =10A		6.9	9.5	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.85	1.3	V
Maximum Body-Diode Continuous Current	I _S				70	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =35V, V _{GS} =0V, f=1MHZ		2000		pF
Output Capacitance	C _{oss}			390		
Reverse Transfer Capacitance	C _{rss}			13		
Gate Resistance	R _g	f=1MHZ		1.6		



Typical Performance Characteristics

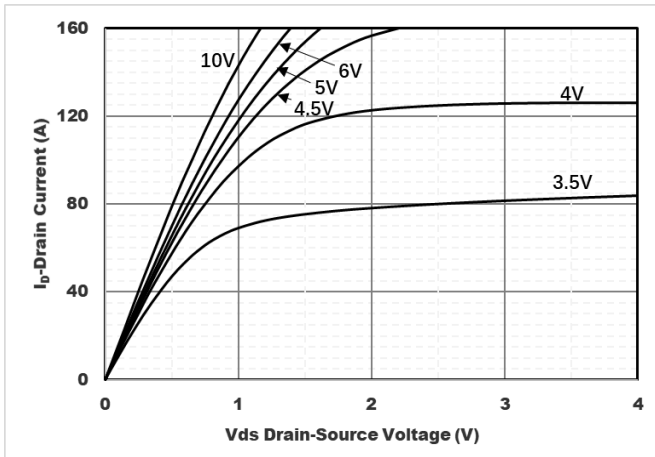


Figure1. Output Characteristics

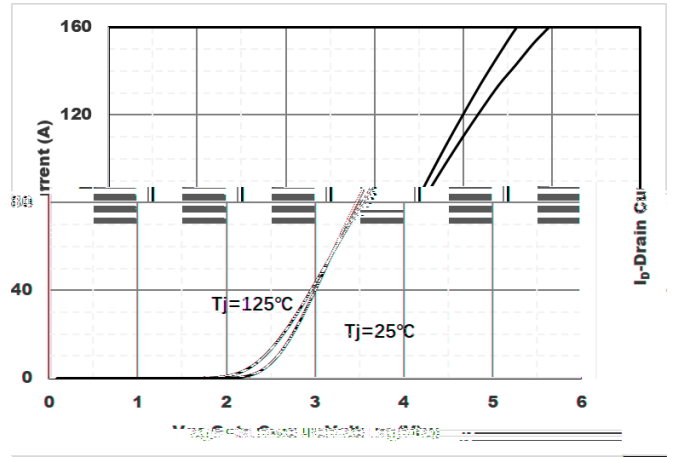


Figure2. Transfer Characteristics

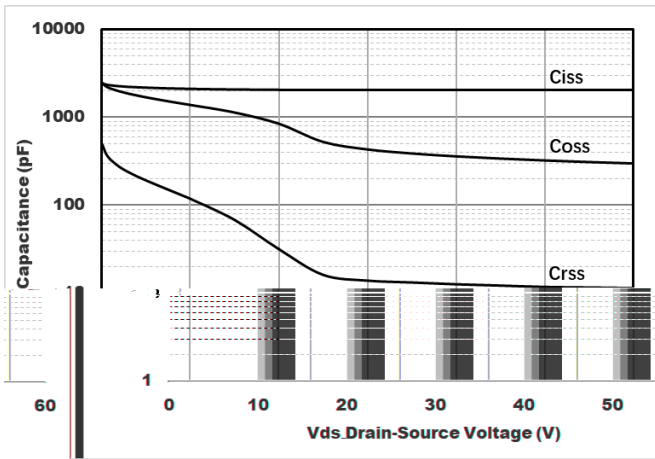


Figure3. Capacitance Characteristics

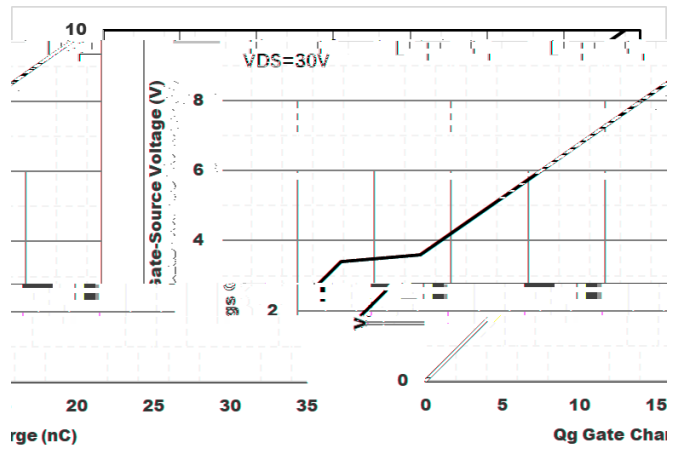


Figure4. Gate Charge

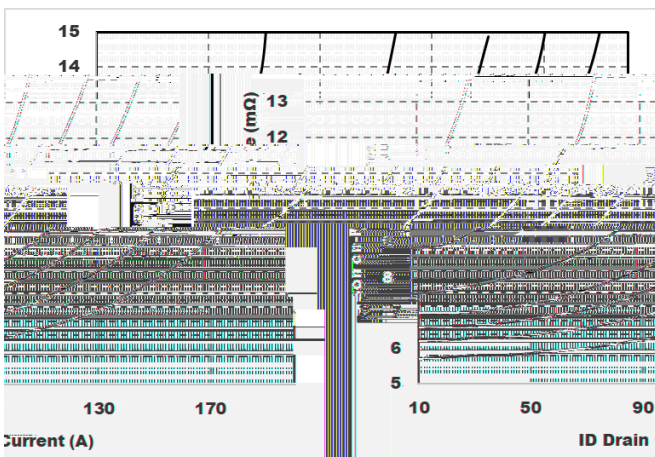


Figure5. Drain-Source on Resistance

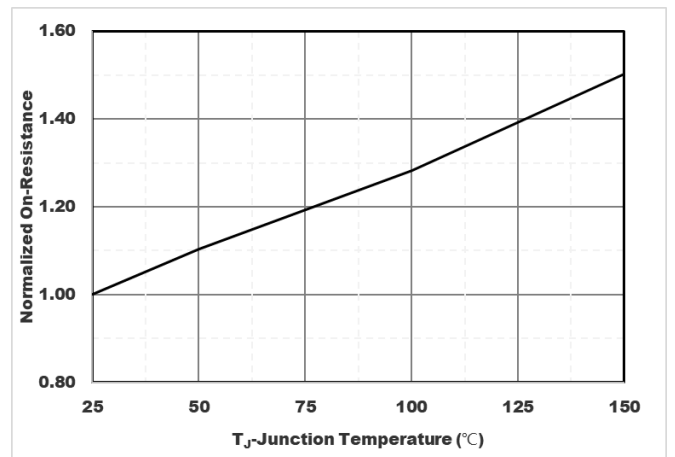


Figure6. Normalized On-Resistance



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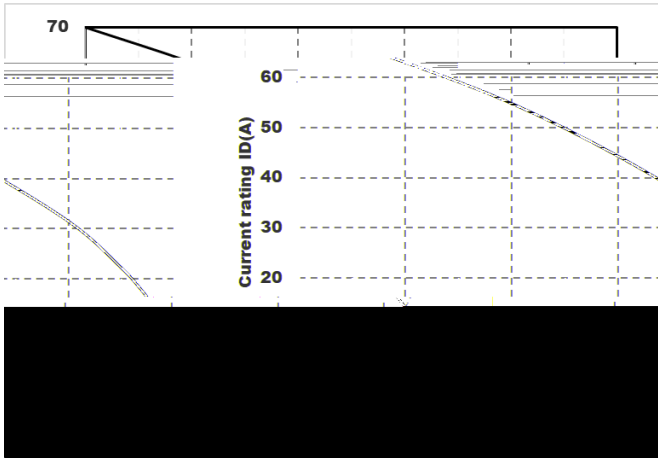


Figure7. Drain current

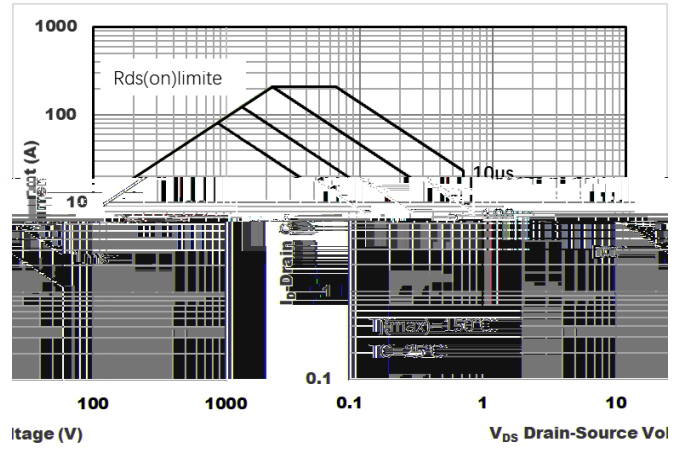


Figure8. Safe Operation Area

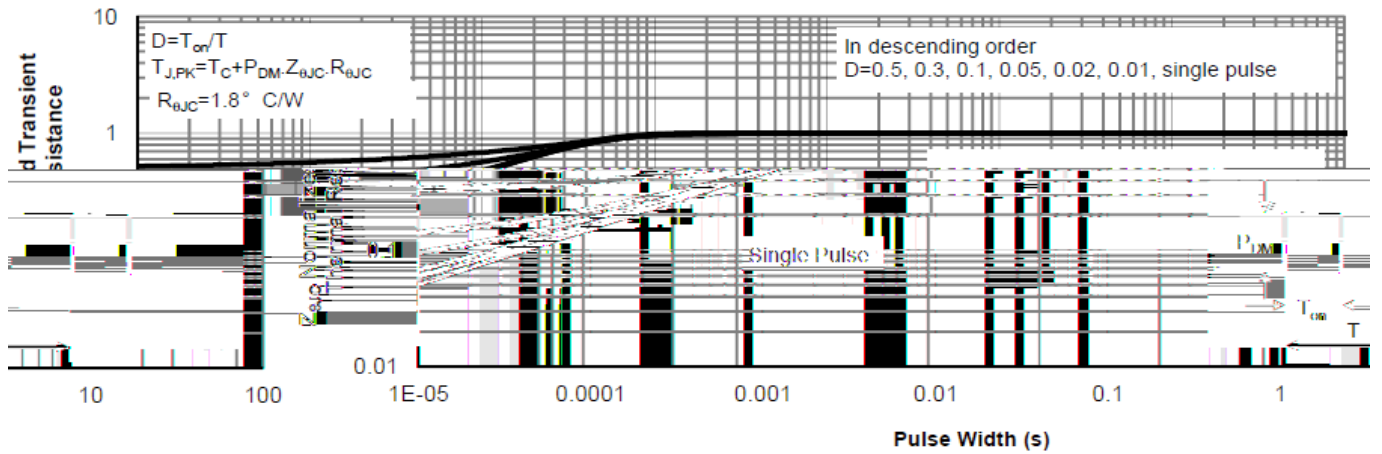
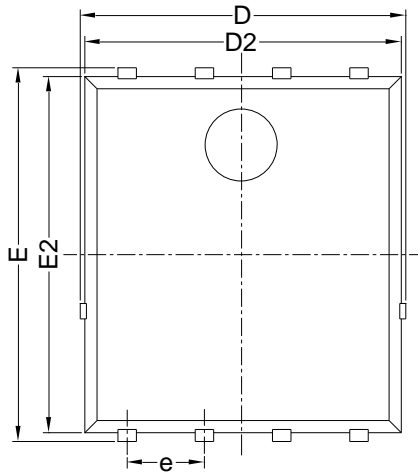


Figure8. Normalized Maximum Transient Thermal Impedance

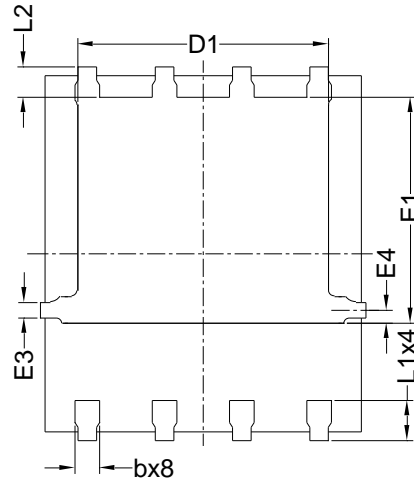


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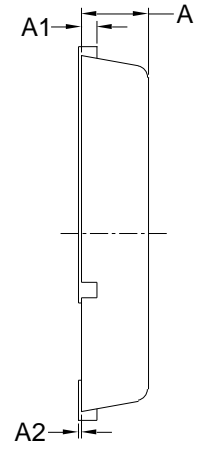
PDFN5060-8L-B-1.1MM Package information



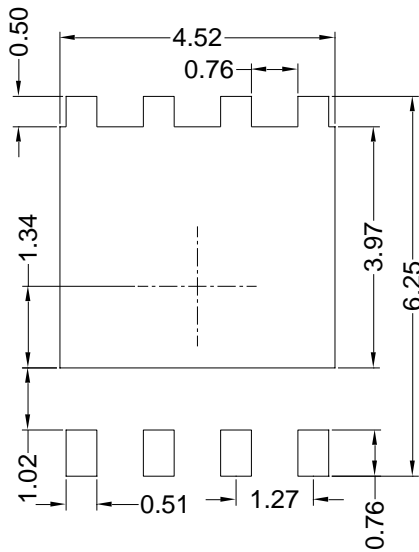
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



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