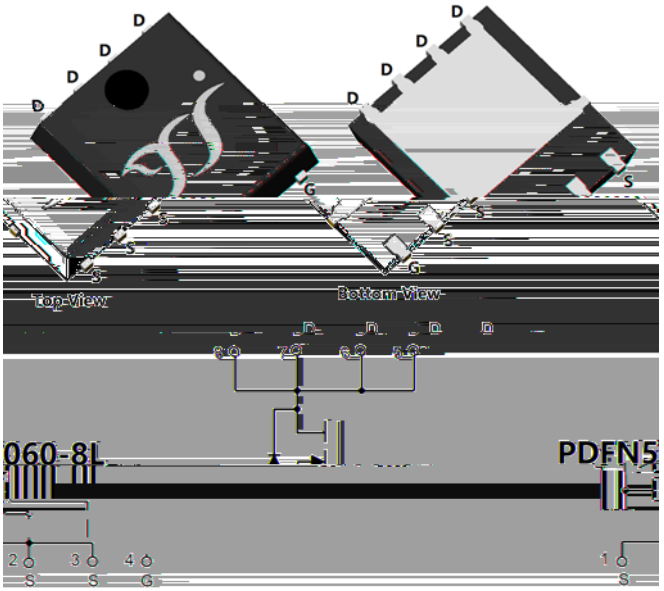
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

V_{DS}	60V
I_D	80A
$R_{DS(ON)}$(at V_{GS}=10V)	4.2 mohm
$R_{DS(ON)}$(at V_{GS}=4.5V)	5.2 mohm

100% EAS Tested

100% V_{DS} Tested

General Description

Split Gate Trench MOSFET technology

Excellent package for heat dissipation

High density cell design for low $R_{DS(ON)}$

Moisture Sensitivity Level 1

Epoxy Meets UL 94 V-0 Flammability Rating

Halogen Free

Applications

DC-DC Converters

Power management functions

Industrial and Motor Drive application

Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current (Silicon limited)	Tc=25	I_D	80	A
	Tc=100		50	
Pulsed Drain Current [A]		I_{DM}	320	A
Avalanche energy [B]		E_{AS}	400	mJ
Total Power Dissipation [C]	Tc=25	P_D	96	W
	Tc=100		38.4	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +150	

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	t ≤ 10S	R	15	20	/W
Thermal Resistance Junction-to-Ambient [D]	Steady-State		45	55	
Thermal Resistance Junction-to-Case	Steady-State	R	1.0	1.3	

Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG80G06B	F1	YJG80G06B	5000	10000	100000	13 reel

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250		60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	T_J=25			1	
			T_J=55			5	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ± 20V, V_{DS}=0V				± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250		1.2	1.7	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=20A			3.0	4.2	m
		V_{GS}= 4.5V, I_D=10A			3.9	5.2	
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			0.85	1.3	V
Maximum Body-Diode Continuous Current	I_S					80	A
Dynamic Parameters							
Input Capacitance	C_{iss}	V_{DS}=35V,V_{GS}=0V,f=1MHZ			4000		pF
Output Capacitance	C_{oss}				780		
Reverse Transfer Capacitance	C_{rss}				26		
Gate Resistance	R_g	f=1MHZ			0.8		
Switching Parameters							
Total Gate Charge	Q_g(10V)				66		
Total Gate Charge	Q_g(5ng (48	V_{DS}=30V,I_D=20A					nC

Typical Performance Characteristics

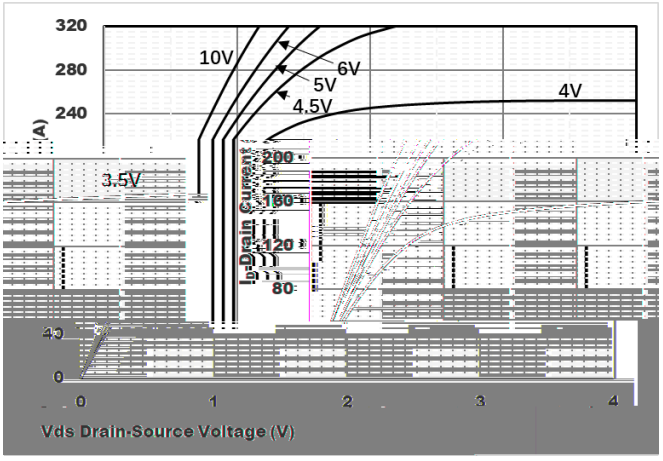


Figure1. Output Characteristics

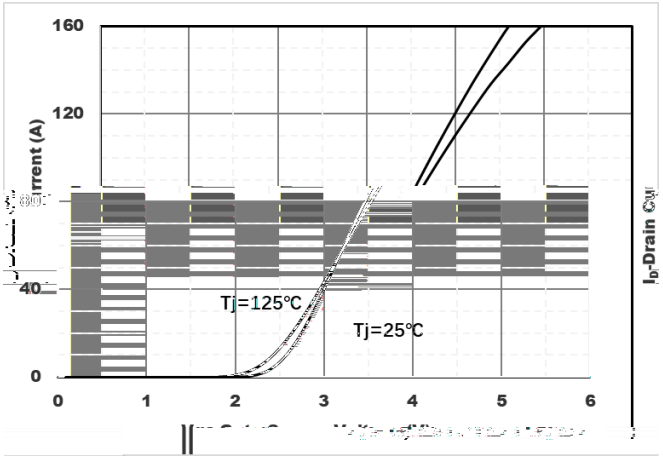


Figure2. Transfer Characteristics

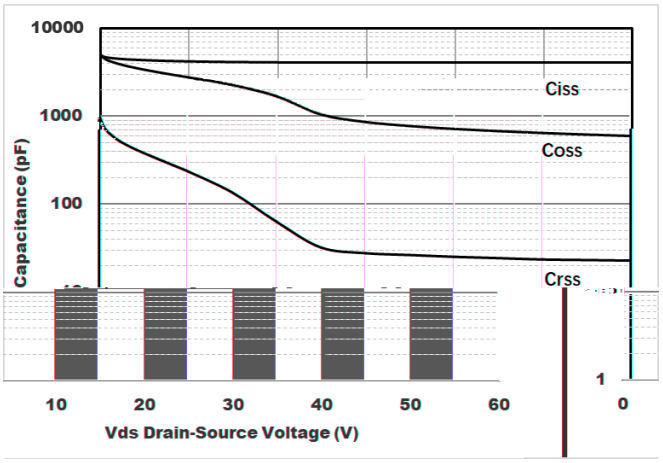


Figure3. Capacitance Characteristics

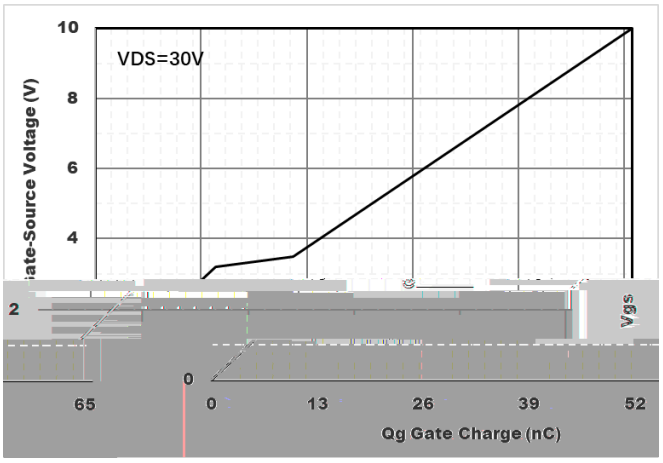


Figure4. Gate Charge

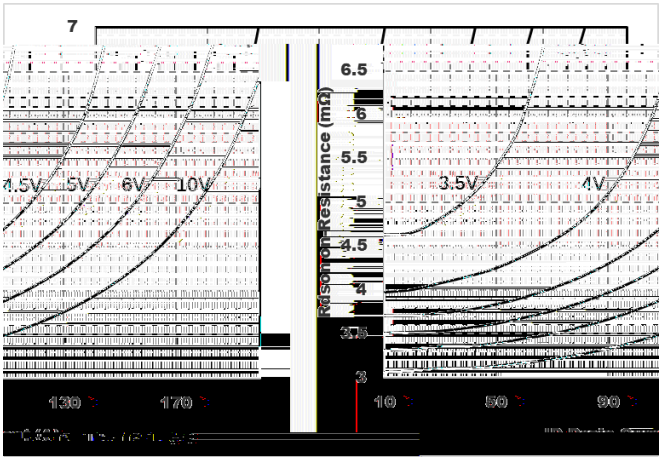


Figure5. Drain-Source on Resistance

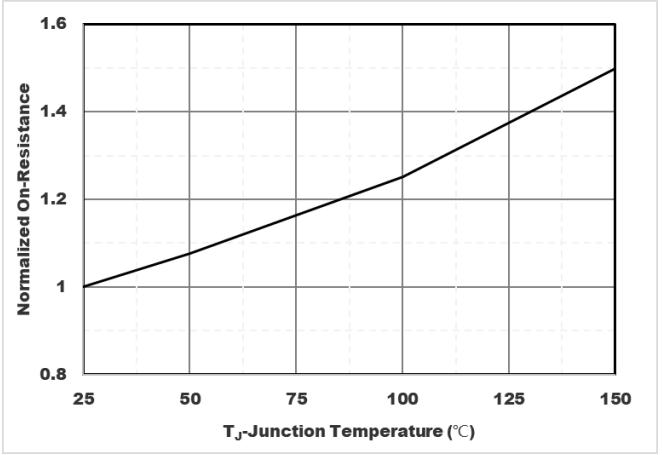


Figure6. Normalized On-Resistance

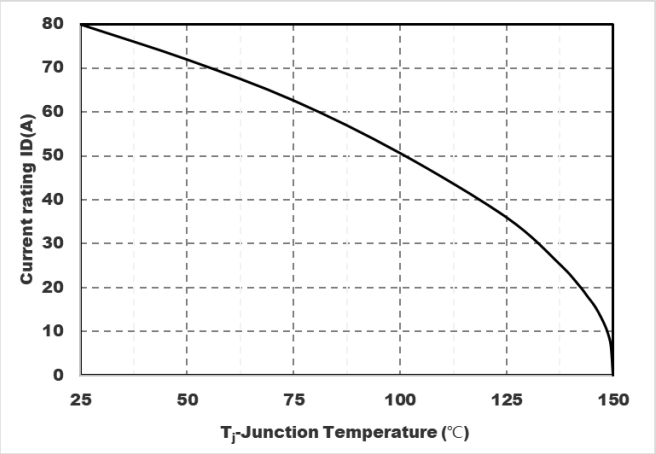


Figure7. Drain current

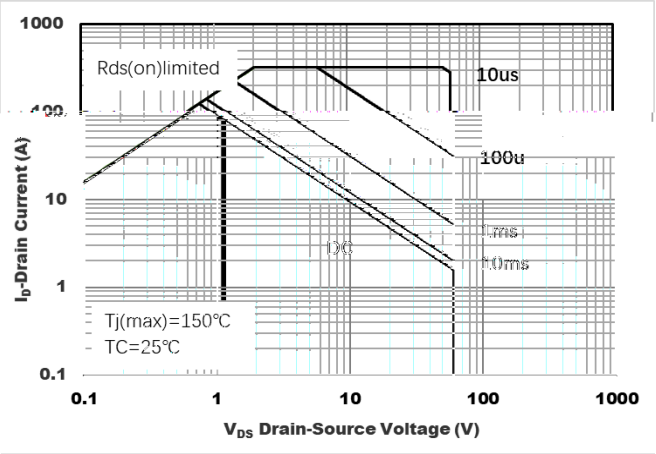


Figure8. Normalized Maximum Transient Thermal Impedance

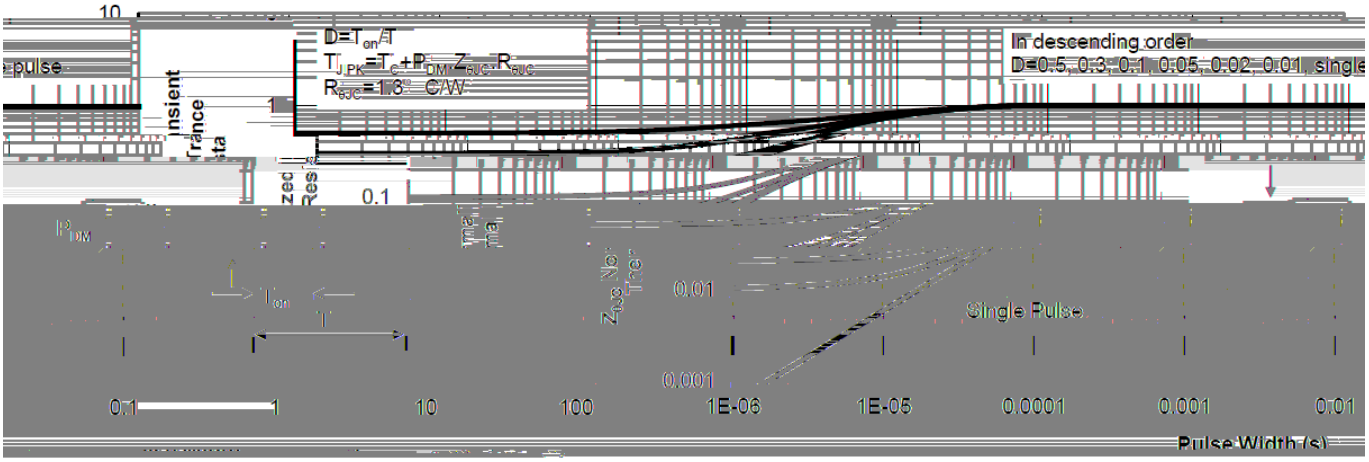
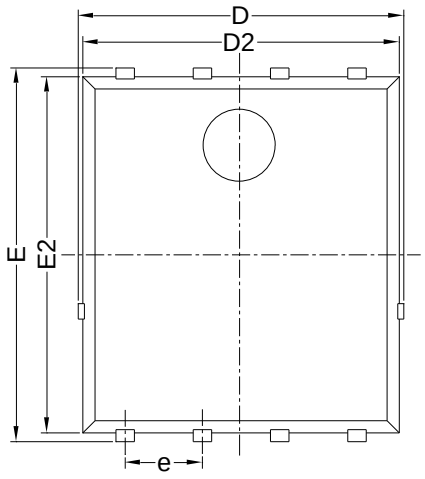
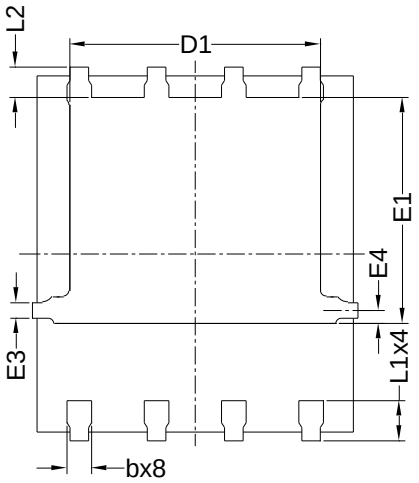


Figure8. Normalized Maximum Transient Thermal Impedance

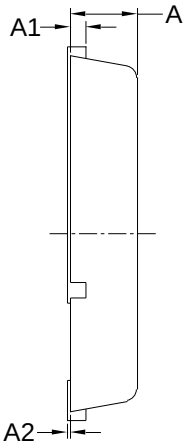
PDFN5060-8L-B-1.1MM Package information



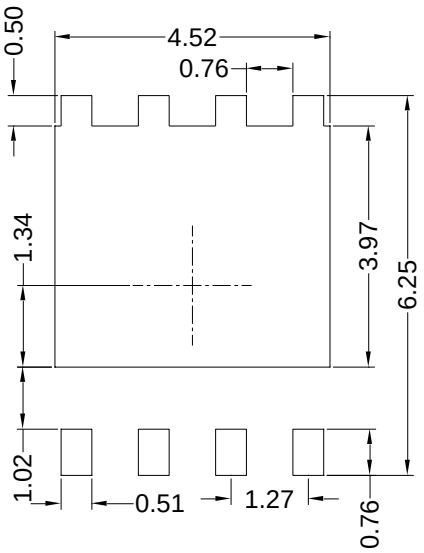
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254 REF	
E4		0.21 REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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