N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	120V
I_D	88A
$R_{DS(ON)}$(at V_{GS}=10V)	7.6mohm
$R_{DS(ON)}$(at V_{GS}=4.5V)	9.6mohm

100% EAS Tested

100% ▽VDS Tested

General Description

Split gate trench MOSFET technology

Excellent package for heat dissipation

High density cell design for low $R_{DS(ON)}$

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Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D	120	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=120V,V_{GS}=0V	-	-	1	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D	1.0	2.0	3.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	6.4	7.6	
		V_{GS}=4.5V, I_D=20A	-	7.6	9.6	
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V	-	-	1.3	V
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=20A	-	80	-	S
Gate resistance	R_G	f=1MHz	-	0.9	-	
Maximum Body-Diode Continuous Current	I_S		-	-	88	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHZ	-	4619	-	pF
Output Capacitance	C_{oss}		-	924	-	
Reverse Transfer Capacitance	C_{rss}		-	28	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=20A	-	72.0	-	nC
Gate-Source Charge	Q_{gs}		-	19.5	-	
Gate-Drain Charge	Q_{gd}		-	8.2	-	
Reverse Recovery Chrage	Q_{rr}	I_F=20A, di/dt=100A/us	-	195	-	
Reverse Recovery Time	t_{rr}		-	86	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=50V,I_D=20A R_{GEN}=2.2	-	19	-	
Turn-on Rise Time	t_r		-	36	-	
Turn-off Delay Time	$t_{D(off)}$		-	45	-	
Turn-off fall Time	t_f		-	45	-	

rr

Typical Performance Characteristics

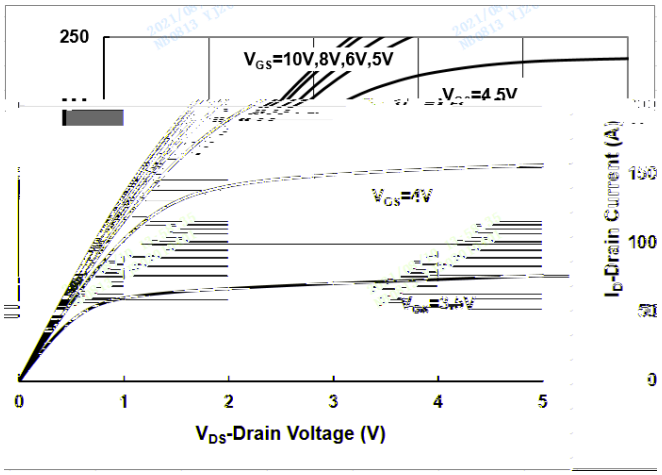


Figure1. Output Characteristics

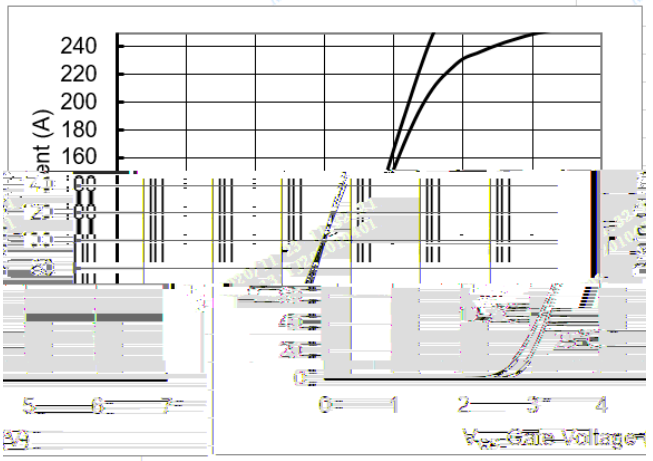


Figure2. Transfer Characteristics

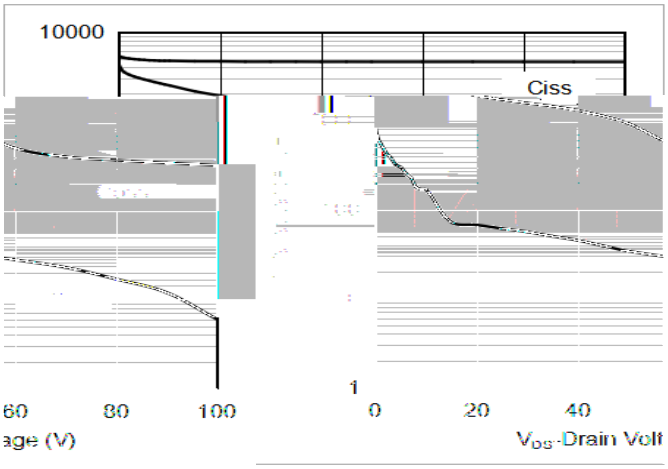


Figure3. Capacitance Characteristics

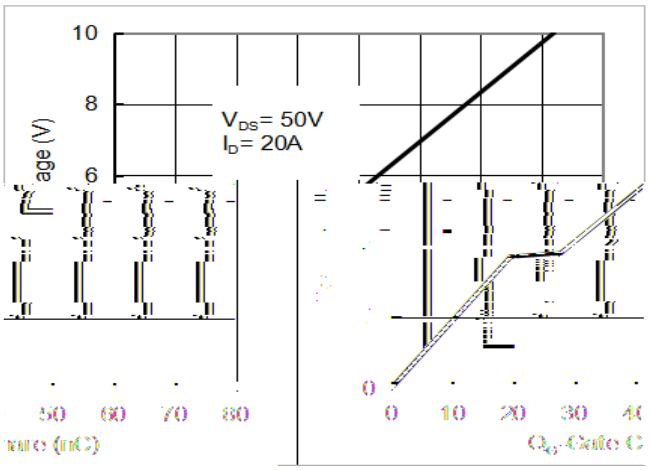


Figure4. Gate Charge

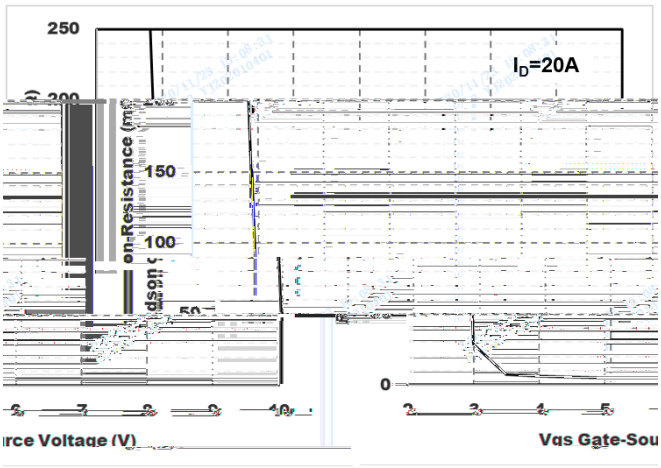


Figure5. **:** On-Resistance vs. Gate to Source Voltage

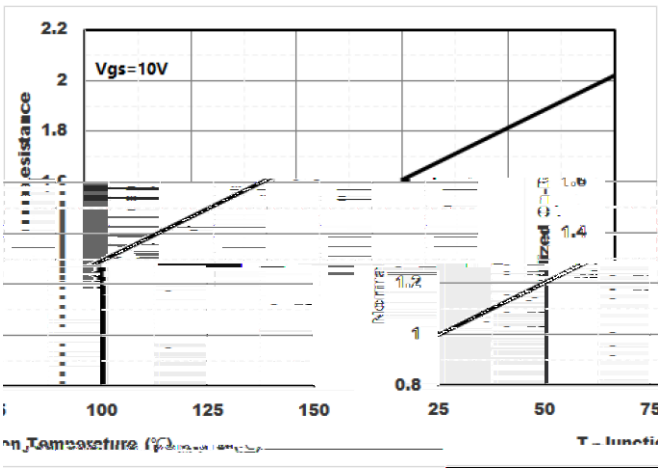


Figure6.Normalized On-Resistance

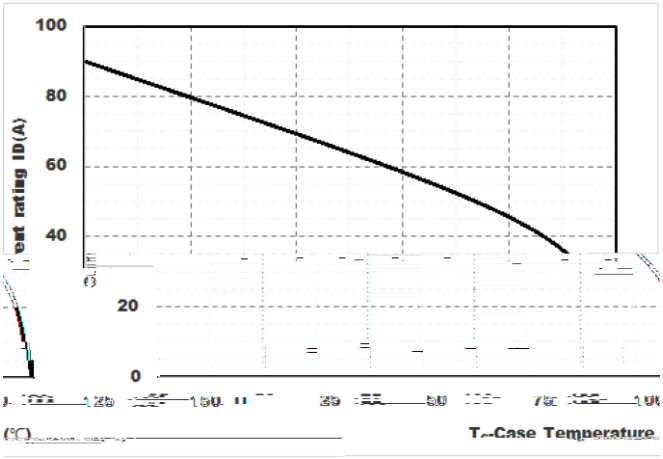


Figure7. Drain current

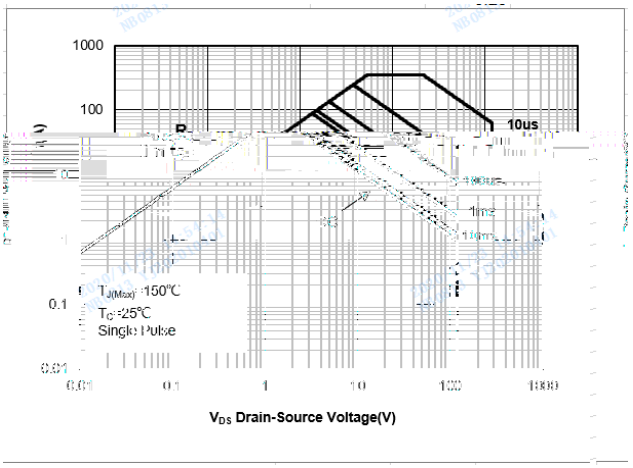


Figure8.Safe Operation Area

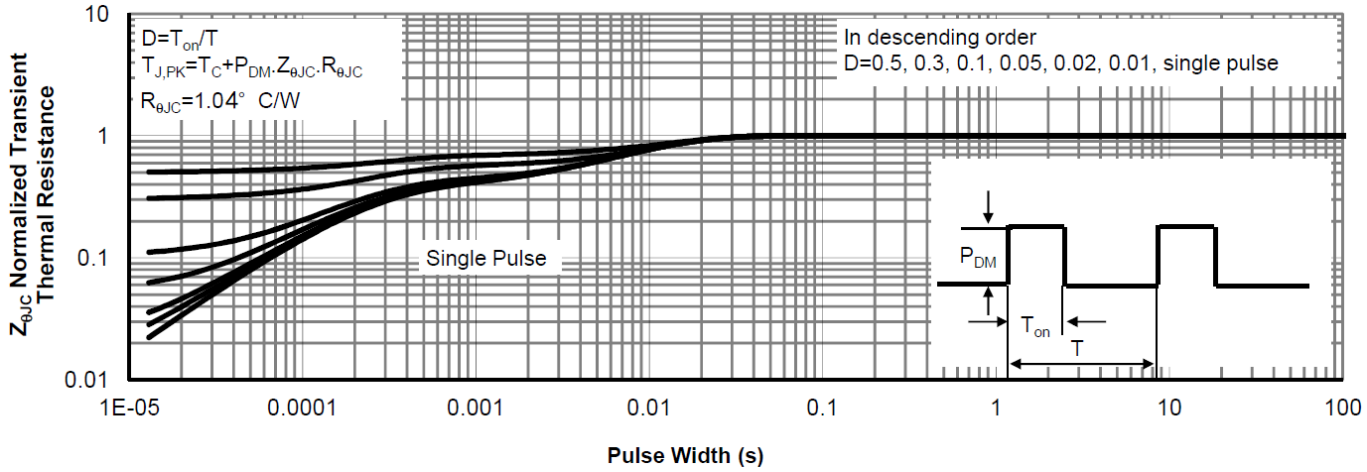
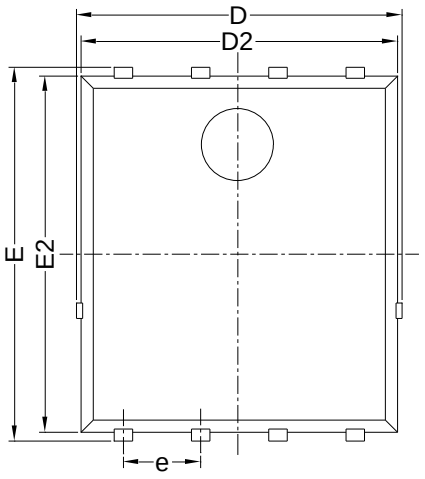
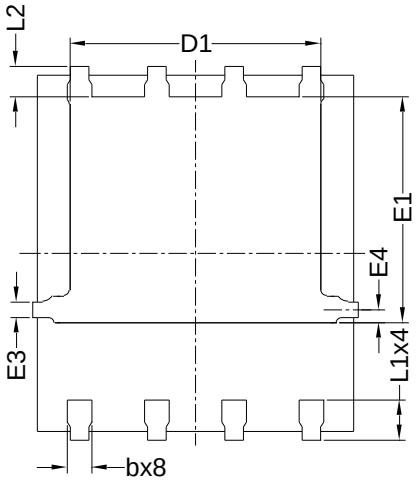


Figure9. Normalized Maximum Transient thermal impedance

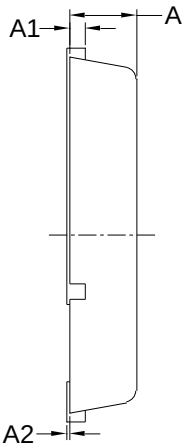
PDFN5060-8L-B-1.1MM Package information



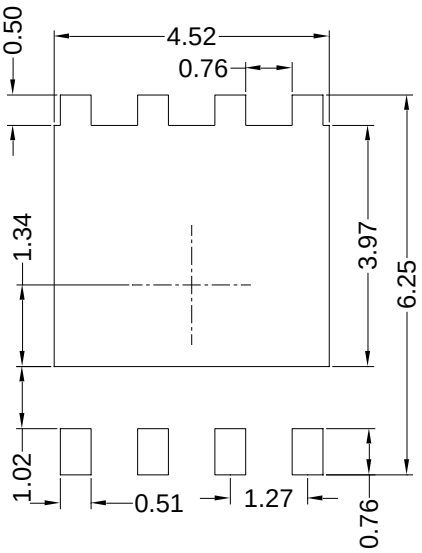
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254 REF	
E4		0.21 REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.