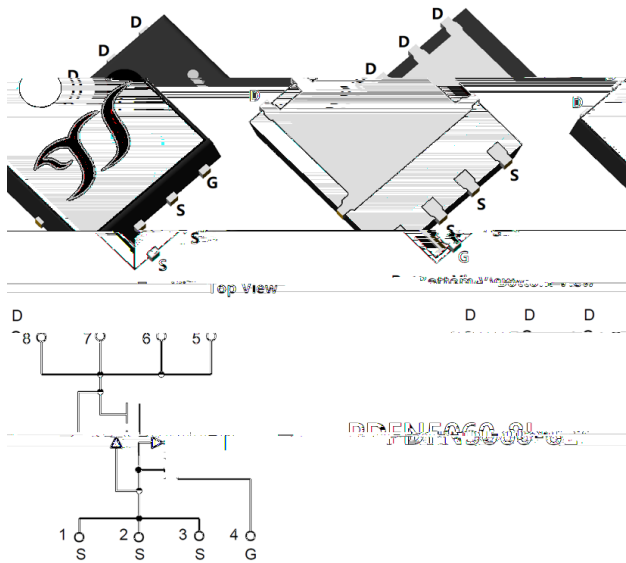


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

V_{DS}	85V
I_D	98A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	6.5m
$R_{DS(ON)}$ (at $V_{GS}=6V$)	10m
100% EAS Tested	
100% V_{DS} Tested	

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC converter

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	85	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	12	A
	$T_A=100^\circ C$		7	
	$T_C=25^\circ C$		98	
	$T_C=100^\circ C$		62	
Pulsed Drain Current ^A		I_{DM}	400	A
Avalanche energy ^B		EAS	400	mJ
Total Power Dissipation ^C	$T_A=25^\circ C$	P_D	2.5	W
	$T_A=100^\circ C$		1	
	$T_C=25^\circ C$		110	
	$T_C=100^\circ C$		45	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	$^\circ C$

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	R_{JA}	40	50	$^\circ C/W$
	Thermal Resistance Junction-to-Case	R_{JC}	0.9	1.1	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG98G08H	F1	YJG98G08H	5000	10000	100000	13" reel



YJG98G08H

Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	85	-	-	V

Zero Gate Voltage Drain Current



Typical Electrical and Thermal Characteristics Diagrams

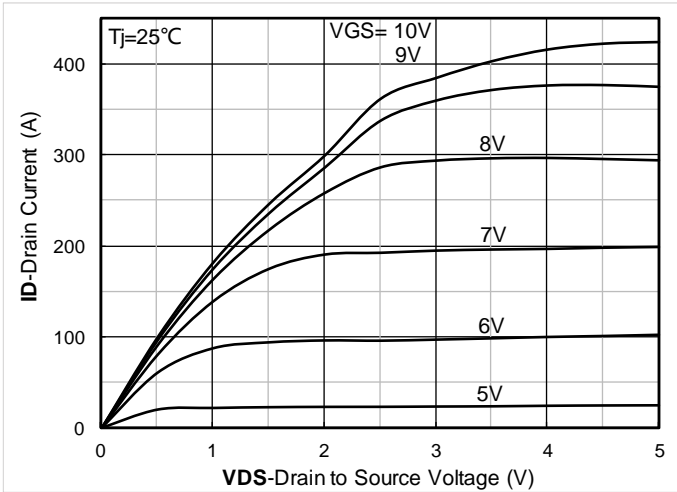


Figure 1. Output Characteristics

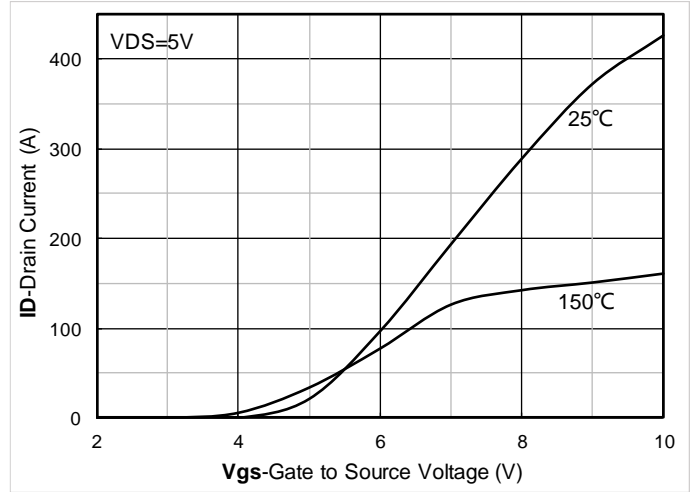


Figure 2. Transfer Characteristics

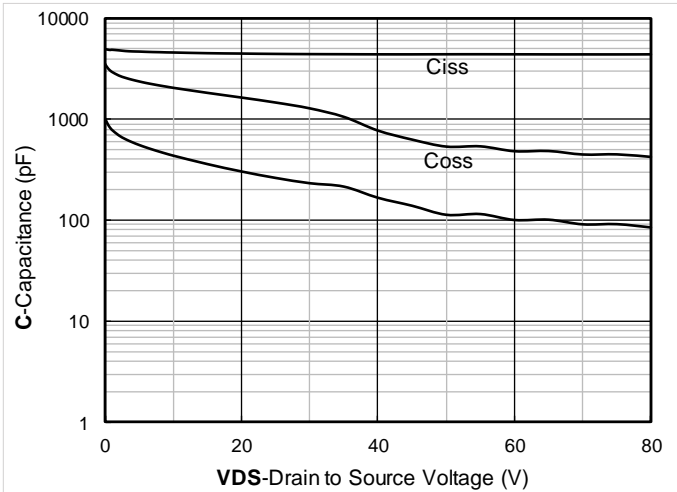


Figure 3. Capacitance Characteristics

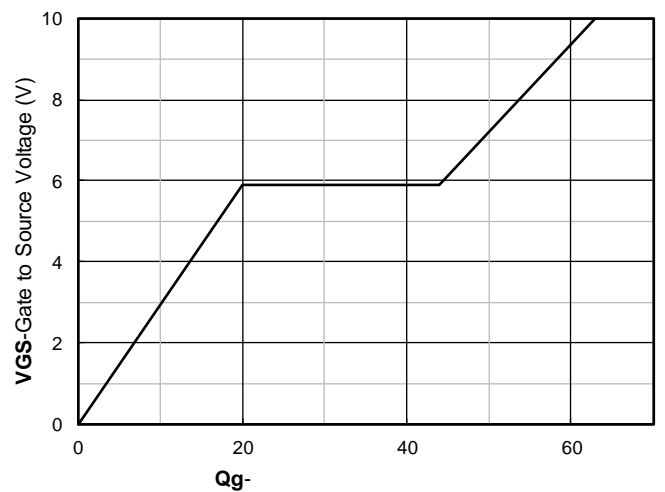


Figure 4. Gate Charge

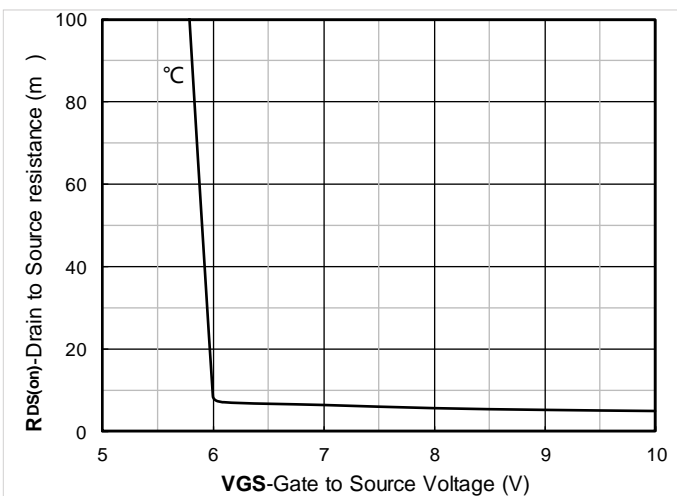


Figure 5. On-Resistance vs Gate to Source Voltage

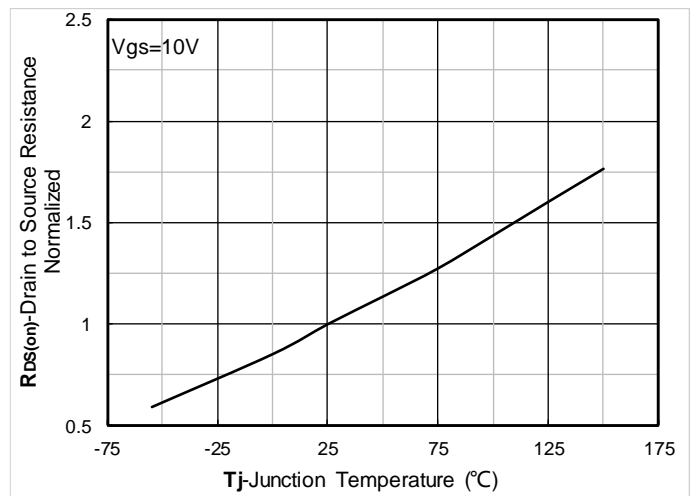


Figure 6. Normalized On-Resistance



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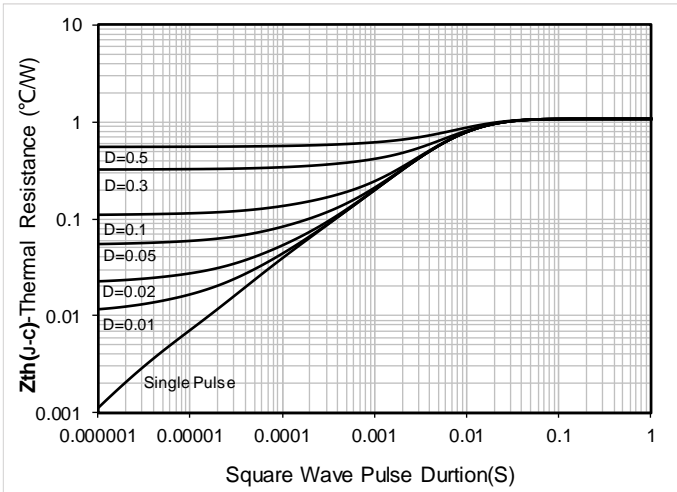


Figure 13. Maximum Transient Thermal Impedance

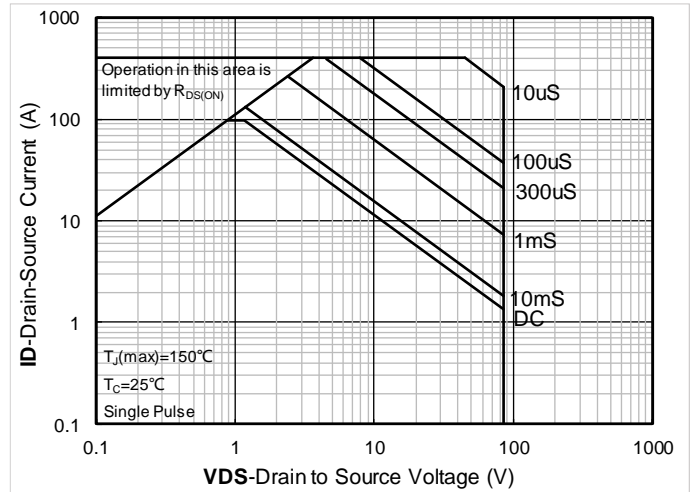


Figure 14. Safe Operation Area

Test Circuits & Waveforms

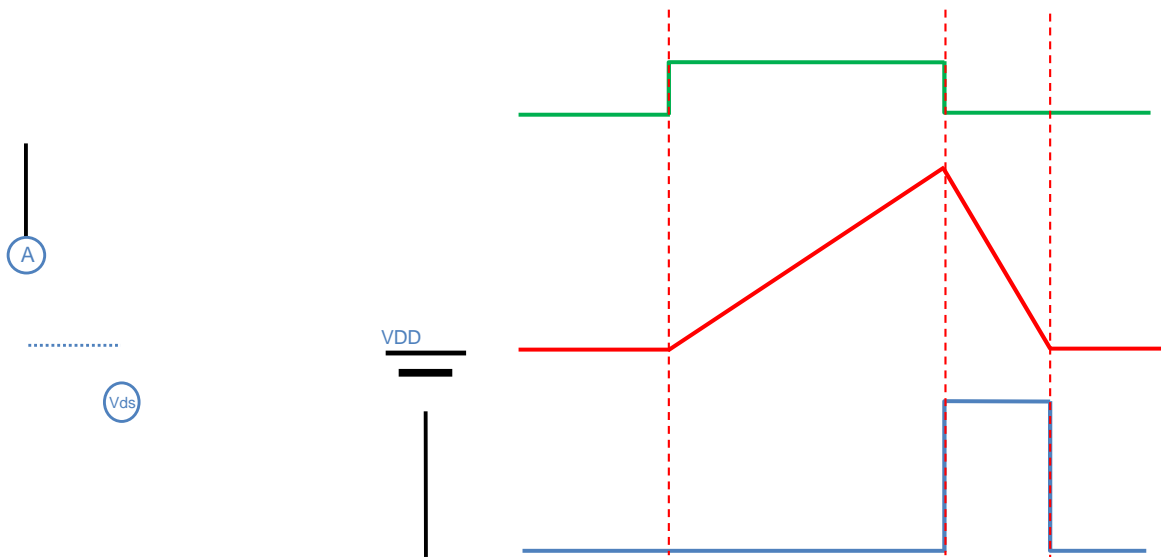


Figure A. Uncl -1501/MCIDI /P AMCID 19/L[.10 1 178.39 239.11 Tm0 g0 G -0.0418 Tc[]TJETQ EMC

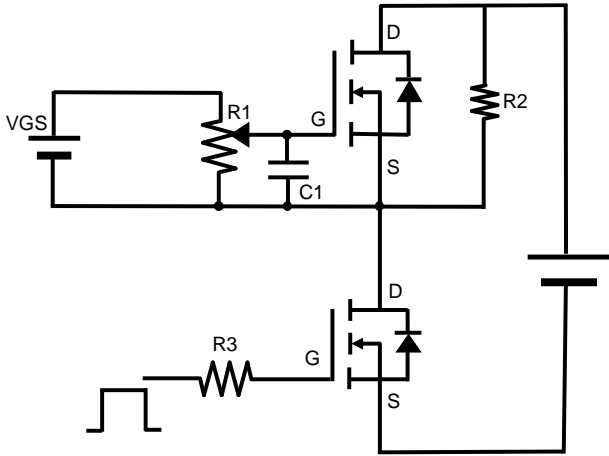


Figure B. Gate Charge Test Circuit & Waveform

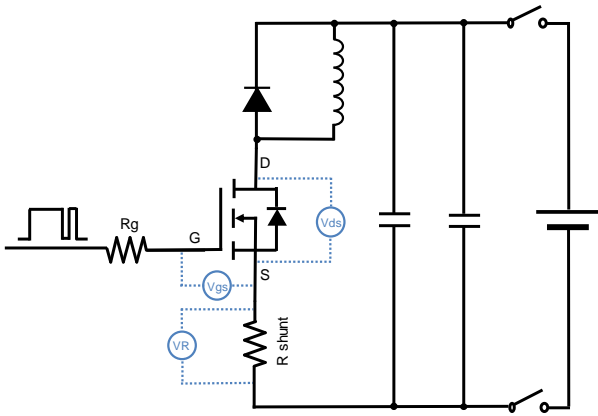


Figure C. Resistive Switching Test Circuit & Waveform

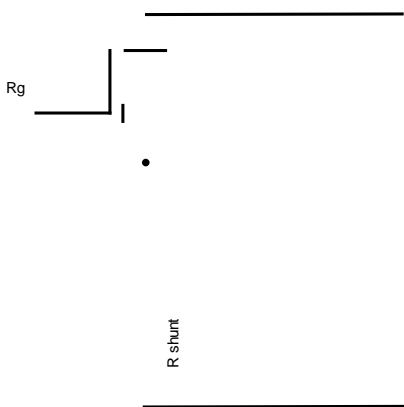
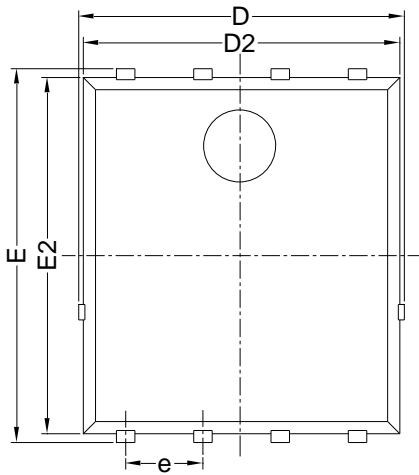


Figure D. Diode Recovery Test Circuit & Waveform

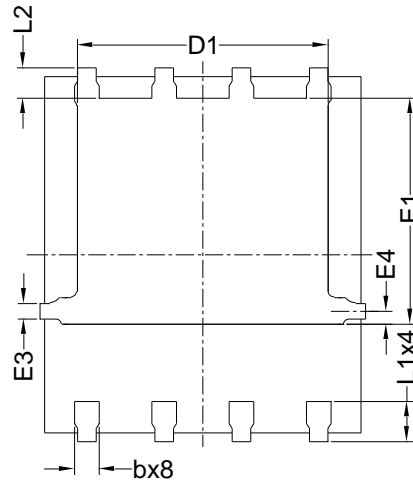


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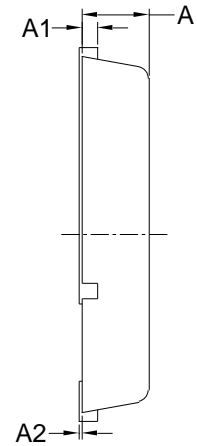
PDFN5060-8L-B-1.1MM Package information



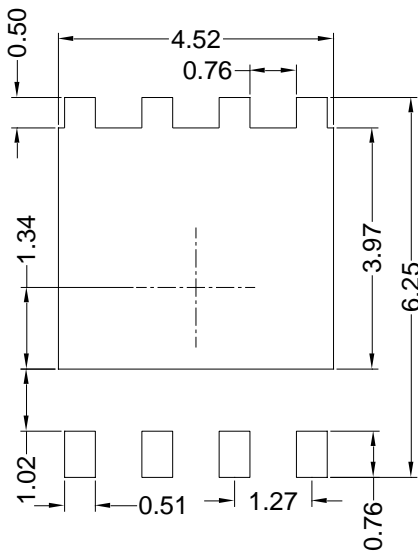
Top View



Bottom View



Side View



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



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