

20V
55A
 (at $V_{GS} = 4.5V$) **25mhm**
 (at $V_{GS} = 2.5V$) **32mhm**
 (at $V_{GS} = 1.8V$) **49mhm**

Power LV MOSFET technology
 density cell design for low $R_{DS(on)}$
 speed switching

protection
 switch
 management

Drain-source Voltage	V_{DS}	20	V
Gate-source Voltage	V_{GS}	10	V
Drain Current	I_D	55	A
		44	
Pulsed Drain Current	I_{DM}	22	A
Total Power Dissipation	P_D	11	W
Thermal Resistance	R_{JA}	114	W
Junction and Storage Temperature Range	T_j, T_{STG}	-55 +150	

(Example)

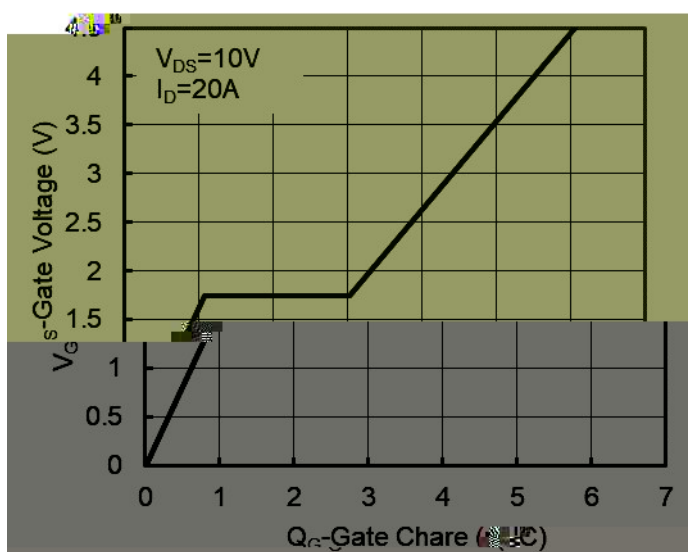
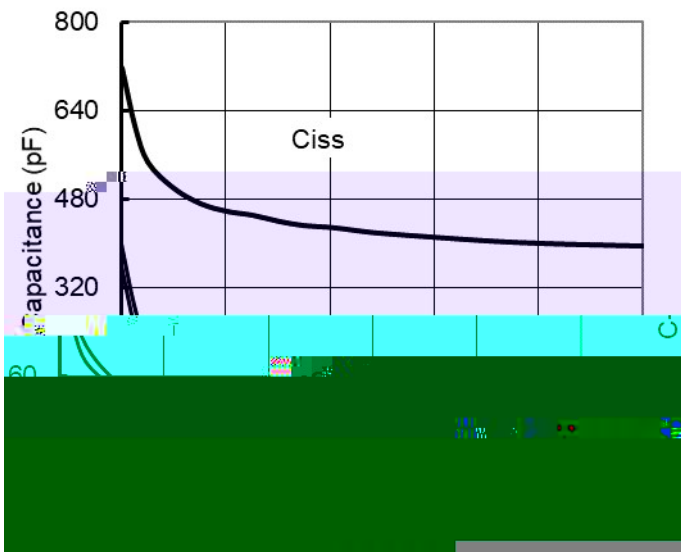
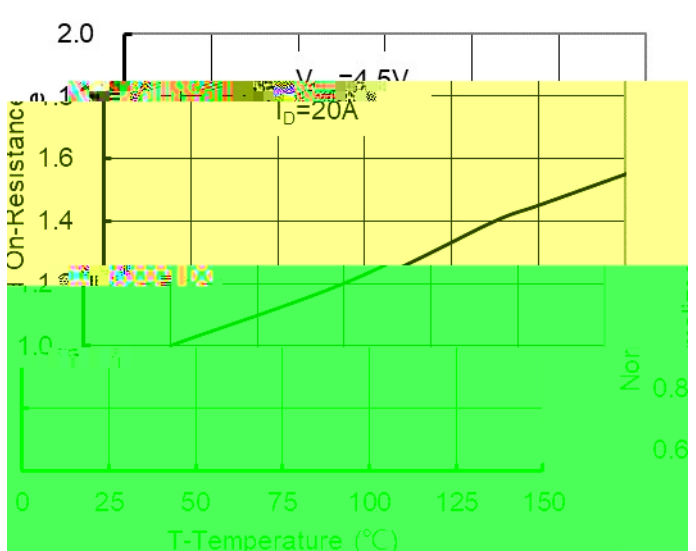
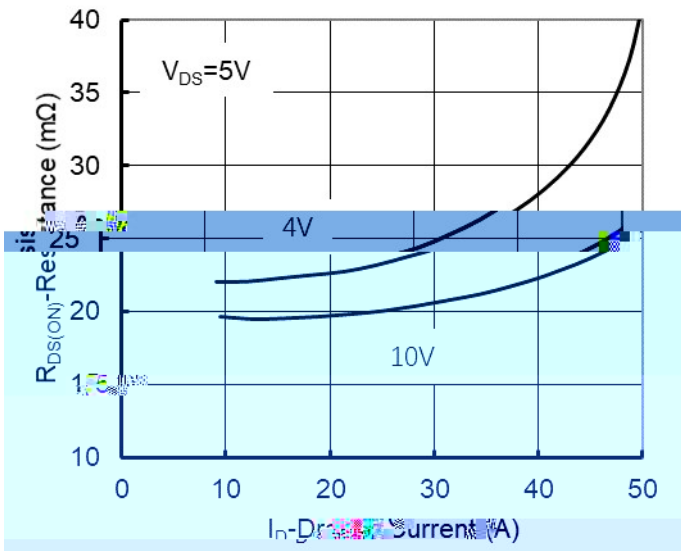
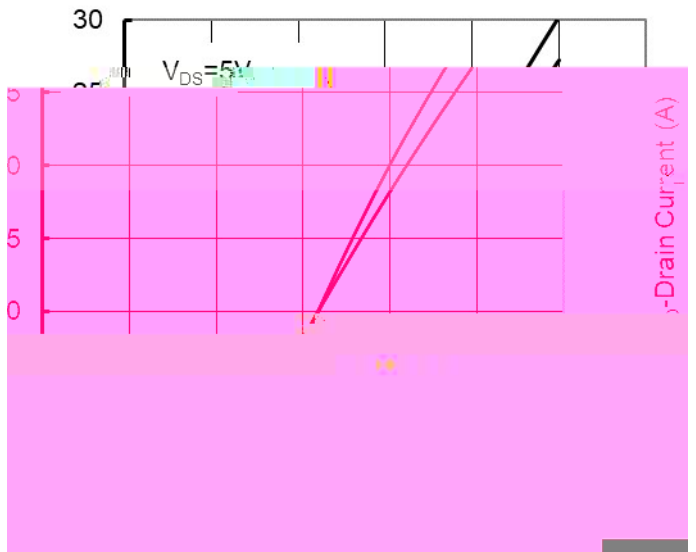
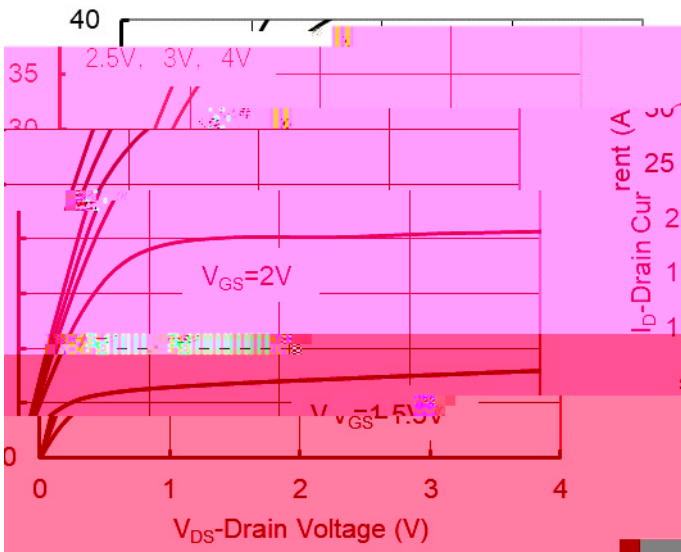


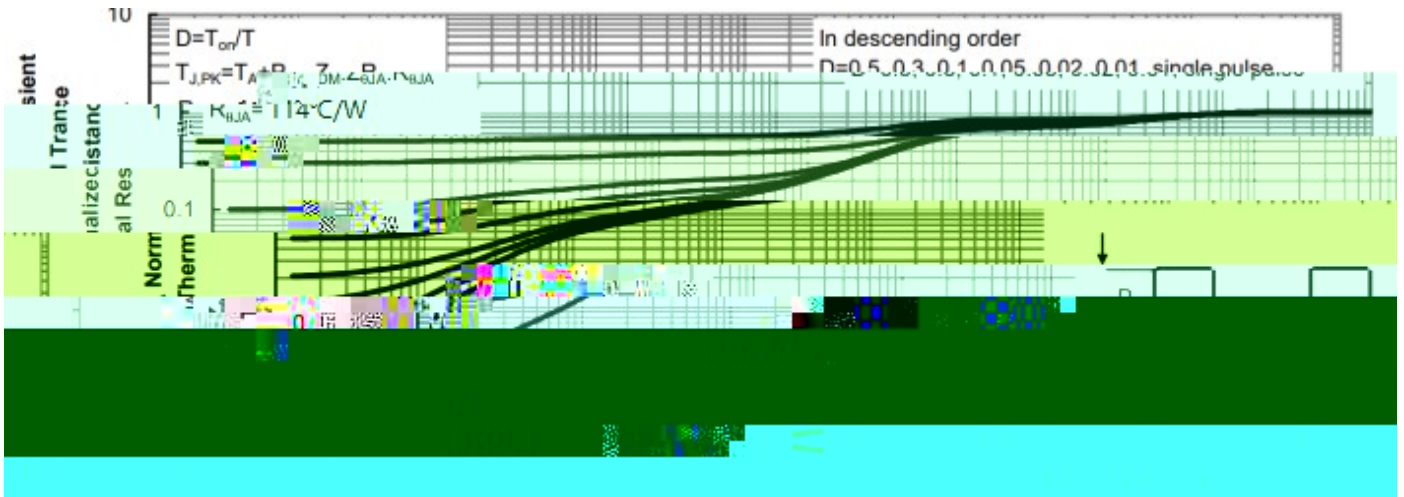
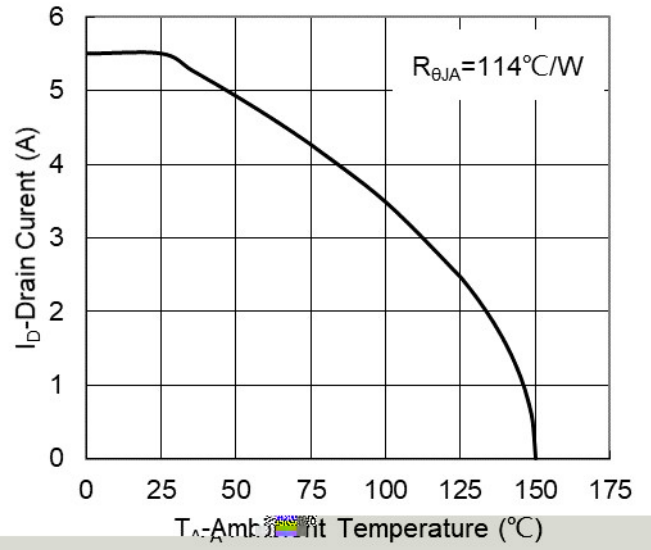
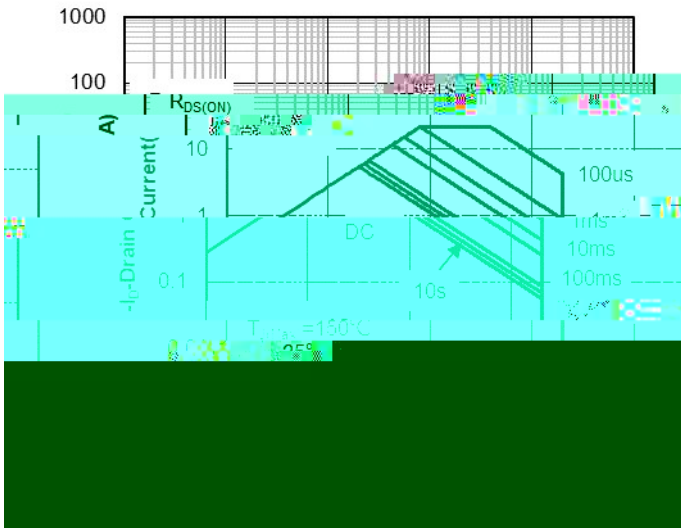


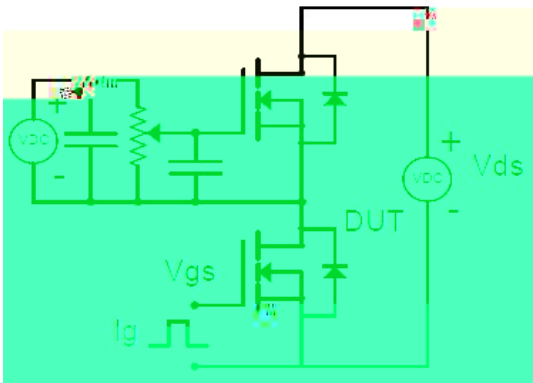
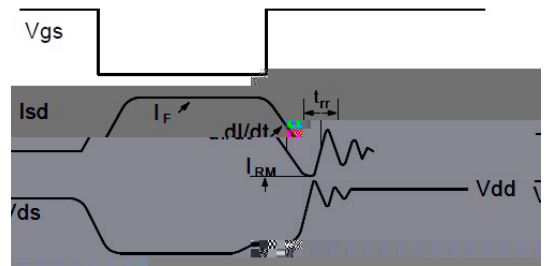
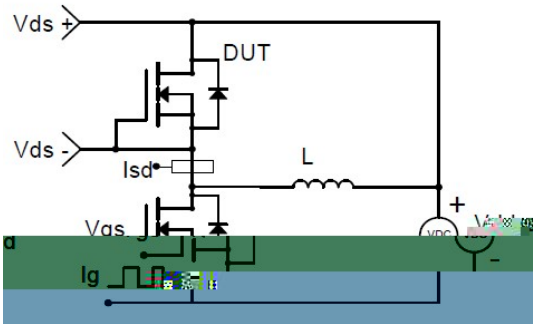
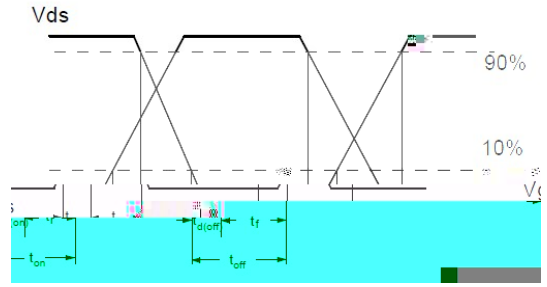
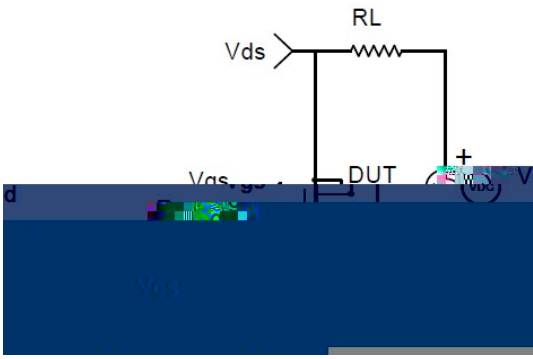
(T_F=25 unless otherwise noted)

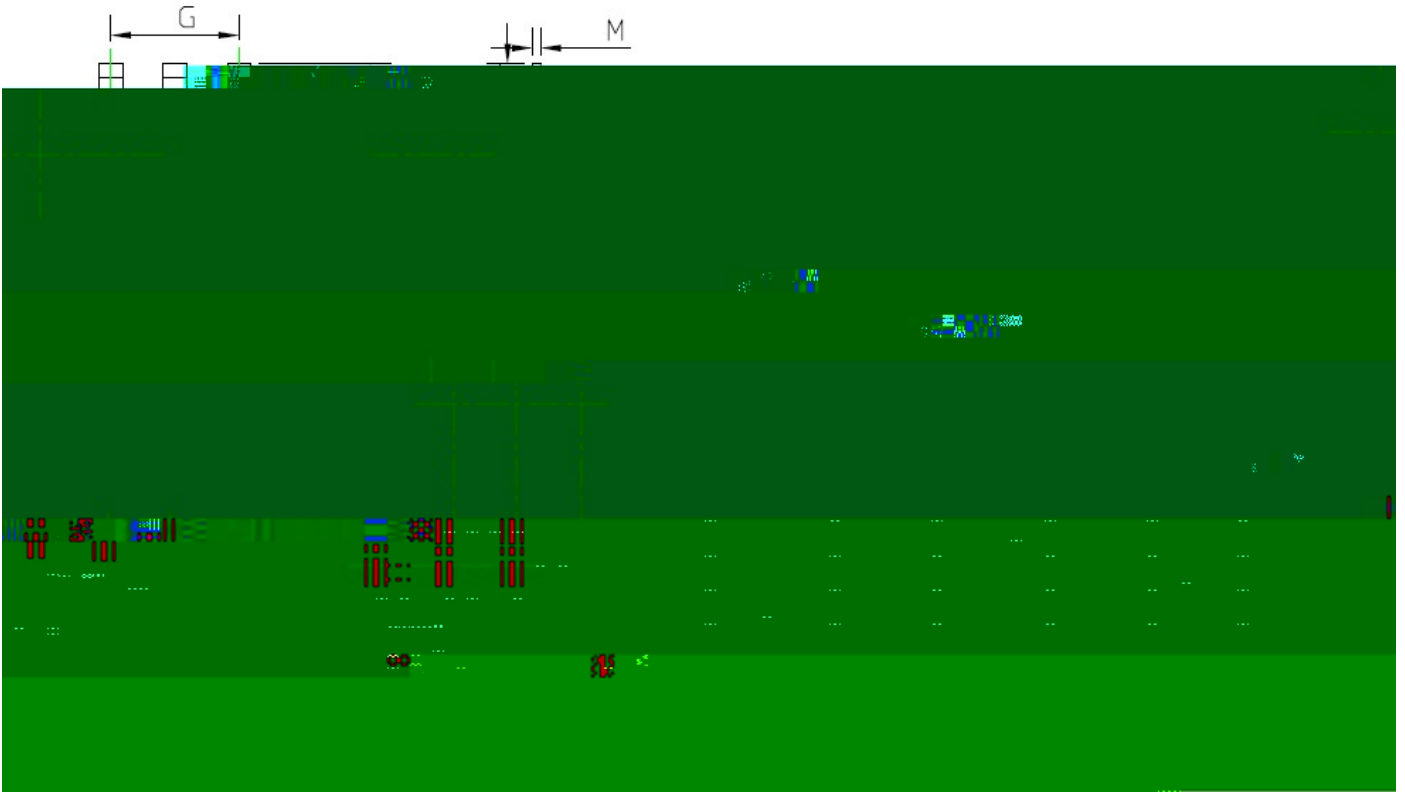
Drain Source Breakdown Voltage					V
Zero Gate Voltage Drain Current			1		μA
Gate Body Leakage Current			100		nA
Gate Threshold Voltage			1		V
Static Drain Source On Resistance			25		m
			32		

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