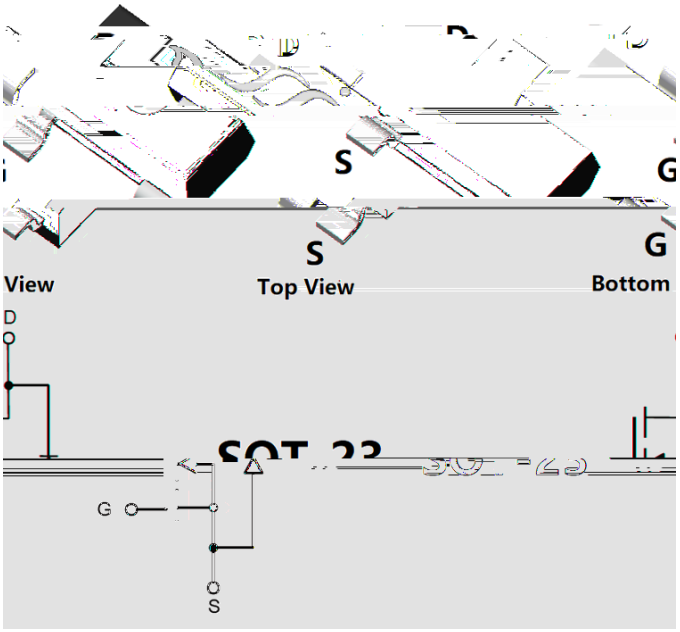
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

. DS	100V
. D	2A
. DS(ON)(at VGS=10V)	280mohm
. DS(ON)(at VGS=4.5V)	310mohm

General Description

Trench Power MV MOSFET technology
Excellent package for heat dissipation
High density cell design for low RDS(ON)
. . . .
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

DC-DC Converters
Power management functions

Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	20	V
Drain Current	T_A=25	I_D	2	A
	T_A=70		1.6	
Pulsed Drain Current [A]		I_{DM}	8	A
Total Power Dissipation	T_A=25	P_D	1.3	W
	T_A=70		0.8	W
Thermal Resistance Junction-to-Ambient [B]		R JA	96	/ W
Thermal Resistance Junction-to-Case [B]		R JL	80	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +150	

Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL02N10A	F2	1002	3000	30000	120000	7 reel

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V			1	
Gate-Body Leakage Current	I_{GSS1}	V_{GS}= 20V, V_{DS}=0V			100	nA
	I_{GSS2}	V_{GS}= 10V, V_{DS}=0V			50	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250	1.1	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=2A		250	280	m
		V_{GS}=4.5V, I_D=1A		260	310	
Diode Forward Voltage	V_{SD}	I_S=2A,V_{GS}=0V			1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=10V,V_{GS}=0V,f=1MHZ		387		pF
Output Capacitance	C_{oss}			31		
Reverse Transfer Capacitance	C_{rss}			28		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=2A		9.56		nC
Gate-Source Charge	Q_{gs}			1.81		
Gate-Drain Charge	Q_{gd}			1.97		
Reverse Recovery Chrage	Q_{rr}	I_F=2A, di/dt=100A/us		14.4		
Reverse Recovery Time	t_{rr}			36.1		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DS}=50V, I_D=1.3A R_{GEN}=1		4		
Turn-on Rise Time	t_r			17.8		
Turn-off Delay Time	$t_{D(off)}$			13.2		
Turn-off fall Time	t_f			28		

A. Pulse Test: Pulse Width 300us,Duty cycle 2%.

B. R_{JA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{JC} is guaranteed by design, while R_{JA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

Typical Performance Characteristics

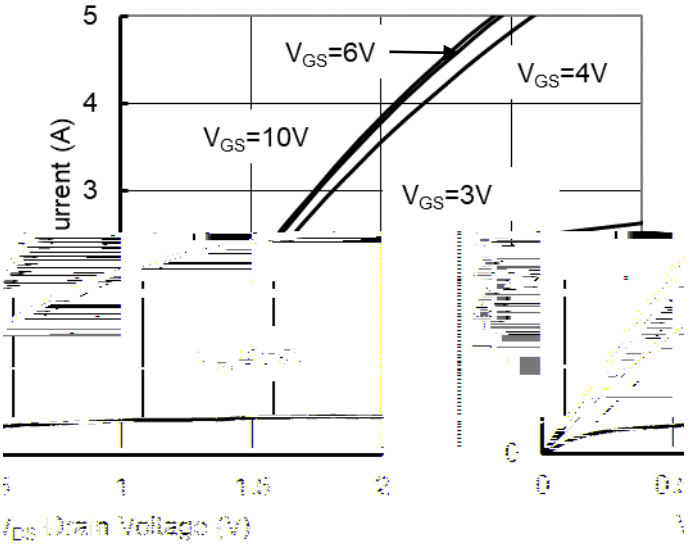


Figure1. Output Characteristics

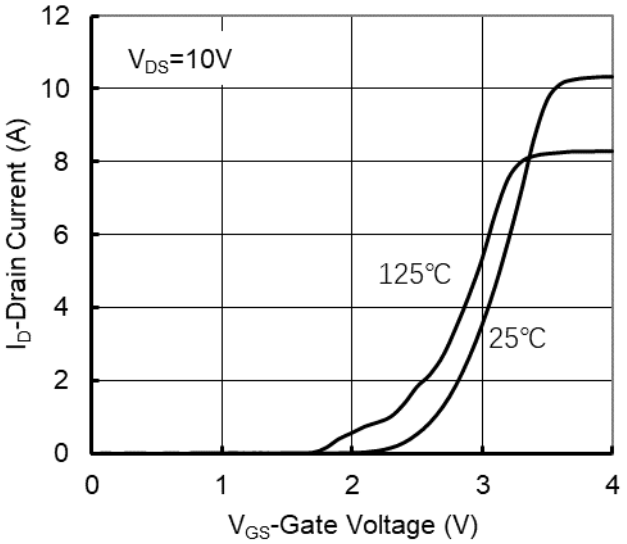


Figure2. Transfer Characteristics

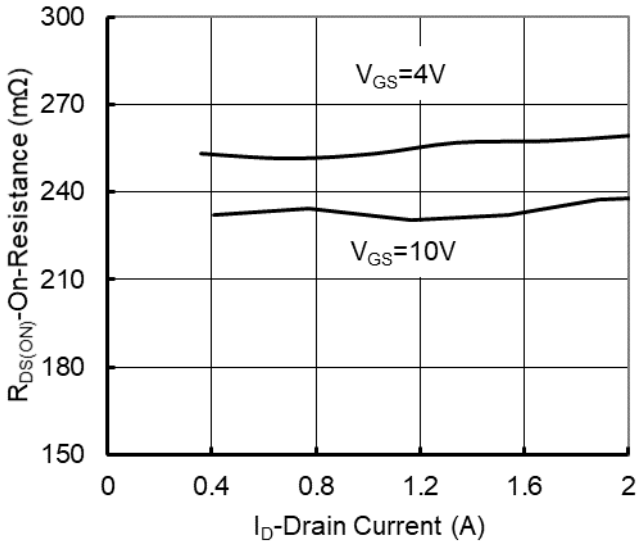


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

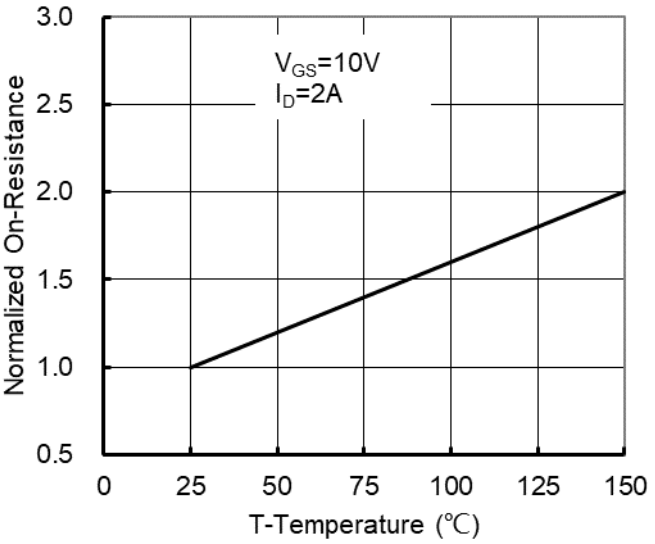


Figure 4: On-Resistance vs. Junction Temperature

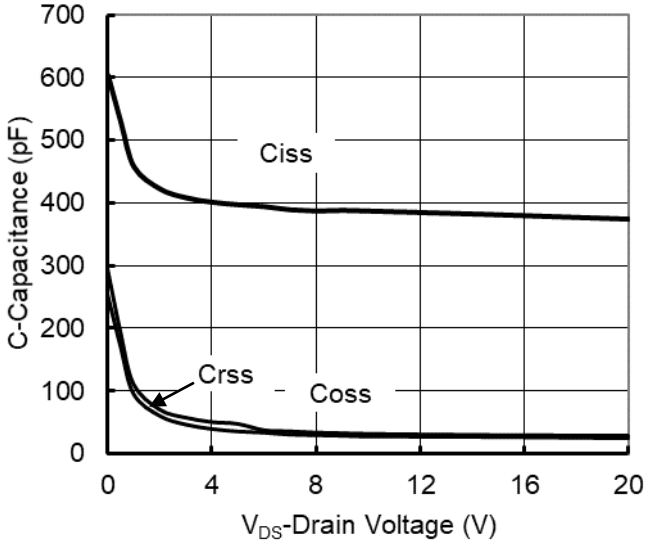


Figure5. Capacitance Characteristics

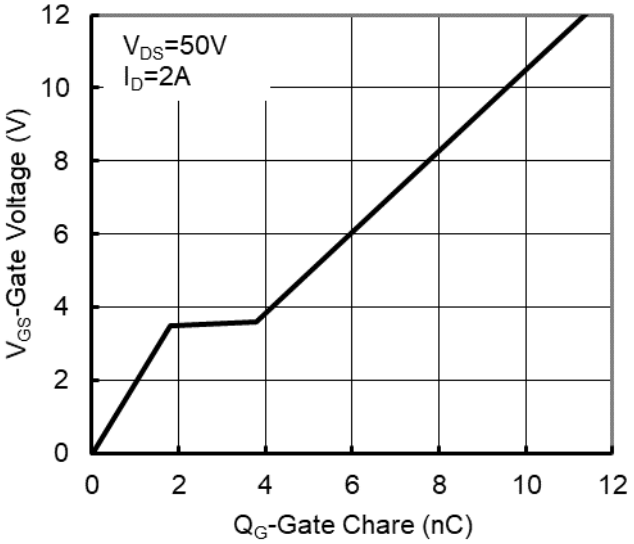
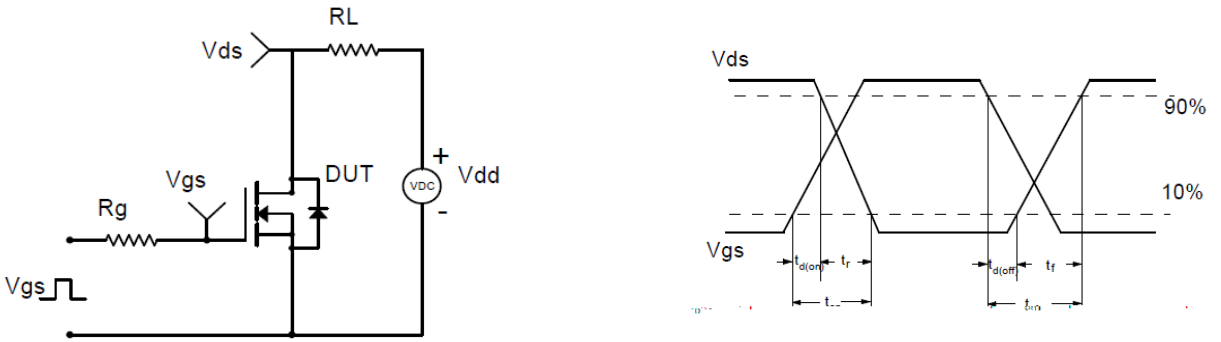
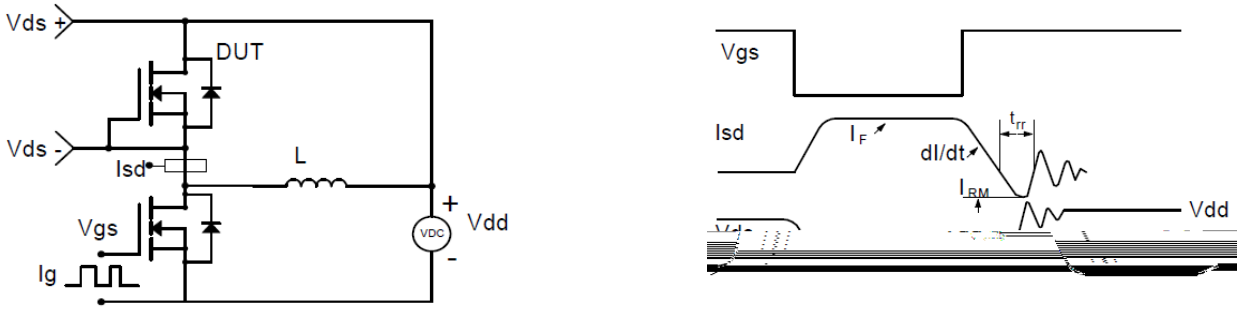


Figure6. Gate Charge

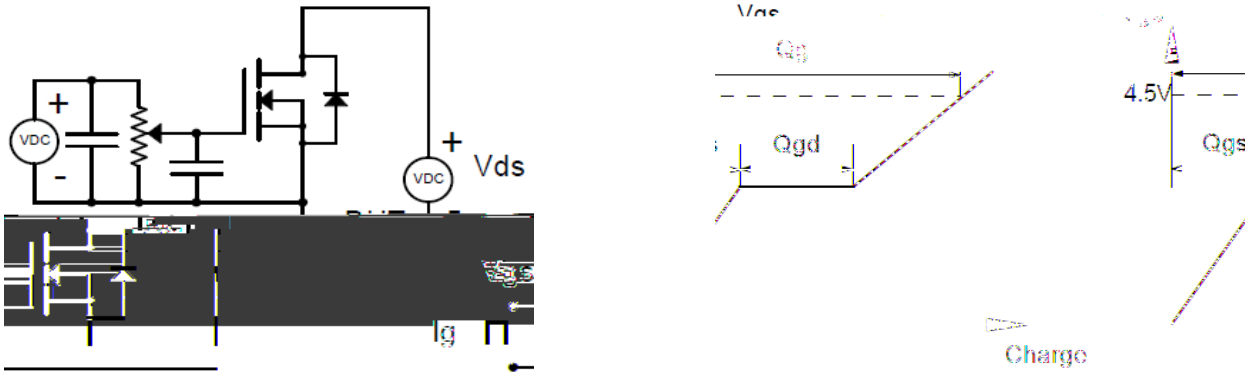
YJL02N10A



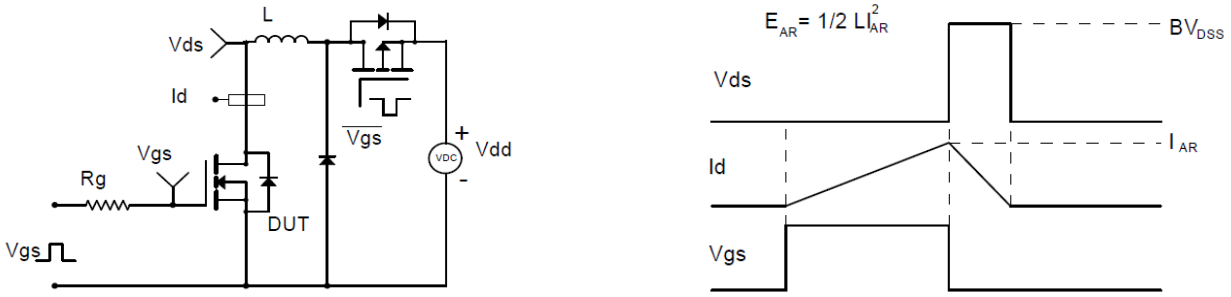
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

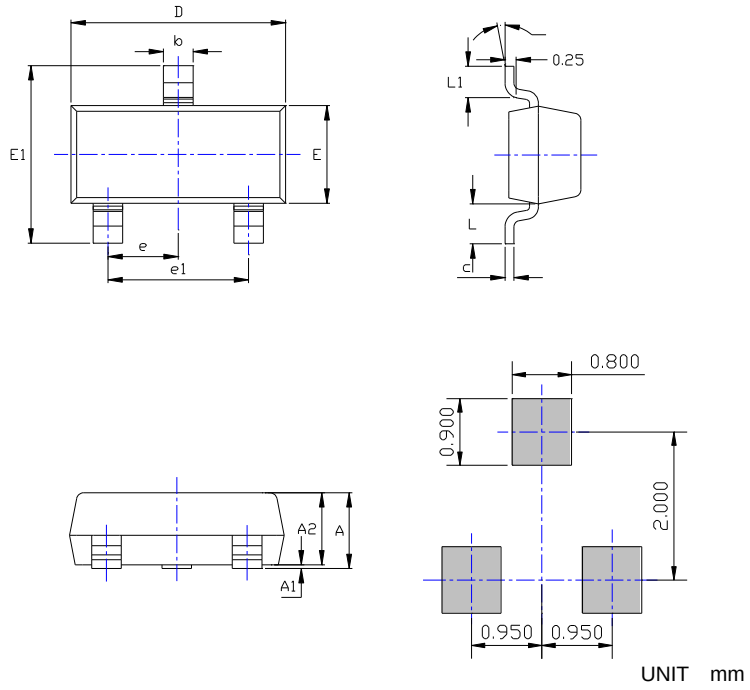


Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

SOT-23 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	(			

UNIT mm

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