



## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	30V
$I_D$	0.4A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	2.5
$R_{DS(ON)}$ ( at $V_{GS}=4.5V$ )	3
Gate-Source ESD Rating Up to 2KV (HBM)	

### General Description

Excellent package for heat dissipation  
 High density cell design for low  $R_{DS(ON)}$   
 Moisture Sensitivity Level 1  
 Epoxy Meets UL 94 V-0 Flammability Rating  
 Halogen Free

### Applications

Power switching application  
 Uninterruptible power supply  
 DC-DC convertor

### Absolute Maximum Ratings ( $T_J=25$ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			$V_{DS}$	30	V
Gate-source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25$ , $V_{GS}=10V$	$I_D$	0.4	A
		$T_A=100$ , $V_{GS}=10V$		0.25	
Pulsed Drain Current	$T_C=25$ , $t=100\mu s$		$I_{DM}$	1.1	A
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25$	$P_D$	0.83	W
		$T_A=100$		0.33	
Junction and Storage Temperature Range			$T_J, T_{STG}$	-55 +150	

### Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	R	125	150	/W

### Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking
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## Typical Electrical and Thermal Characteristics Diagrams

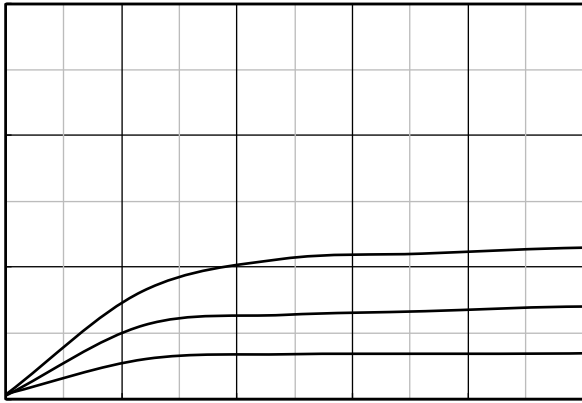


Figure 1. Output Characteristics

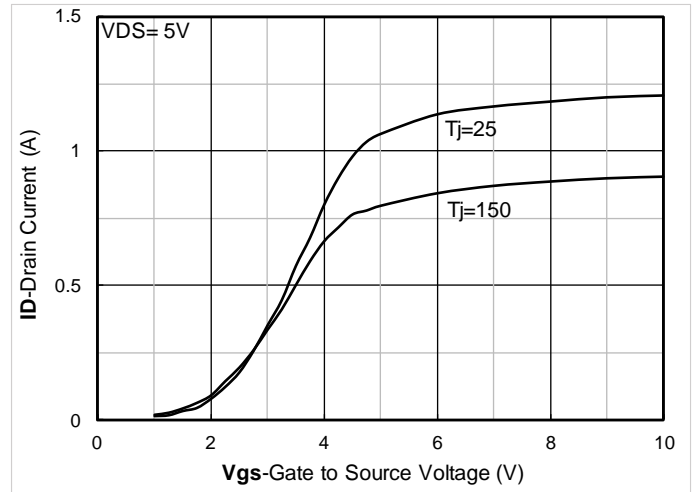


Figure 2. Transfer Characteristics

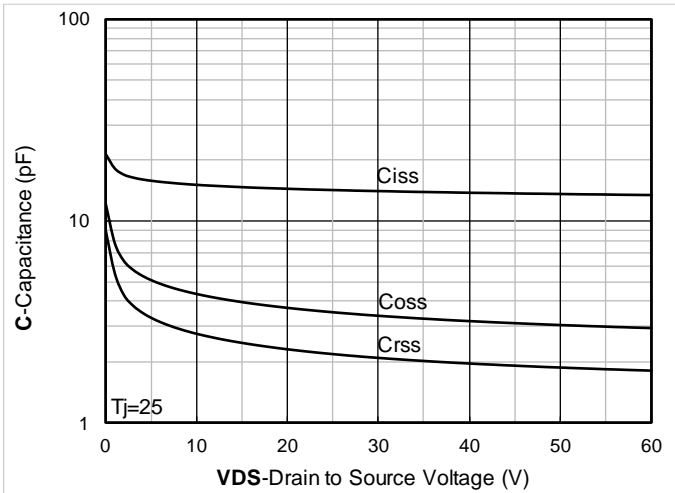


Figure 3. Capacitance Characteristics

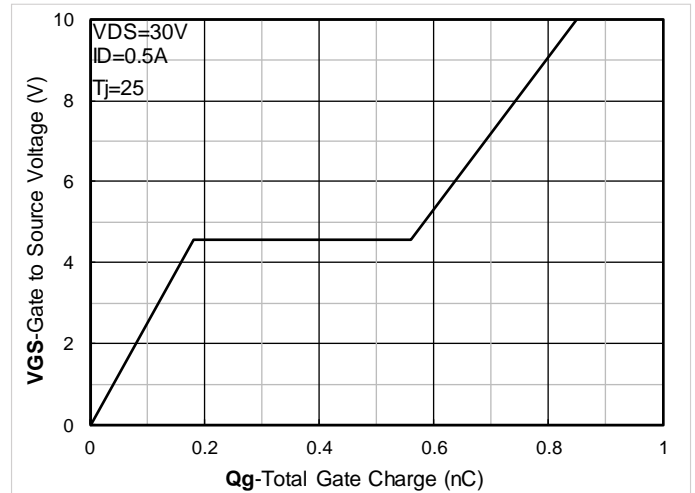


Figure 4. Gate Charge

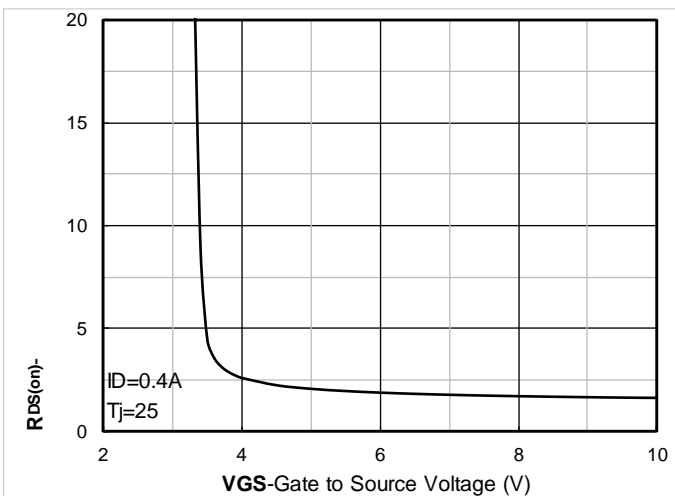


Figure 5. On-Resistance vs Gate to Source Voltage

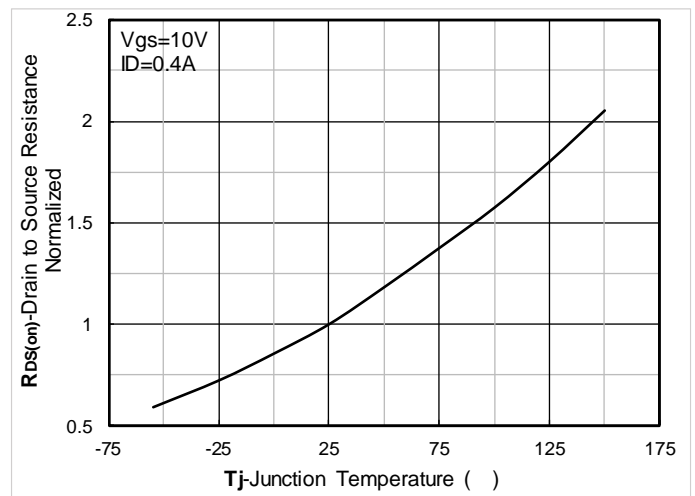


Figure 6. Normalized On-Resistance

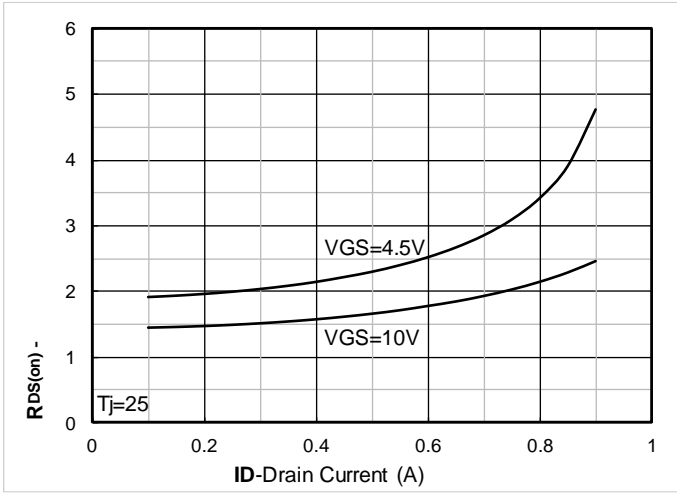


Figure 7. RDS(on) VS Drain Current

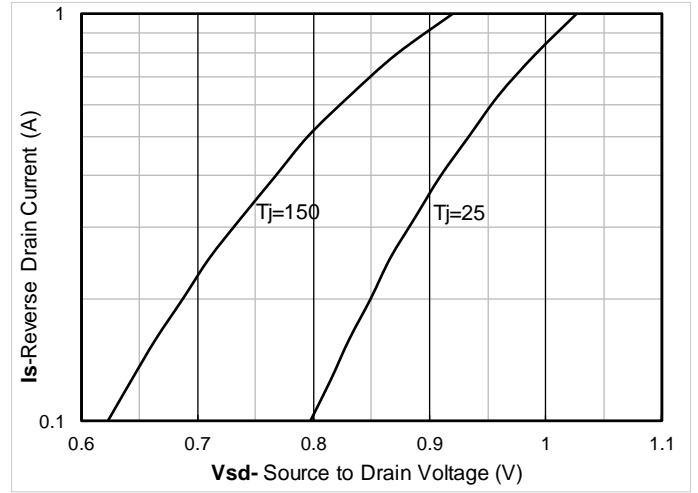


Figure 8. Forward characteristics of reverse diode

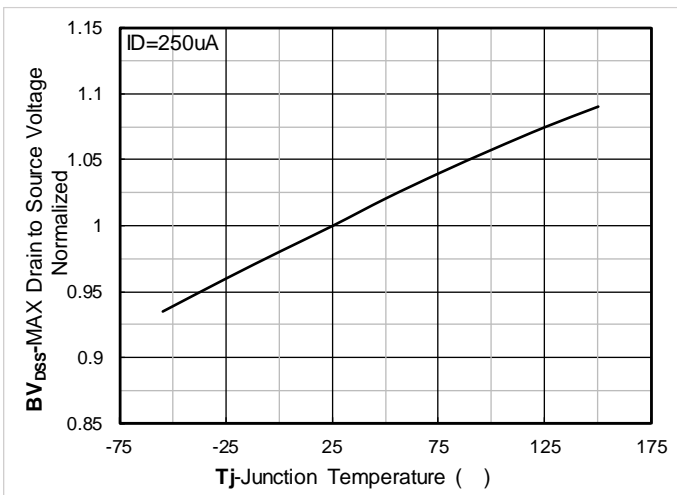


Figure 9. Normalized breakdown voltage

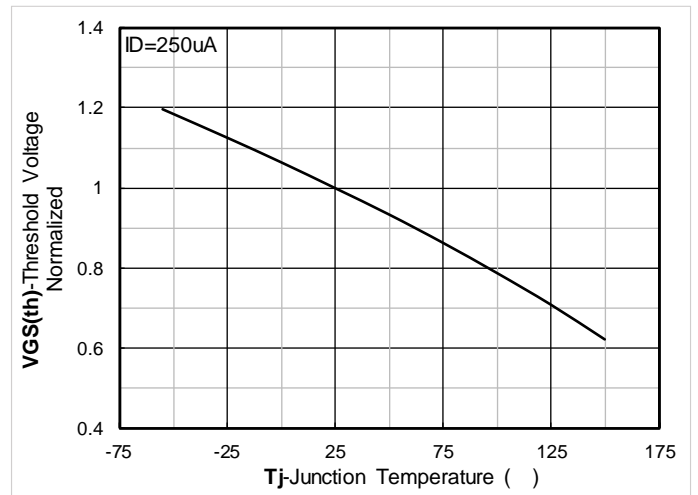


Figure 10. Normalized Threshold voltage

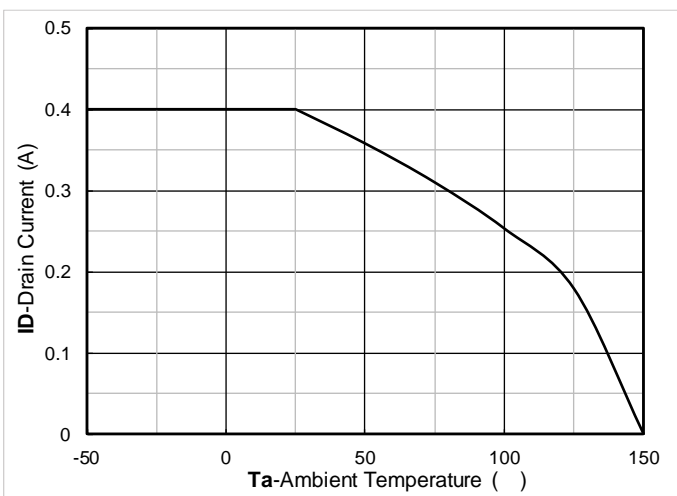


Figure 11. Current dissipation

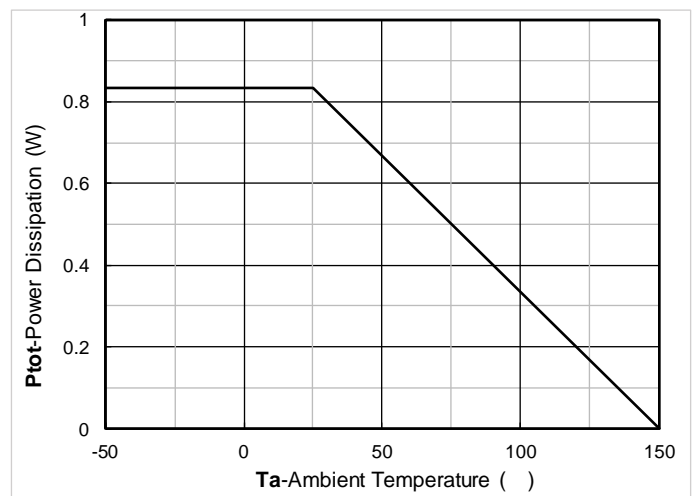


Figure 12. Power dissipation

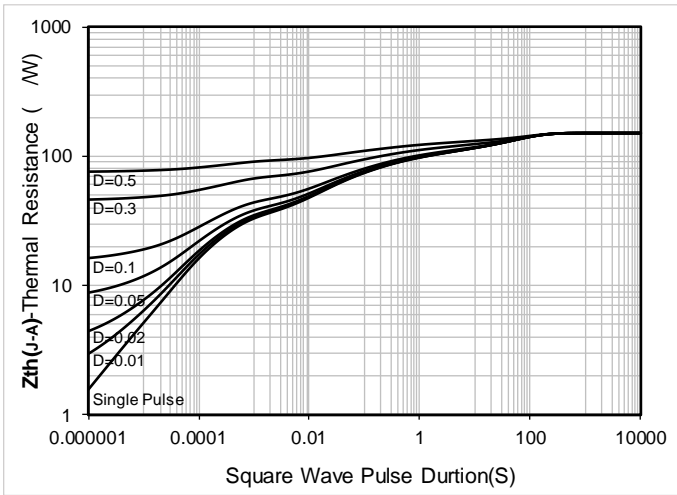


Figure 13. Maximum Transient Thermal Impedance

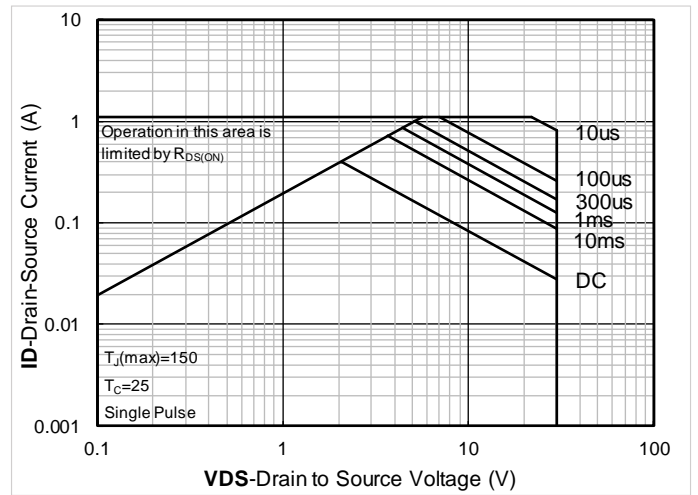


Figure 14. Safe Operation Area

### Test Circuits & Waveforms

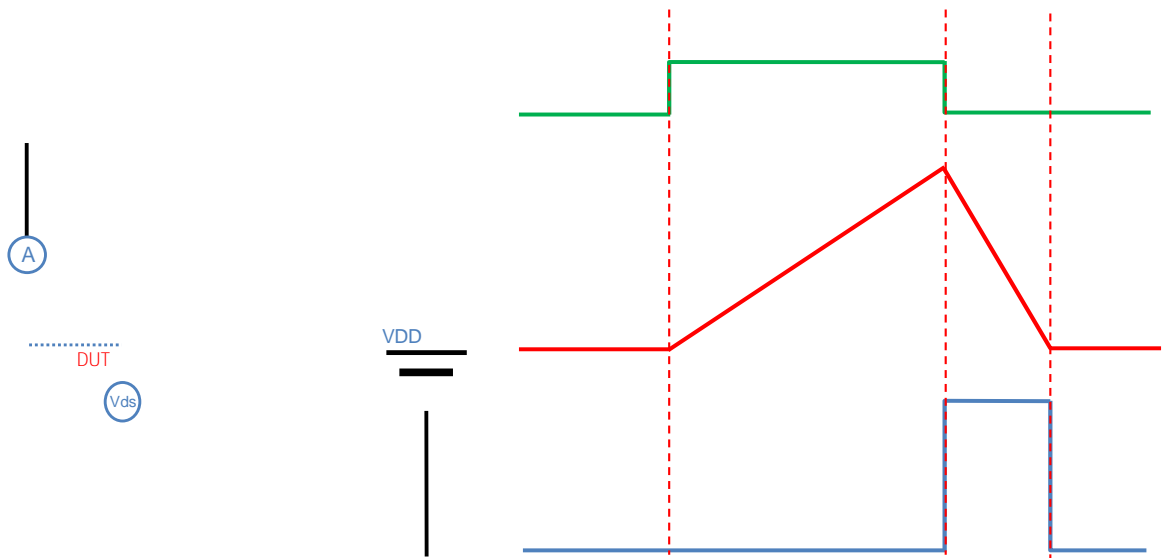


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

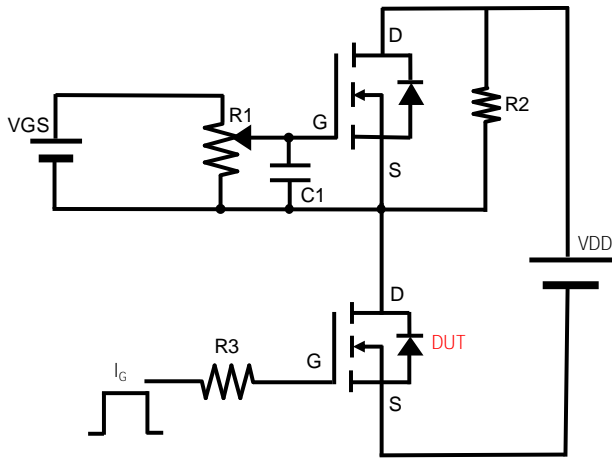


Figure B. Gate Charge Test Circuit & Waveform

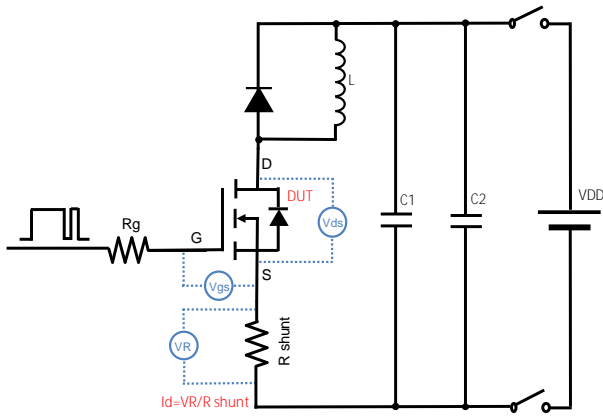


Figure C. Resistive Switching Test Circuit & Waveform

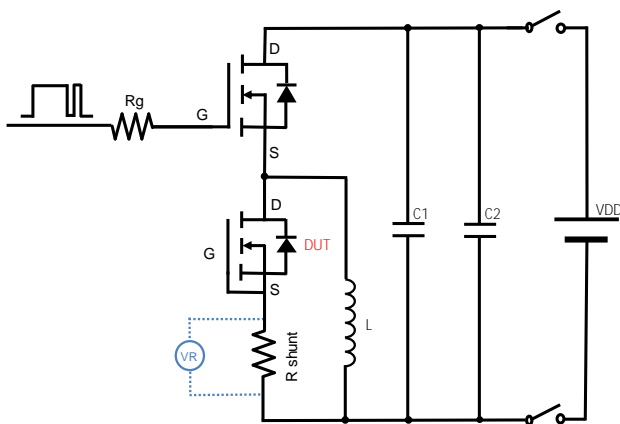
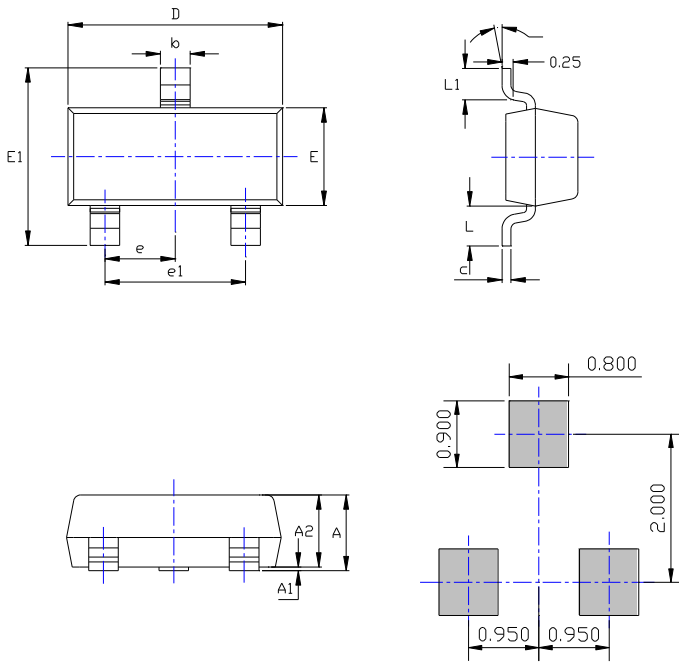


Figure D. Diode Recovery Test Circuit & Waveform



# YJL3018KJ

## SOT-23 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
	0°	8°	0°	8°

NOTE:  
 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.  
 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



## YJL3018KJ

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