



YJP118G08H

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	85V
I_D	118A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	6.5m
$R_{DS(ON)}$ (at $V_{GS}=6V$)	10m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Split gate trench MOSFET technology
 Excellent package for heat dissipation
 High density cell design for low $R_{DS(ON)}$
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

Power switching application
 Uninterruptible power supply
 DC-DC convertor

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	85	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	13	A
	$T_A=100^\circ C$		8	
	$T_C=25^\circ C$		118	
	$T_C=100^\circ C$		74	
Pulsed Drain Current ^A		I_{DM}	472	A
Avalanche energy ^B		EAS	351	mJ
			3.1	
Total Power Dissipation ^C	$T_A=100^\circ C$	P_D	1.2	W



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Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D$	85	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=85V, V_{GS}=0V$	-	-	1	
		$V_{DS}=85V, V_{GS}=0V, T_J=150^\circ C$	-	-	100	



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Typical Electrical and Thermal Characteristics Diagrams

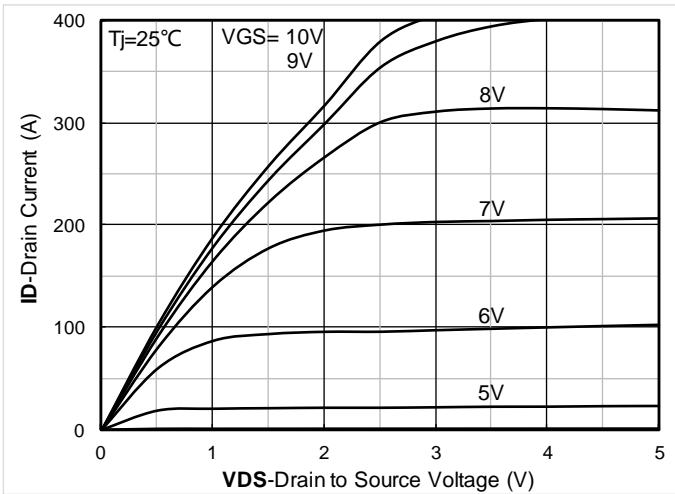


Figure 1. Output Characteristics

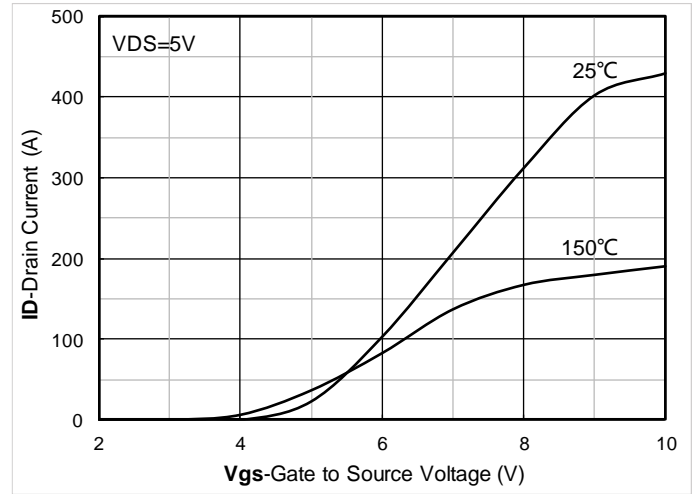


Figure 2. Transfer Characteristics

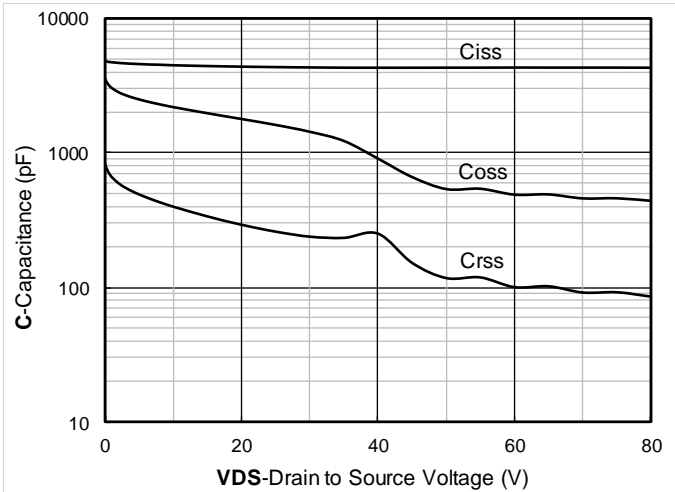


Figure 3. Capacitance Characteristics

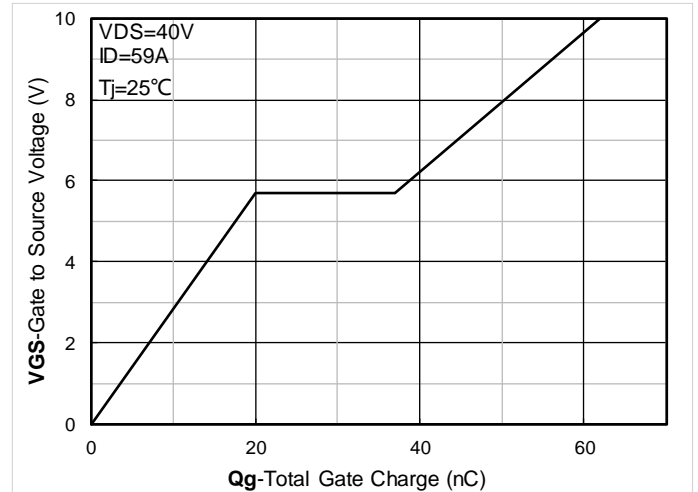


Figure 4. Gate Charge

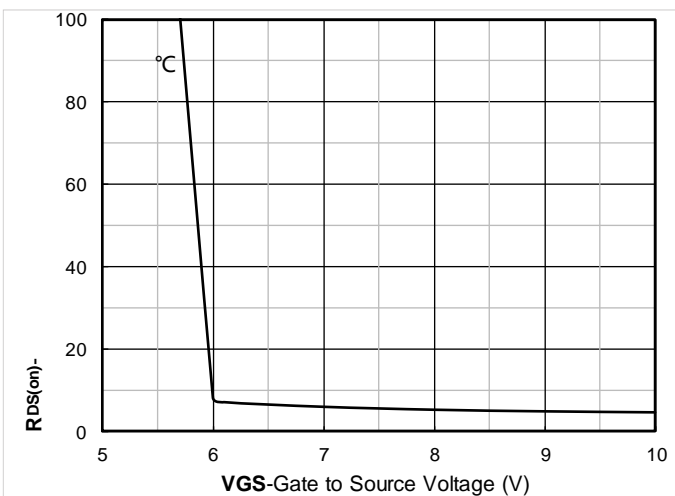


Figure 5. On-Resistance vs Gate to Source Voltage

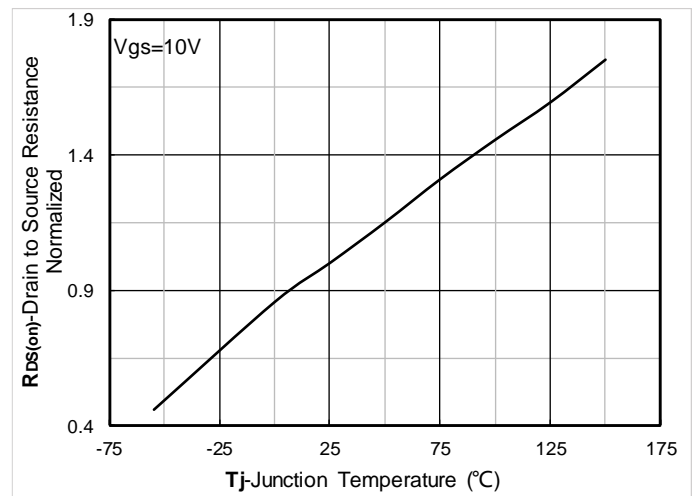


Figure 6. Normalized On-Resistance



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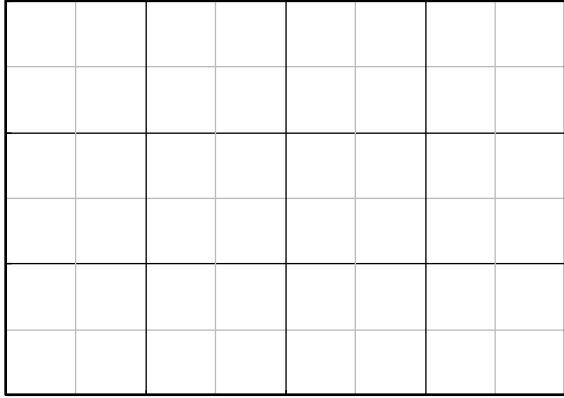


Figure 7. $R_{DS(on)}$ VS Drain Current

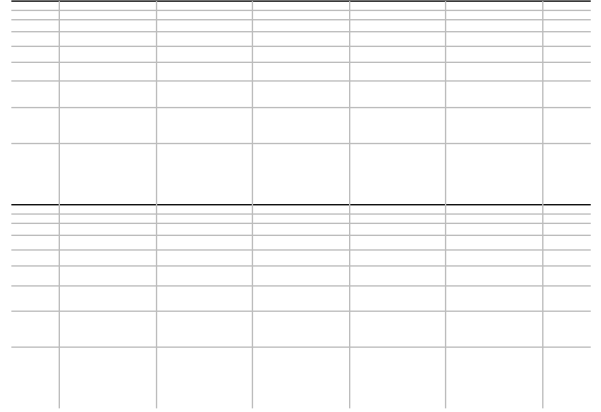


Figure 8. Forward characteristics of reverse diode

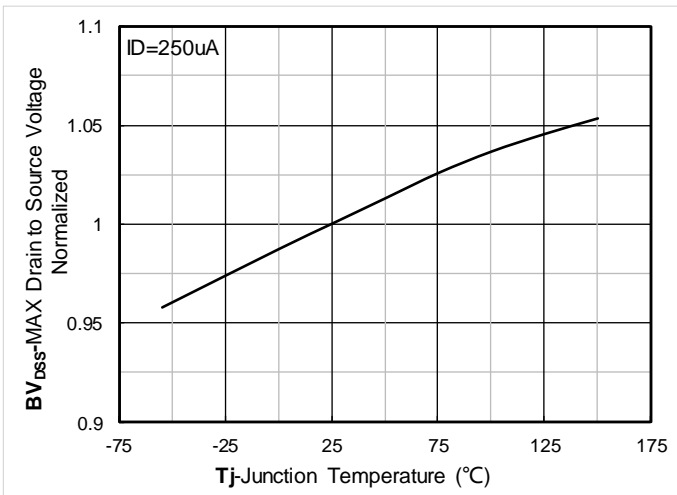


Figure 9. Normalized breakdown voltage

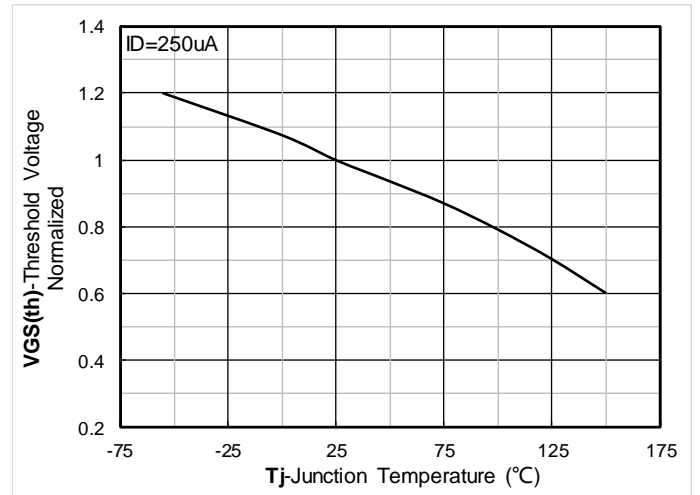


Figure 10. Normalized Threshold voltage

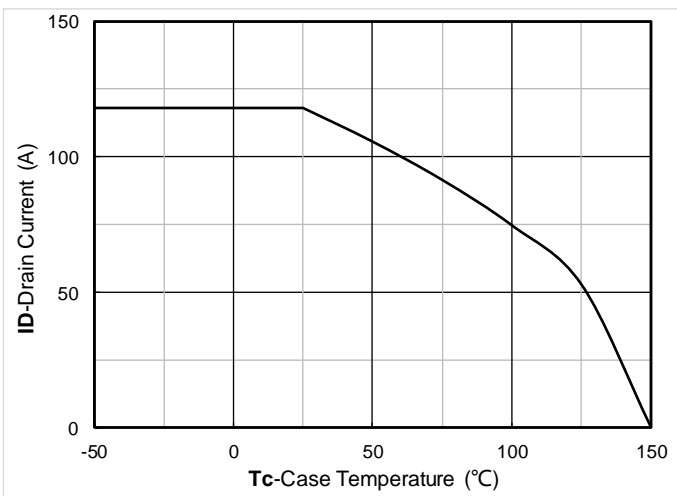


Figure 11. Current dissipation

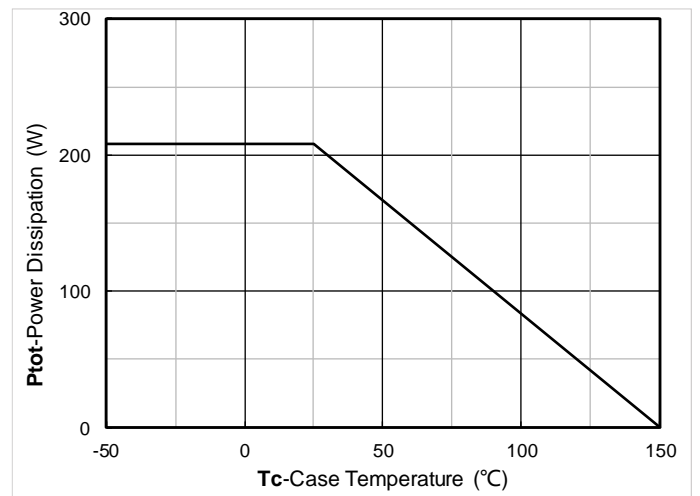


Figure 12. Power dissipation



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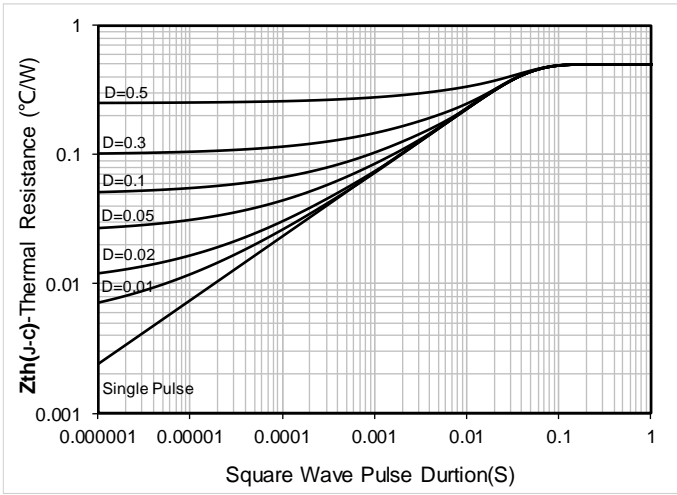


Figure 13. Maximum Transient Thermal Impedance

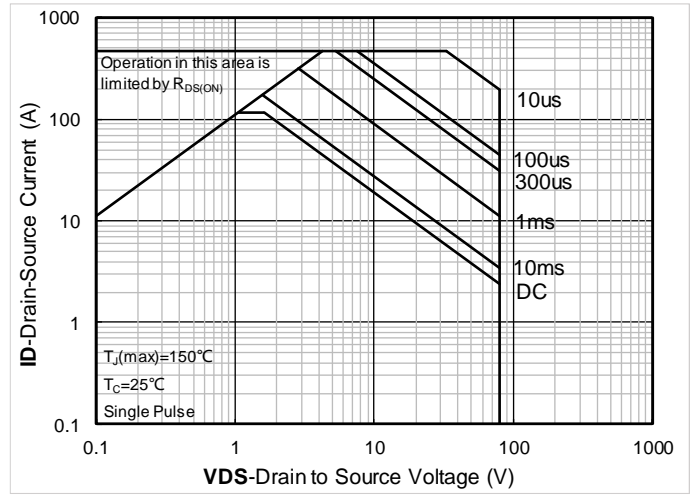


Figure 14. Safe Operation Area

Test Circuits & Waveforms

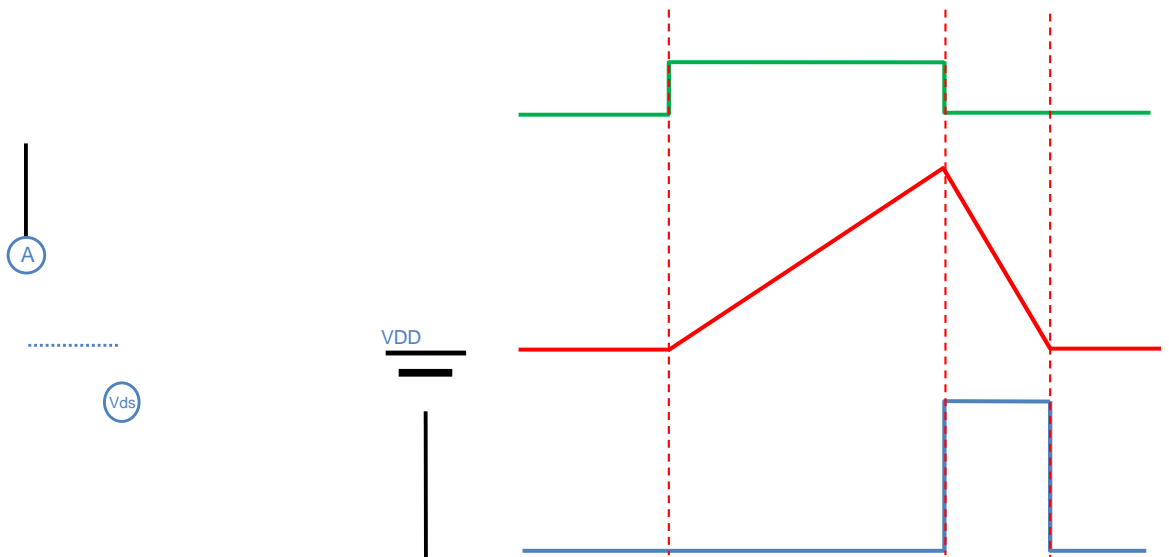


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

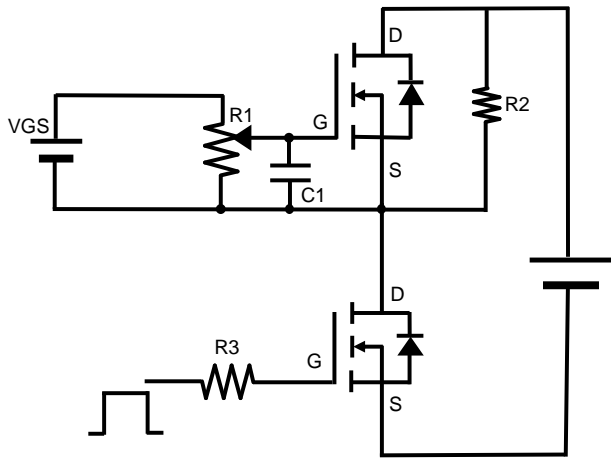


Figure B. Gate Charge Test Circuit & Waveform

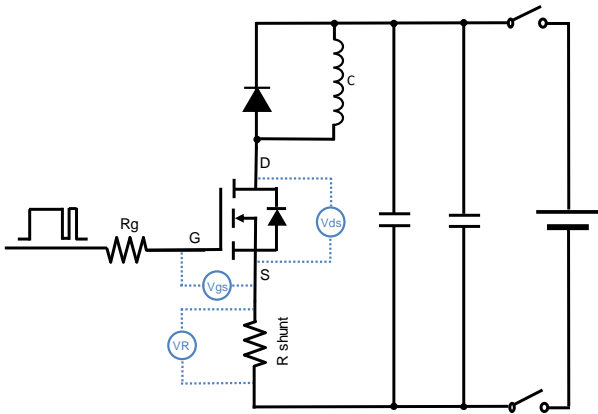


Figure C. Resistive Switching Test Circuit & Waveform

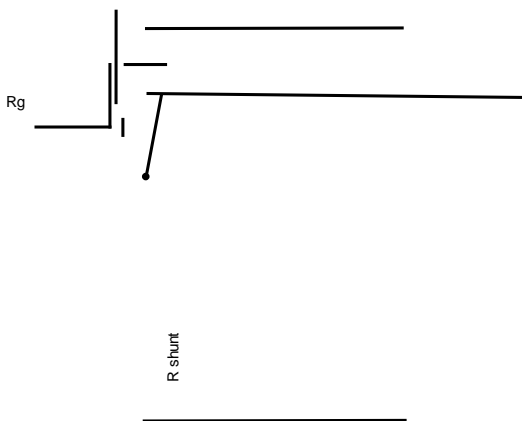
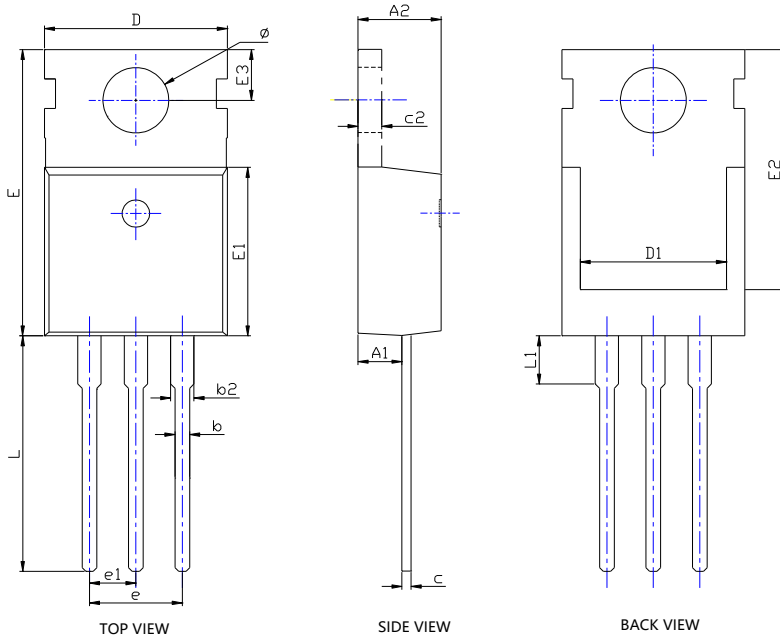


Figure D. Diode Recovery Test Circuit & Waveform



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TO-220AB-D Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A1	0.091	0.098	2.300	2.500
A2	0.175	0.183	4.450	4.650
b	0.030	0.033	0.750	0.850
b2	0.048	0.052	1.220	1.320
c	0.018	0.022	0.450	0.550
c2	0.050	0.052	1.270	1.330
D	0.386	0.402	9.800	10.200
D1	0.303	0.327	7.700	8.300
E	0.614	0.630	15.600	16.000
E1	0.360	0.372	9.150	9.450
E2	0.510	0.533	12.950	13.550
E3	0.110BSC		2.800BSC	
e	0.200BSC		5.080BSC	
e1	0.100BSC		2.540BSC	
L	0.506	0.518	12.850	13.150
L1	0.093	0.117	2.360	2.960
ϕ	0.138	0.146	3.500	3.700

NOTE:
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.



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