



YJP30GP10A

P-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	-100V
I_D	-30A
$R_{DS(ON)}$ (at $V_{GS}=-10V$)	56 mohm
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	62 mohm
100% EAS Tested	
100% V_{DS} Tested	

General Description

Split gate trench MOSFET technology
Excellent package for heat dissipation
High density cell cety cel



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Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-100V, V _{GS} =0V	T _J =25		-1	μA
			T _J =55		-5	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = 20V, V _{DS} =0V			100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-1.0	-1.8	-2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10V, I _D =-15A		42	56	m
		V _{GS} = -4.5V, I _D =-7A		46	62	
Diode Forward Voltage	V _{SD}	I _S =-15A, V _{GS} =0V			-1.3	V
Maximum Body-Diode Continuous Current	I _S				-30	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-50V, V _{GS} =0V, f=1MHZ		2100		pF
Output Capacitance	C _{oss}			236		
Reverse Transfer Capacitance	C _{rss}			48		
Switching Parameters						
Total Gate Charge	Q _{g(-10V)}	V _{GS} =-10V, V _{DS} =-50V, I _D =-5A		40		nC
Total Gate Charge	Q _{g(-4.5V)}			19.4		
Gate-Source Charge	Q _{gs}			7.8		
Gate-Drain Charge	Q _{gd}			8.6		
Reverse Recovery Charge	Q _{rr}	I _F =-5A, di/dt=100A/us		280		
Reverse Recovery Time	t _{rr}			104		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-50V, I _{DS} =-5A R _{GEN} =6		13		ns
Turn-on Rise Time	t _r			39		
Turn-off Delay Time	t _{D(off)}			100.1		
Turn-off fall Time	t _f			105.3		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V_{DD}=50V, R_G=25 , L=0.5mH.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{JA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25 C. The Power dissipation PDSM is based on R_{JA} t_{10s} and the maximum allowed junction temperature of 150 C. The value in any given application depends on the user's specific board design.



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Typical Performance Characteristics

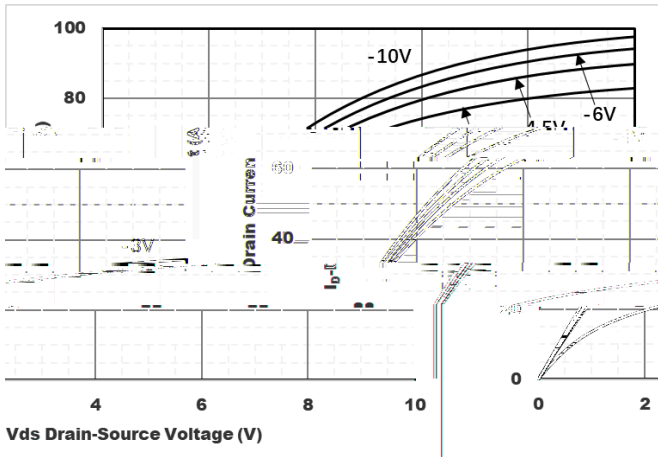


Figure1. Output Characteristics

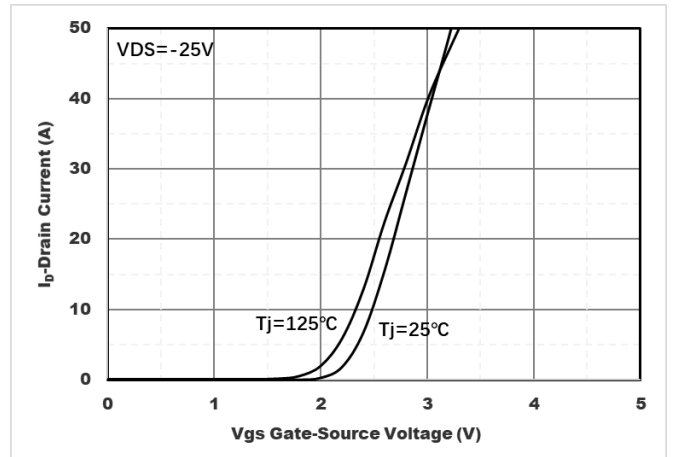


Figure2. Transfer Characteristics

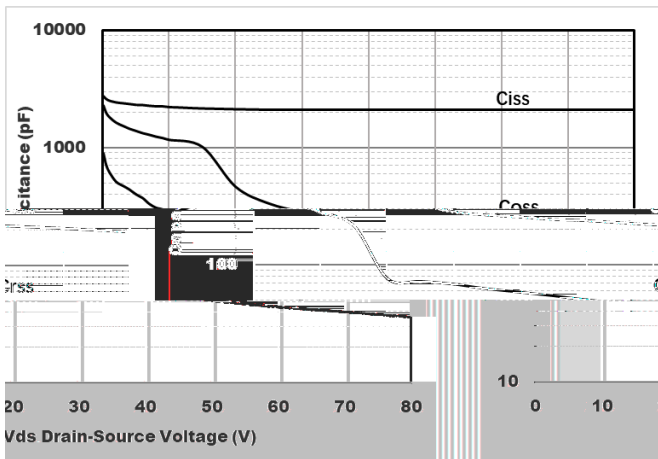


Figure3. Capacitance Characteristics

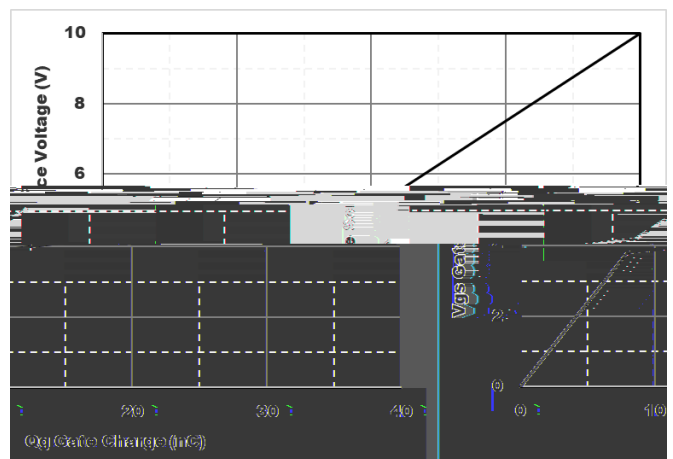


Figure4. Gate Charge

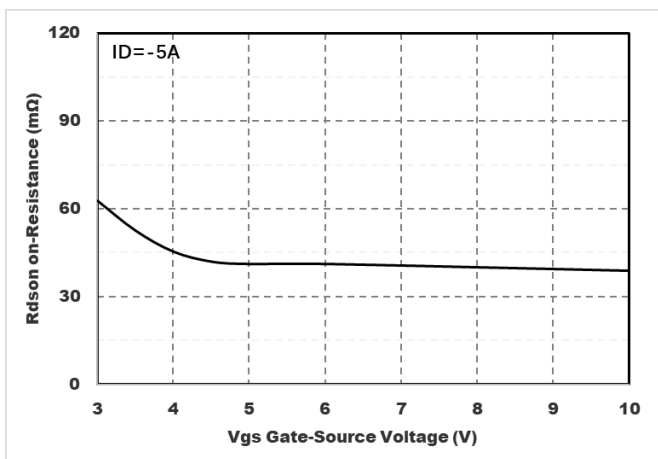


Figure5. On-Resistance vs. Gate to Source Voltage

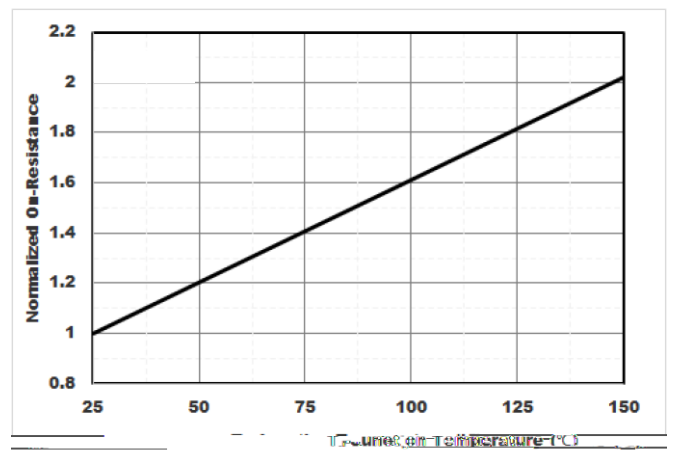


Figure6. Normalized On-Resistance



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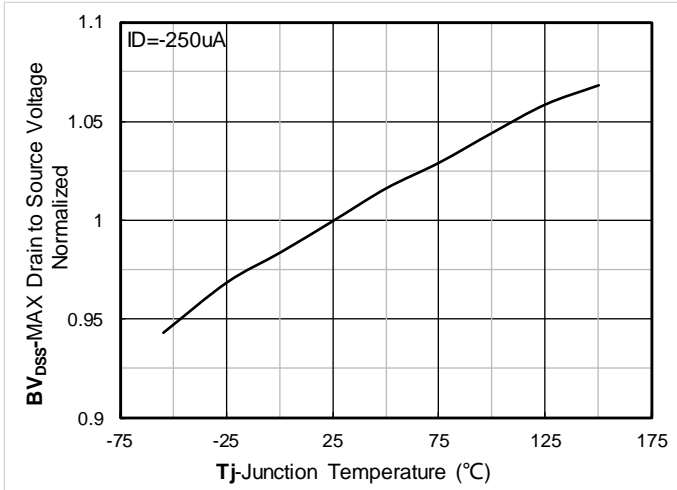


Figure12. Normalized breakdown voltage

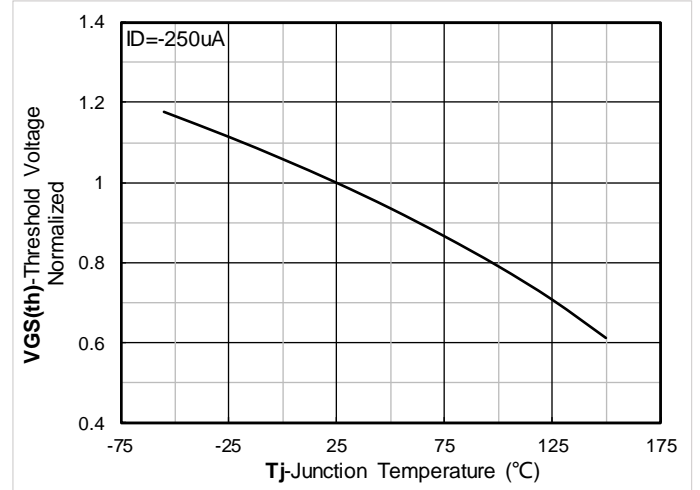


Figure13. Normalized Threshold voltage

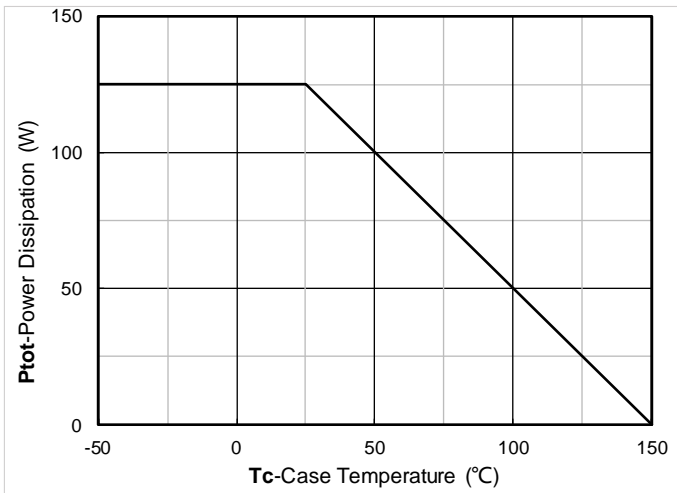


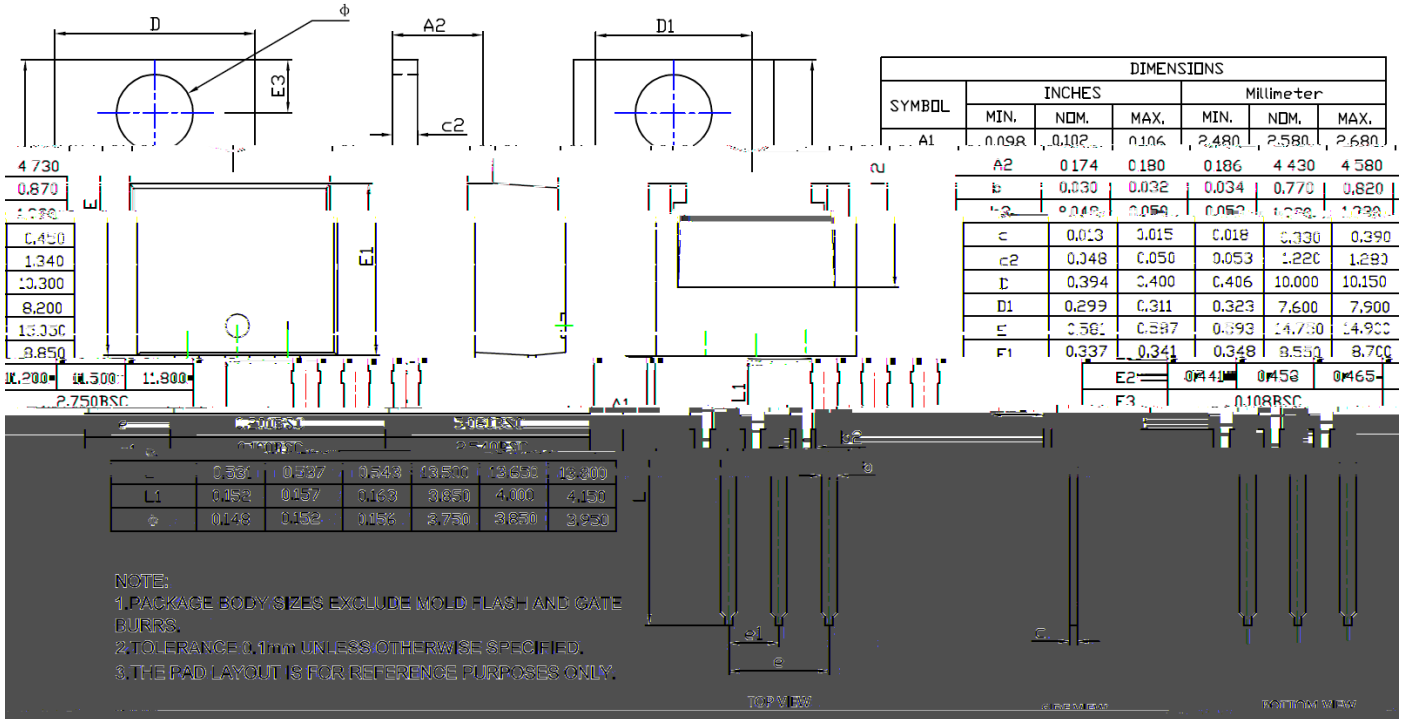
Figure14. Power dissipation



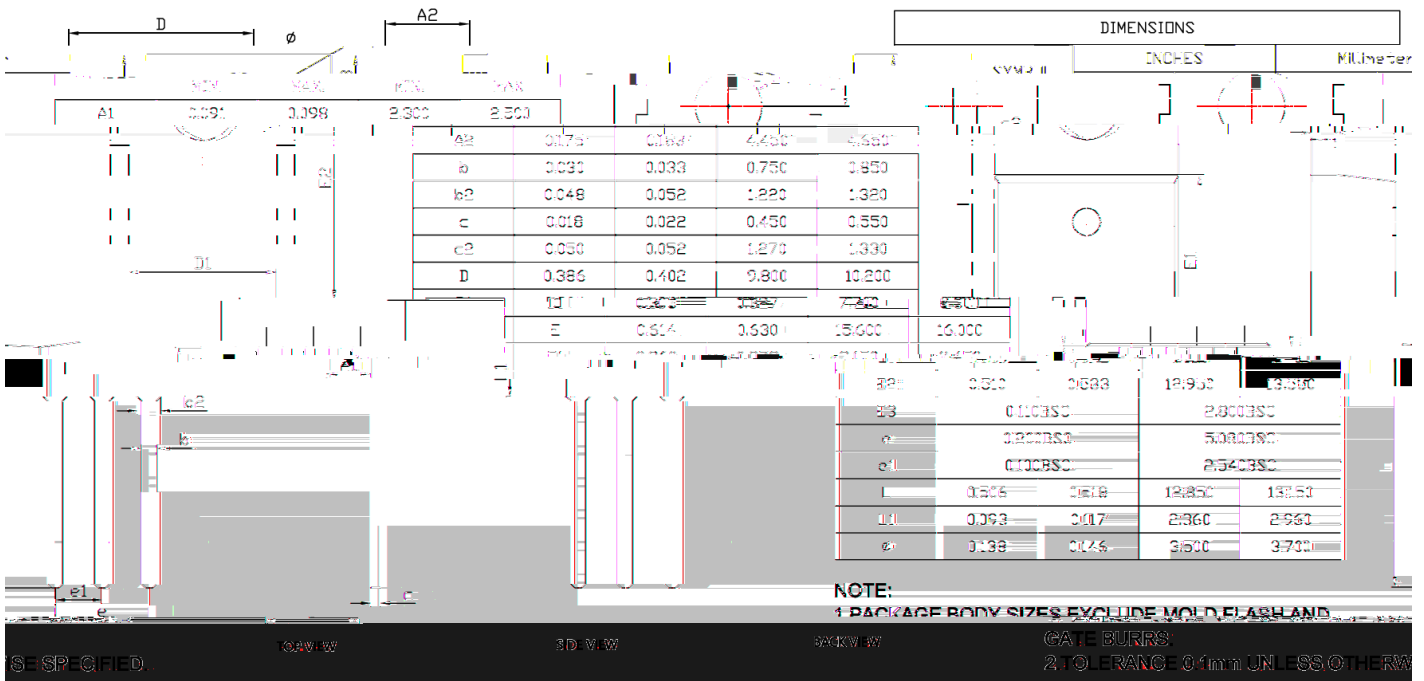
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TO-220AB Package Information

Type B



Type D





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