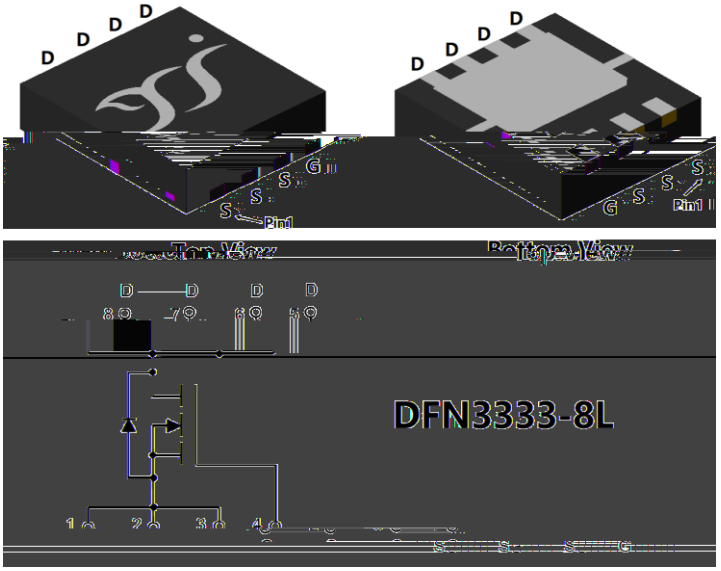
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 100V
- I_D 3A
- $R_{DS(ON)}$(at V_{GS}=10V) 240mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) 250mΩ
- 100% EAS Tested

General Description

- Trench Power MV MOSFET technology
- Voltage controlled small signal switch
- Fast Switching Speed
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- DC-DC convertor

■ Absolute Maximum Ratings (T_A=25 unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	1	A
	T_A=100℃		0.6	
	T_C=25℃		3	
	T_C =100℃		1.9	
Pulsed Drain Current [A]		I_{DM}	10	A
Avalanche energy [B]		EAS	4	mJ
Total Power Dissipation [C]	T_A=25℃	P_D	1.5	W
	T_A=100℃		0.6	
	T_C=25℃		13.8	
	T_C =100℃		5.5	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55 +150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [C]	Steady-State	$R_{\theta JA}$	65	80	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	7.5	9	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ03N10A	F1	Q03N10A	5000	10000	100000	13“ reel

■ **Electrical Characteristics** (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100	-	-	V

Typical Electrical and Thermal Characteristics Diagrams

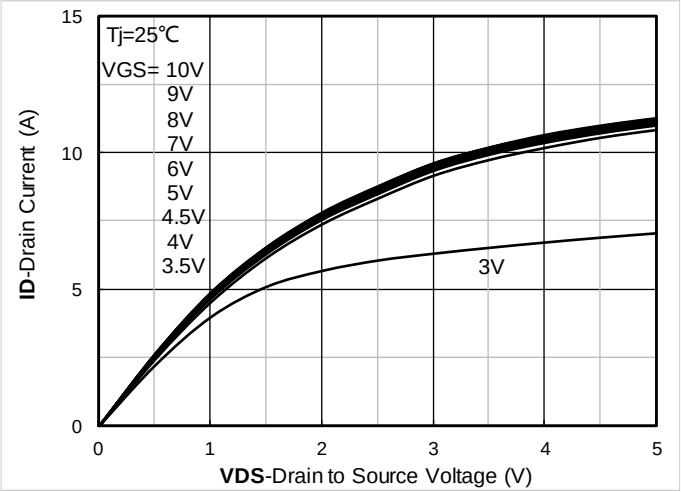


Figure 1. Output Characteristics

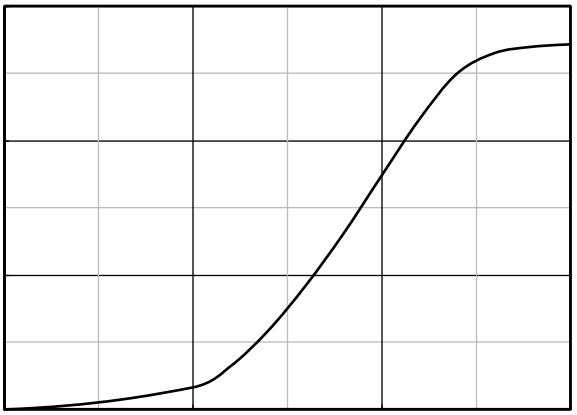


Figure 2. Transfer Characteristics

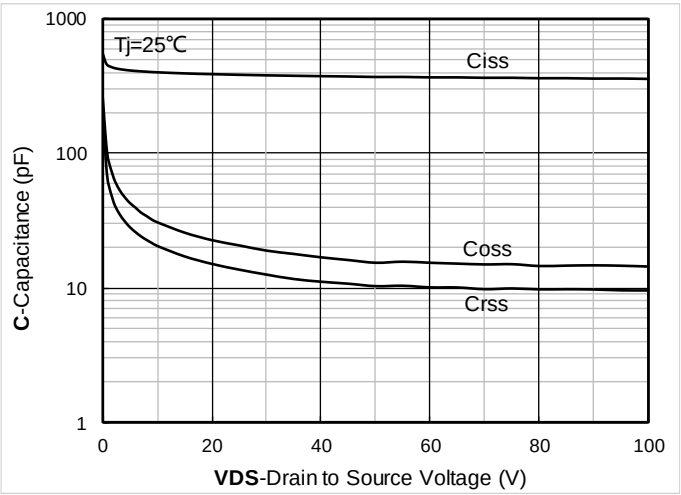


Figure 3. Capacitance Characteristics

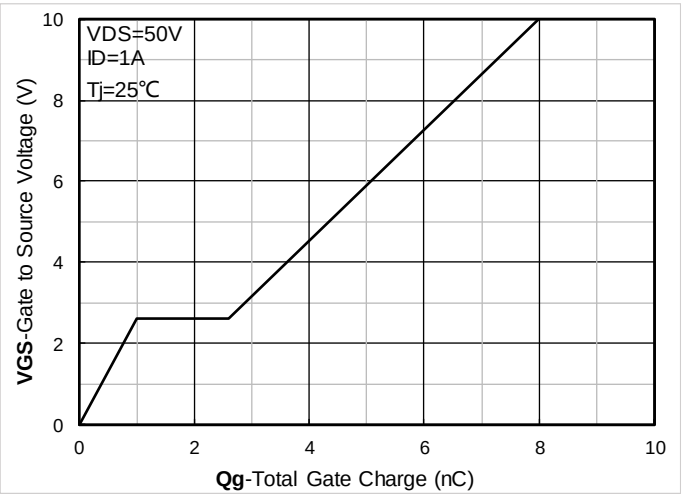


Figure 4. Gate Charge

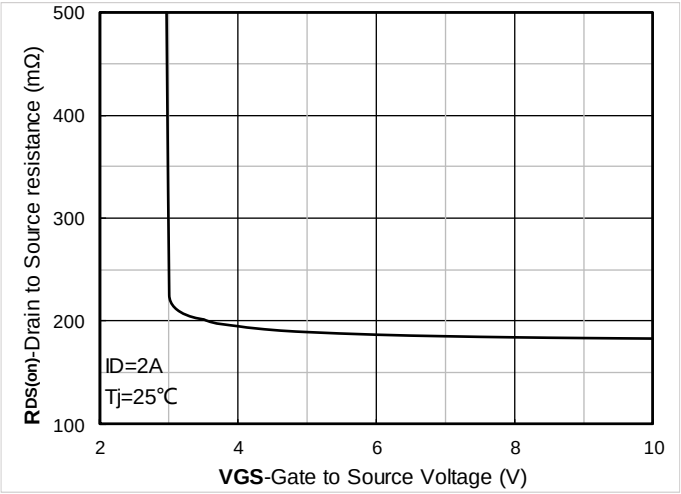


Figure 5. On-Resistance vs Gate to Source Voltage

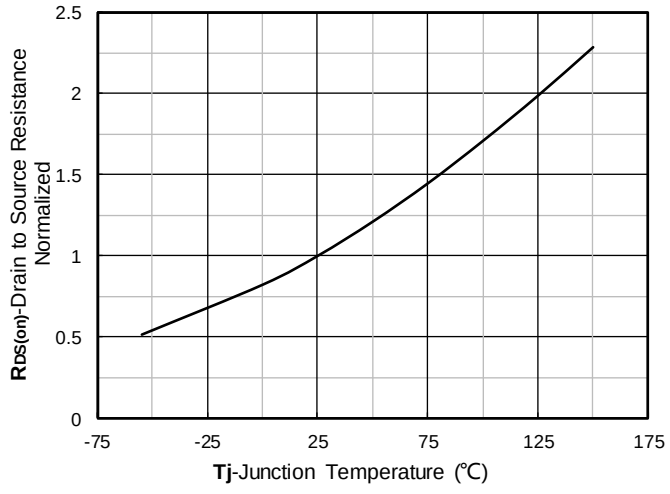


Figure 6. Normalized On-Resistance

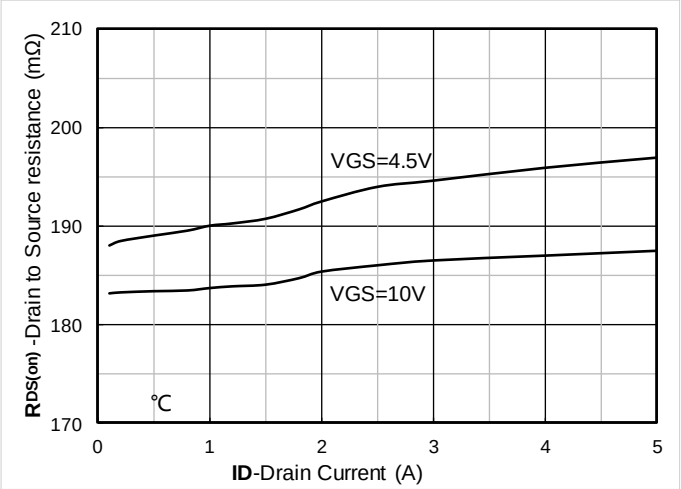


Figure 7. $R_{DS(on)}$ VS Drain Current

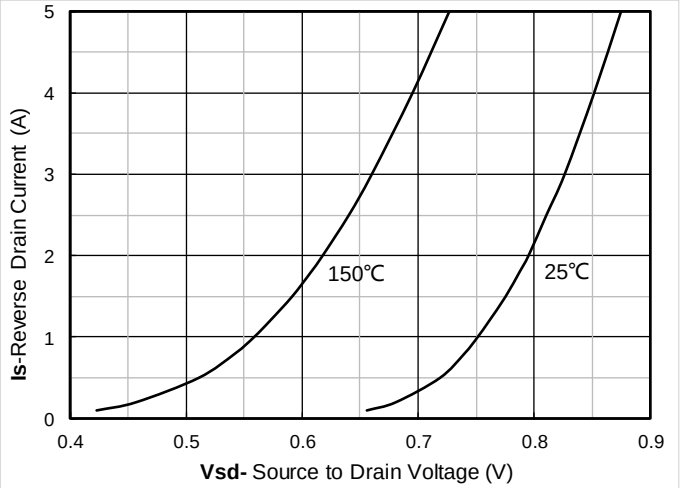


Figure 8. Forward characteristics of reverse diode

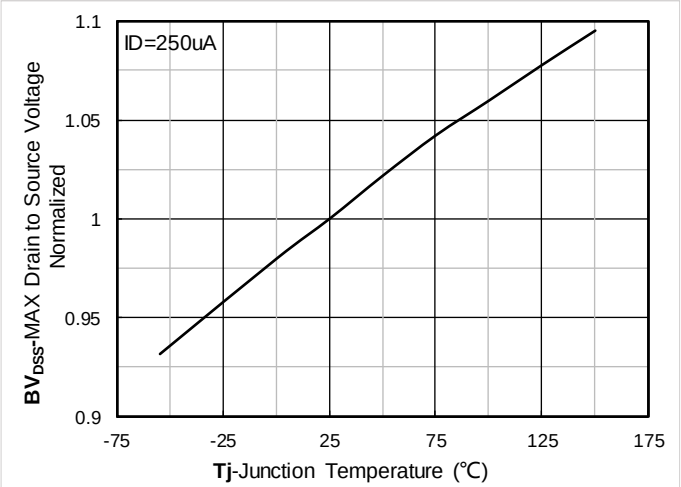


Figure 9. Normalized breakdown voltage

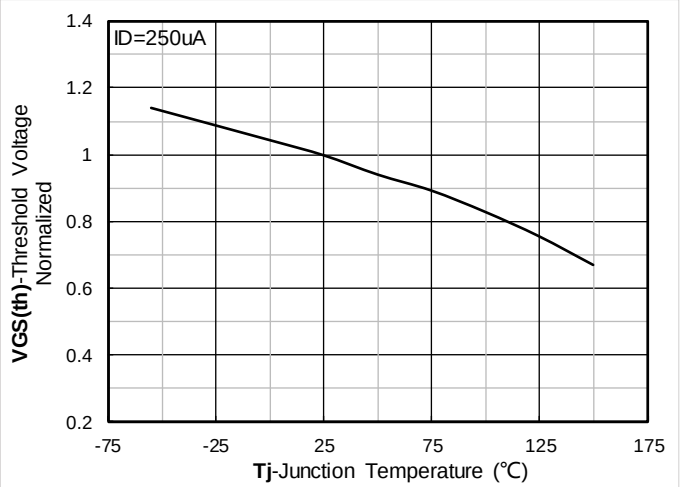


Figure 10. Normalized Threshold voltage

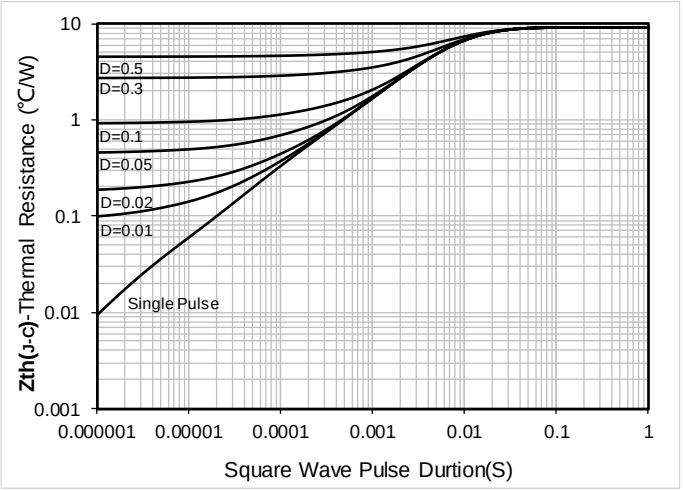


Figure 13. Maximum Transient Thermal Impedance

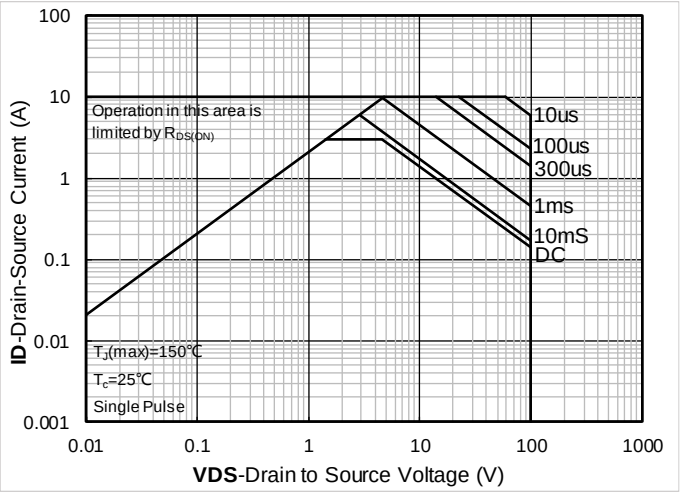
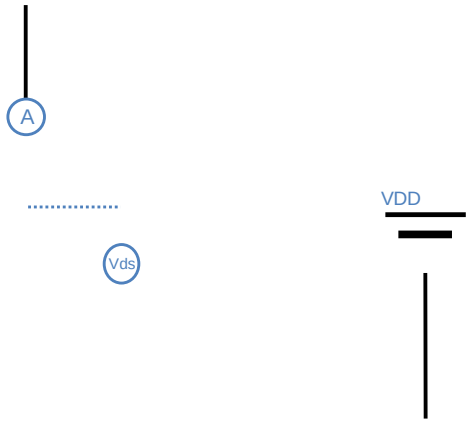


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms



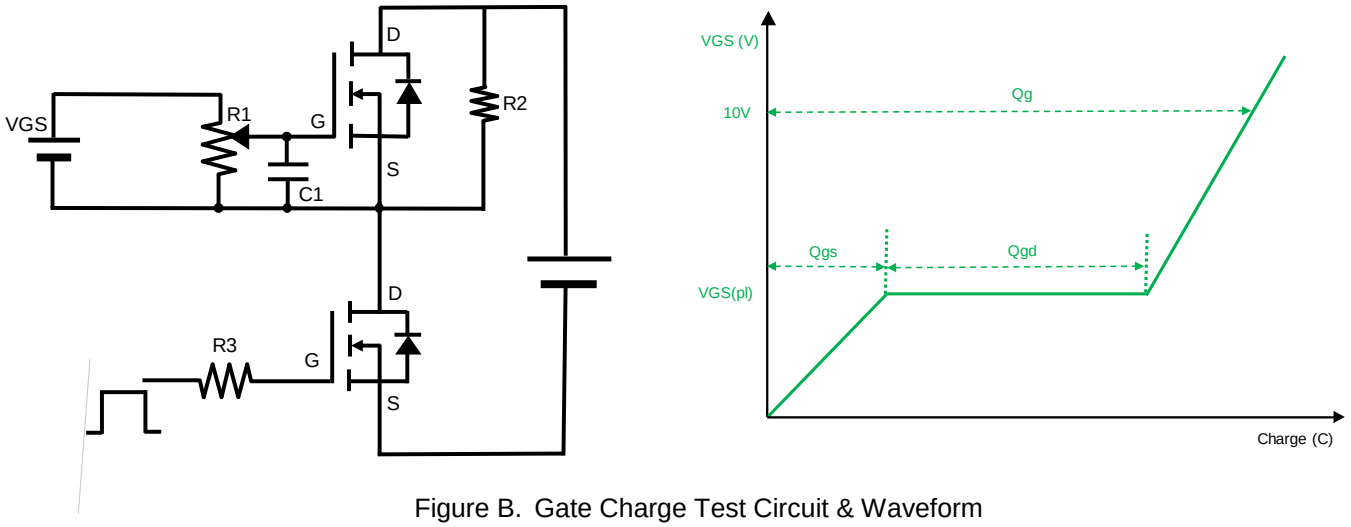
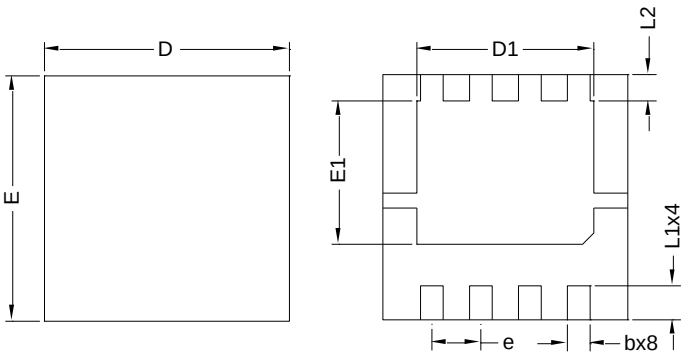


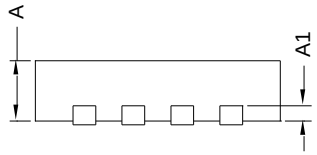
Figure B. Gate Charge Test Circuit & Waveform

■ DFN3333-8L-A-0.8MM Package information

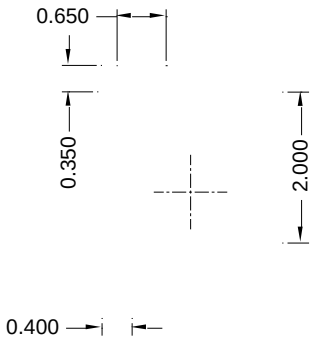


Top View　　Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1		0.20 BSC	
A2			



Side View



Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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