



N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	60V
I_D	18A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	29m
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	35m
100% EAS Tested	

General Description

Trench Power LV MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Moisture Sensitivity Level 1
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications



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Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
		$V_{DS}=60V, V_{GS}=0V, T_J=150$	-	-	100	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=18A$	-	22	29	m
		$V_{GS}=4.5V, I_D=15A$	-	26	35	
Diode Forward Voltage	V_{SD}	$I_S=18A, V_{GS}=0V$	-	-	1.2	V
Gate resistance	R_G	$f=1MHz$	-	1.6	-	
Maximum Body-Diode Continuous Current	I_S		-	-	18	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V, f=1MHz$	-	1180	-	pF
Output Capacitance	C_{oss}		-	65	-	
Reverse Transfer Capacitance	C_{rss}		-	55	-	
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=30V, I_D=20A$	-	23	-	nC
Gate-Source Charge	Q_{gs}		-	3	-	
Gate-Drain Charge	Q_{gd}		-	6	-	
Reverse Recovery Charge	Q_{rr}	$I_F=20A, di/dt=100A/us$	-	17.5	-	nC
Reverse Recovery Time	t_{rr}		-	23.5	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=30V, I_D=20A$ $R_{GEN}=2.2$	-	5	-	ns
Turn-on Rise Time	t_r		-	45	-	
Turn-off Delay Time	$t_{D(off)}$		-	19	-	
Turn-off fall Time	t_f		-	2	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. $T_J=25$, $V_G=10V$, $R_G=25$, $L=0.5mH$, $I_{AS}=12A$.

C. P_d is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{JA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with $T_A=25$. The maximum allowed junction temperature of 150. The value in any given application depends on the user's specific board design.



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Typical Electrical and Thermal Characteristics Diagrams

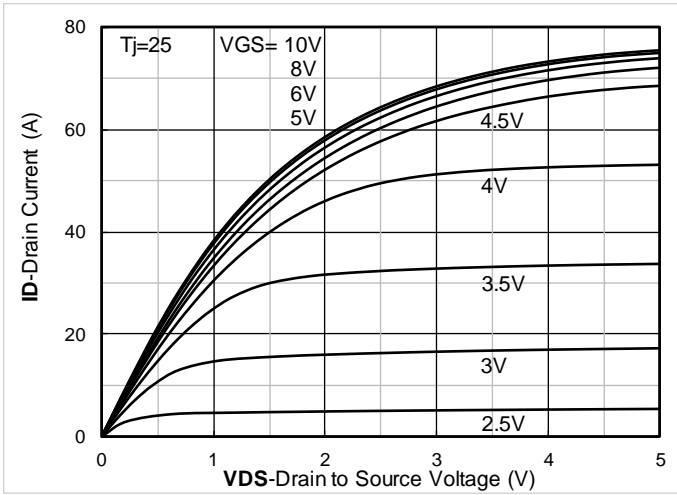


Figure 1. Output Characteristics

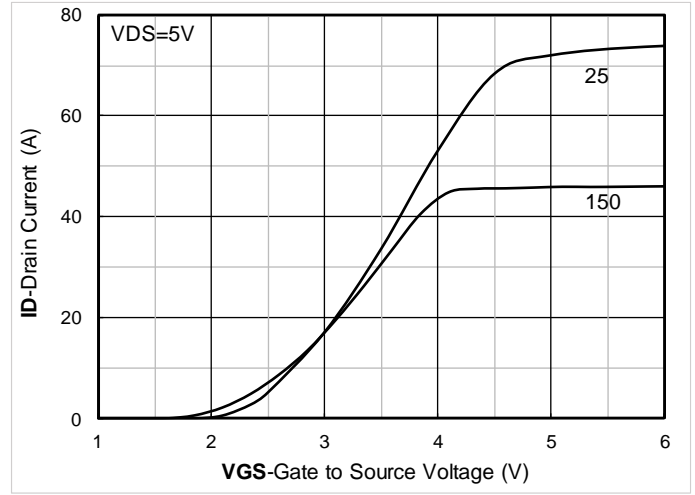


Figure 2. Transfer Characteristics

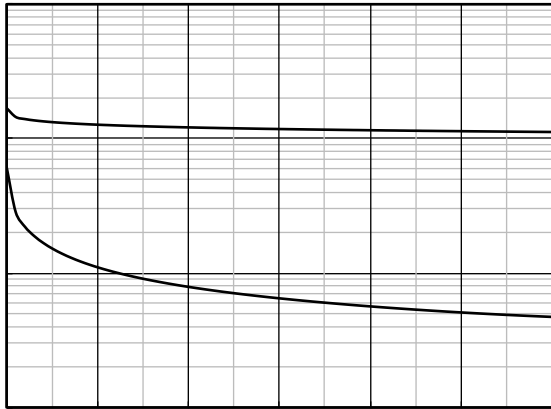


Figure 3. Capacitance Characteristics

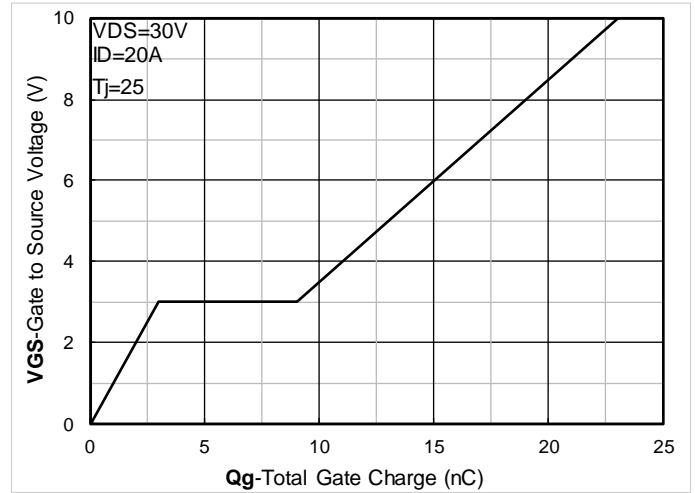


Figure 4. Gate Charge

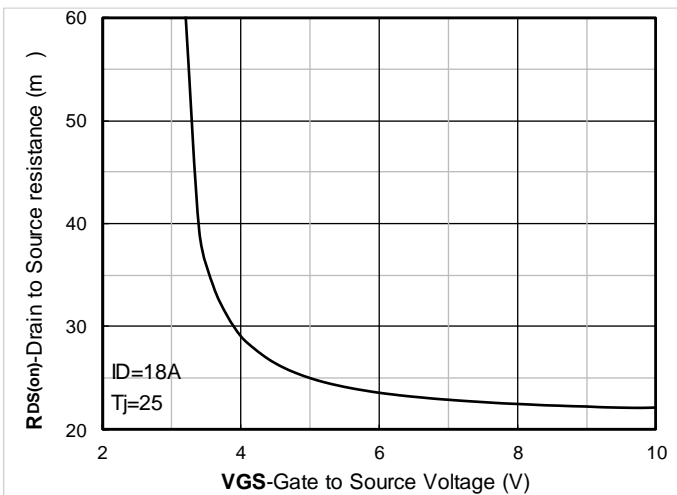


Figure 5. On-Resistance vs Gate to Source Voltage

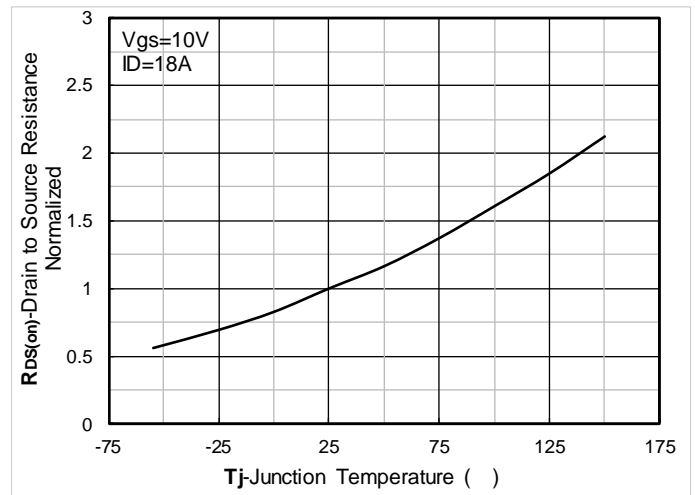


Figure 6. Normalized On-Resistance



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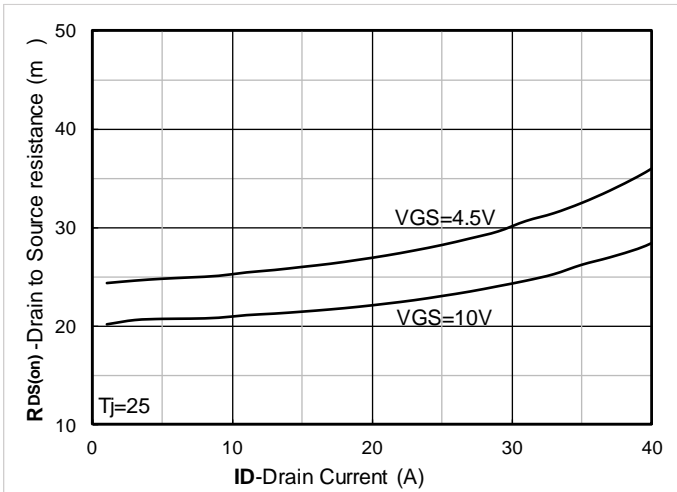


Figure 7. $R_{DS(on)}$ VS Drain Current

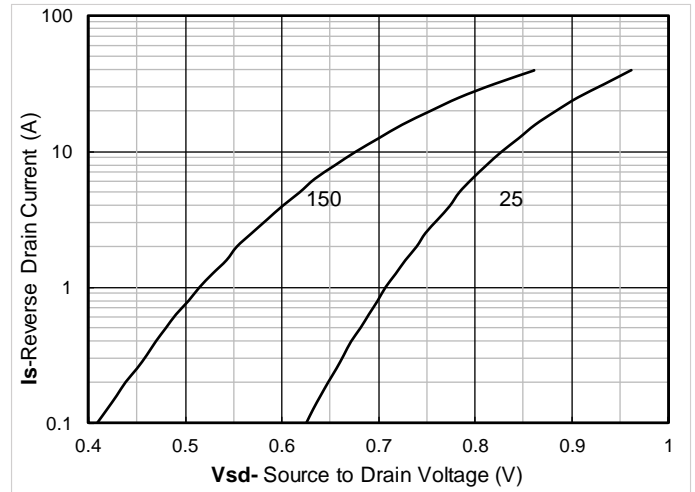


Figure 8. Forward characteristics of reverse diode

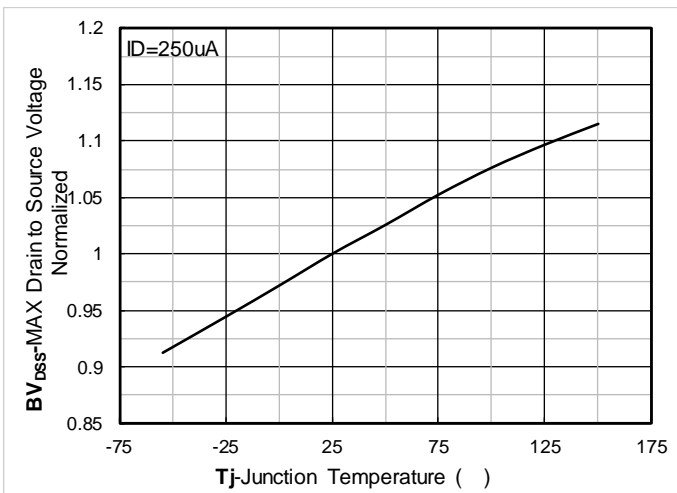


Figure 9. Normalized breakdown voltage

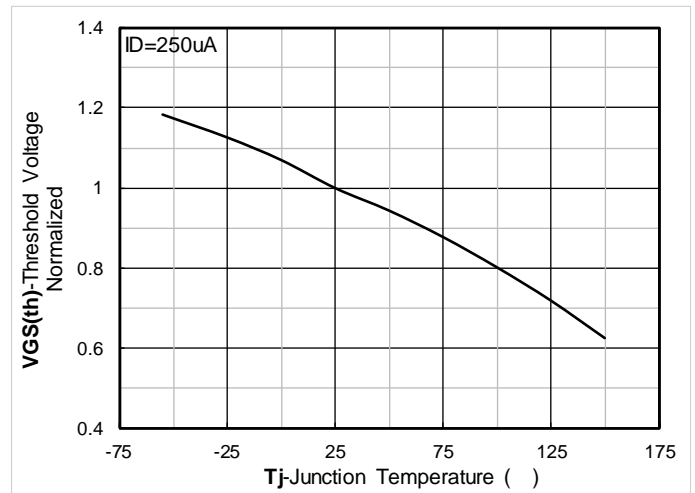


Figure 10. Normalized Threshold voltage

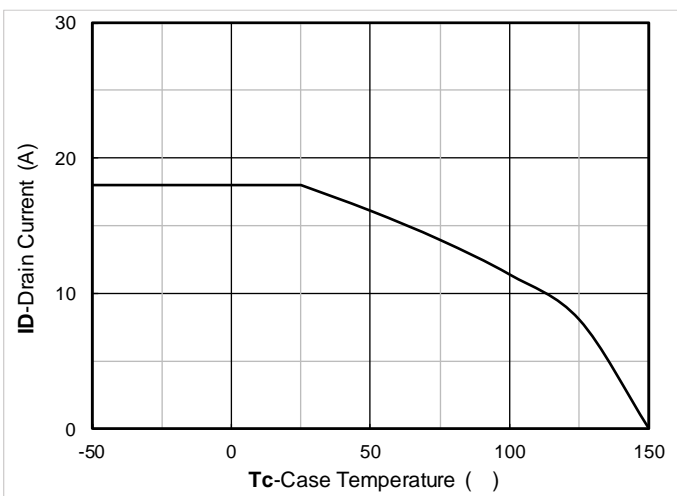


Figure 11. Current dissipation

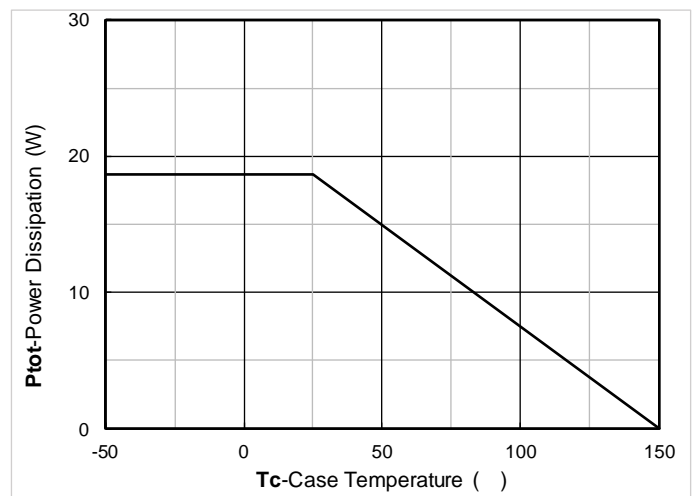


Figure 12. Power dissipation



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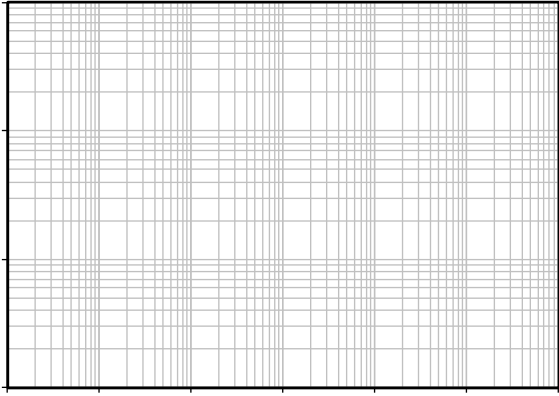


Figure 13. Maximum Transient Thermal Impedance

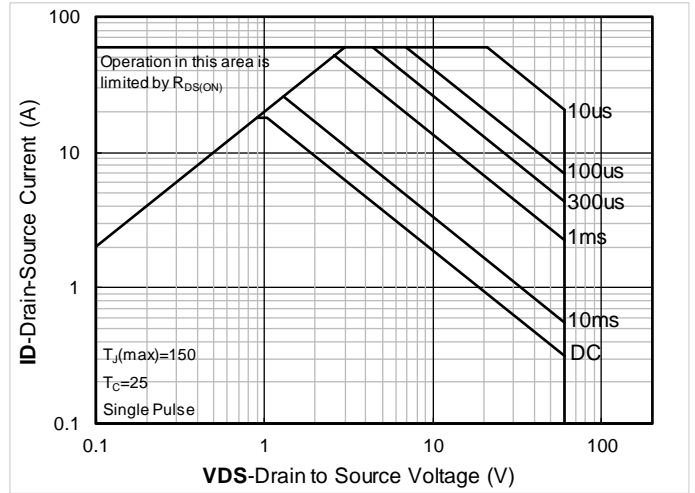


Figure 14. Safe Operation Area

Test Circuits & Waveforms

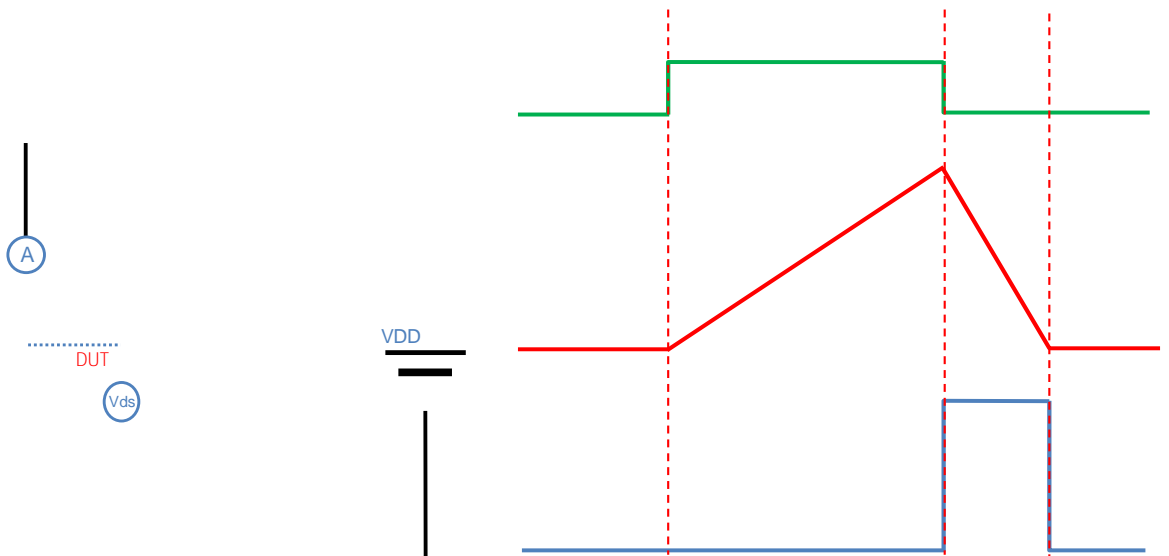


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

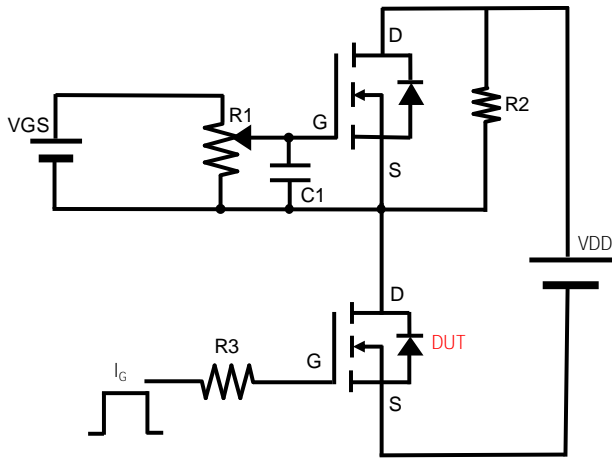


Figure B. Gate Charge Test Circuit & Waveform

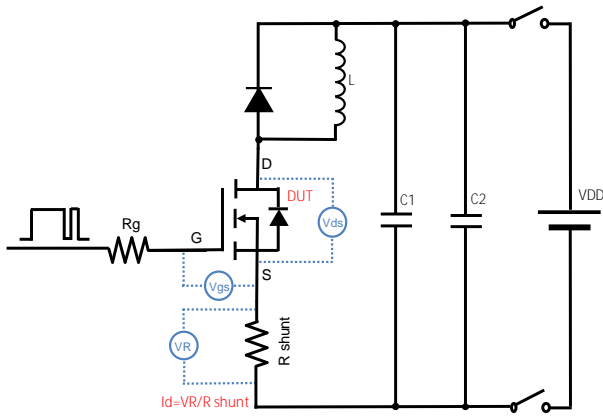


Figure C. Resistive Switching Test Circuit & Waveform

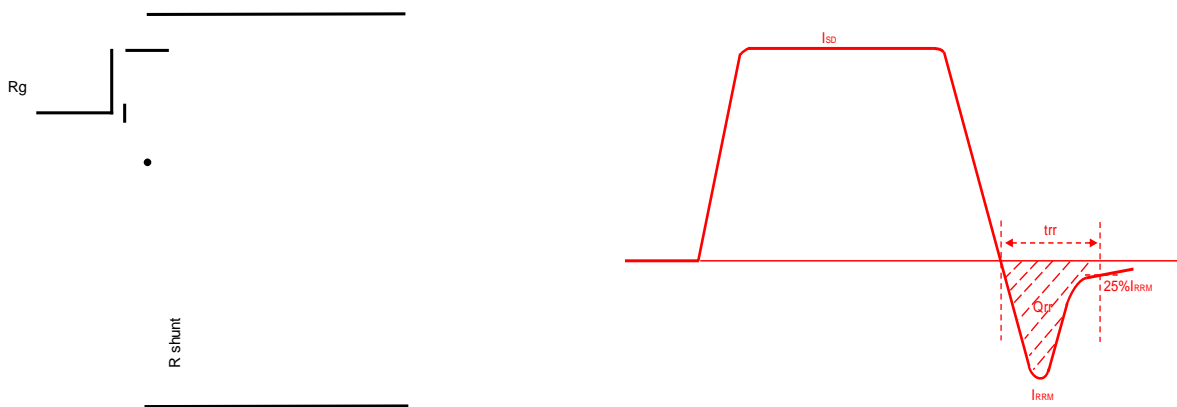
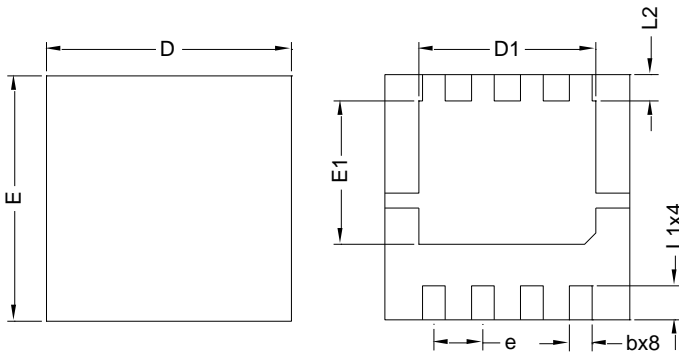


Figure D. Diode Recovery Test Circuit & Waveform



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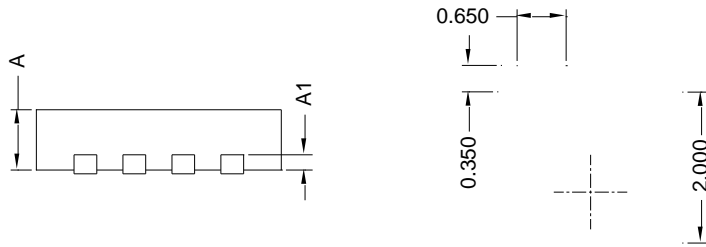
DFN3333-8L-A-0.8MM Package information



Top View

Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1		0.20 BSC	



Side View

0.400

Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



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