

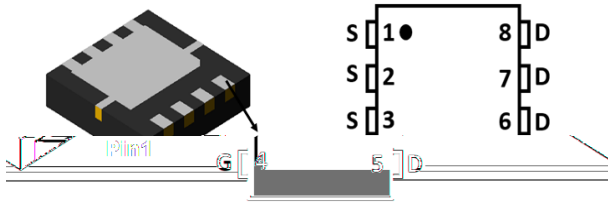


# YJQ35N04A

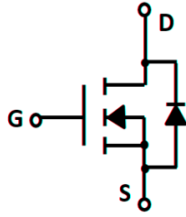
## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	40 V
$I_D$	35 A
$r_{DS(ON)}$ (at $V_{GS} = 10V$ )	8 $\Omega$



3.3X3.3



DFN



# YJQ35N04A

## Electrical Characteristics (T<sub>J</sub>=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250	40			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V			1	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = 20V, V <sub>DS</sub> =0V			100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =20A		6.5	8.0	m
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =10A		8.7	13	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V		0.7	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				35	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1MHZ		1860		pF
Output Capacitance	C <sub>oss</sub>			256		
Reverse Transfer Capacitance	C <sub>rss</sub>			205		
Gate Resistance	R <sub>g</sub>	f= 1MHZ		1.5	2	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =20A		46.7		nC
Gate-Source Charge	Q <sub>gs</sub>			8		
Gate-Drain Charge	Q <sub>gd</sub>			11.6		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =20A, di/dt=100A/us		2.3		
Reverse Recovery Time	t <sub>rr</sub>			15		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =2A, R <sub>L</sub> =1 R <sub>GEN</sub> =3		10		ns
Turn-on Rise Time	t <sub>r</sub>			21		
Turn-off Delay Time	t <sub>D(off)</sub>			36		
Turn-off fall Time	t <sub>f</sub>			25		

A. Pulse Test: Pulse Width 300us, Duty cycle 2%.

B. R<sub>JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>JC</sub> is guaranteed by design, while R<sub>JA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



## Typical Performance Characteristics

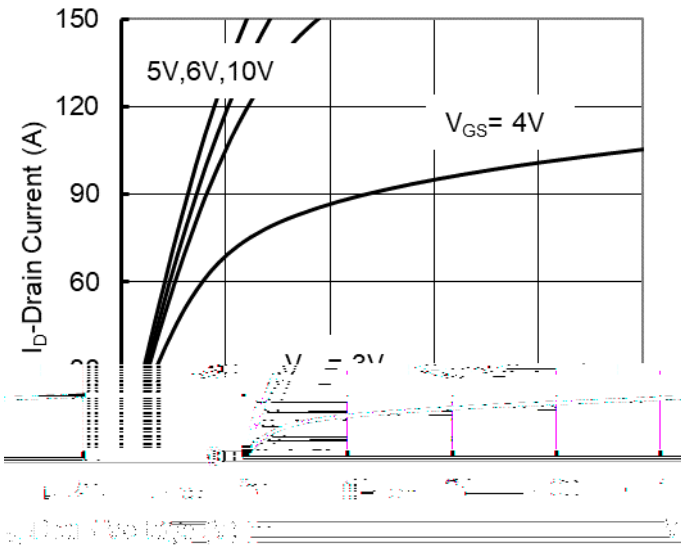


Figure 1. Output Characteristics

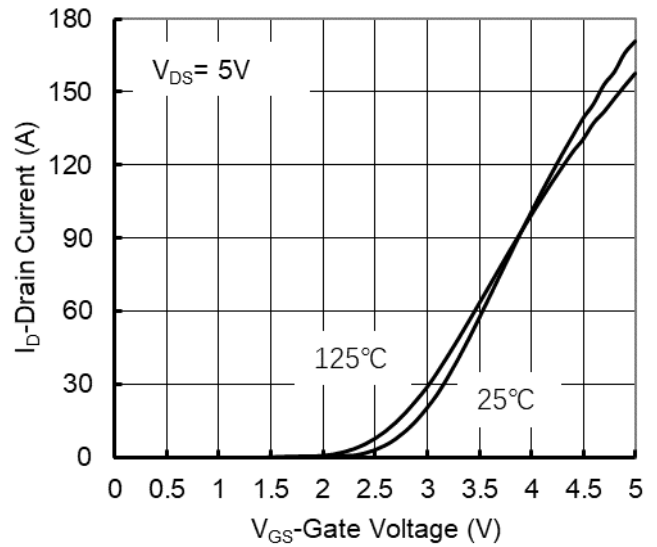


Figure 2. Transfer Characteristics

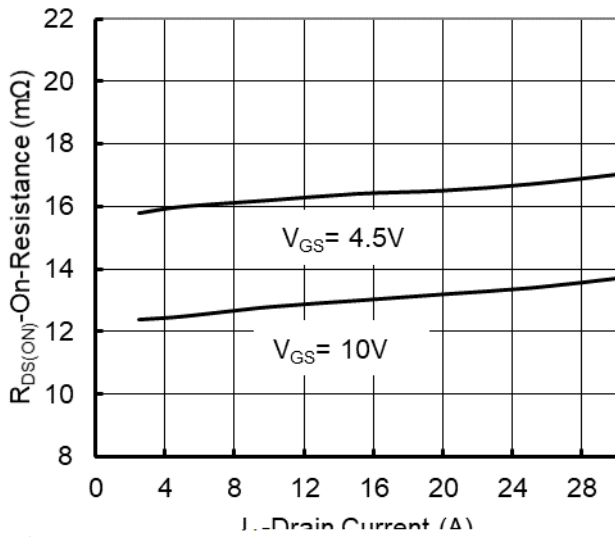


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

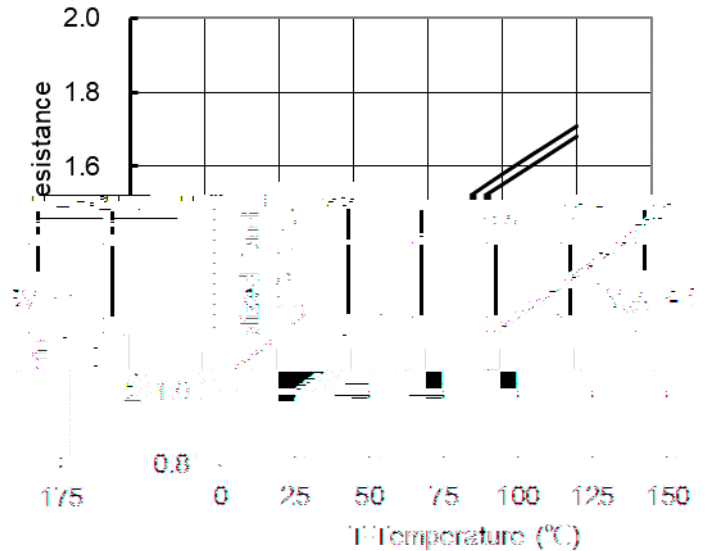


Figure 4. On-Resistance vs. Junction Temperature

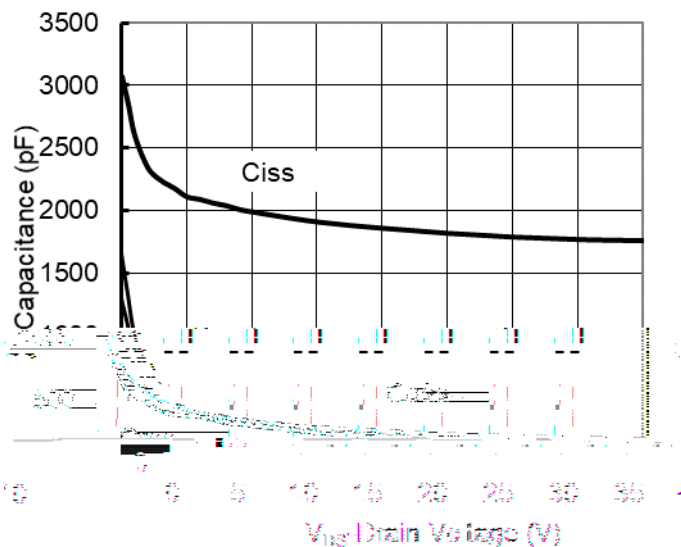


Figure 5. Capacitance Characteristics

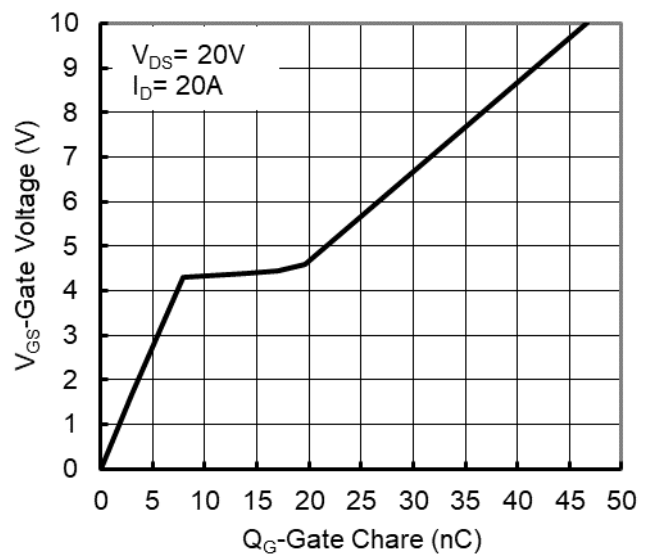


Figure 6. Gate Charge



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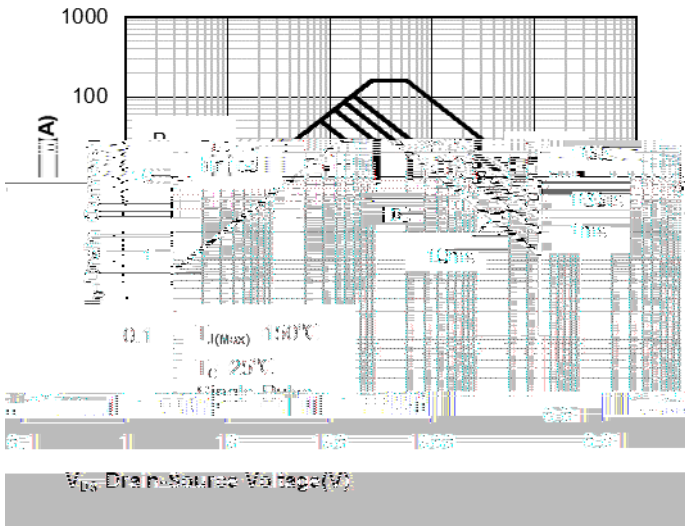


Figure 7. Safe Operation Area

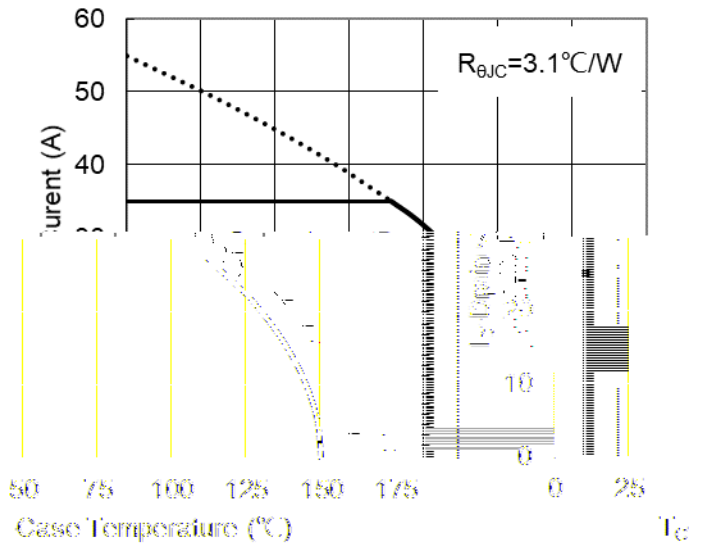


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

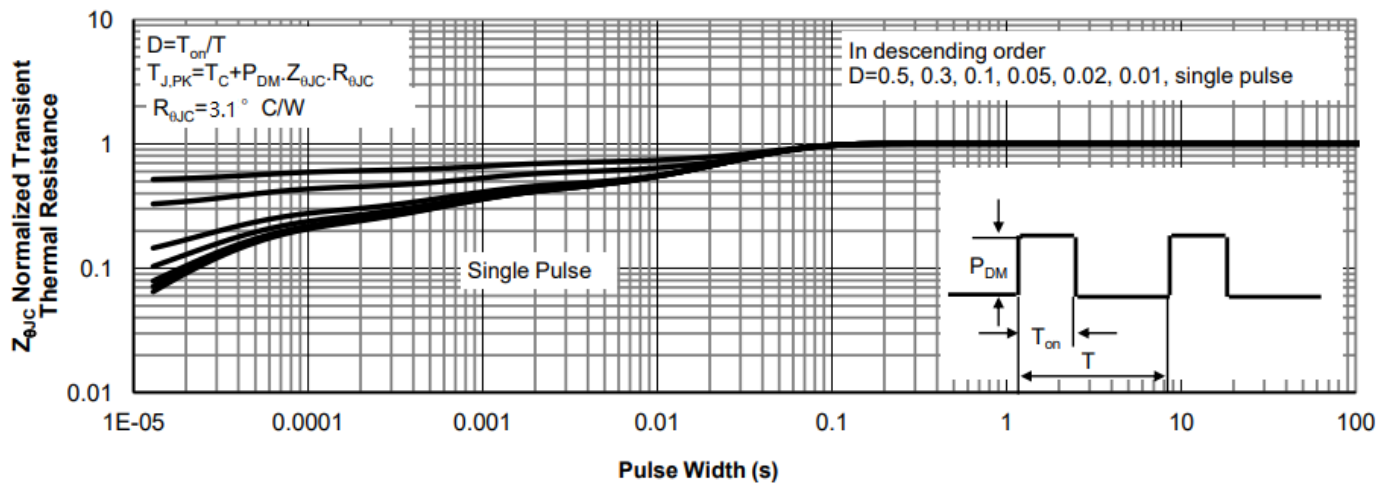
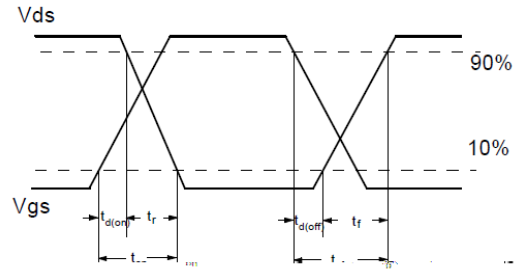
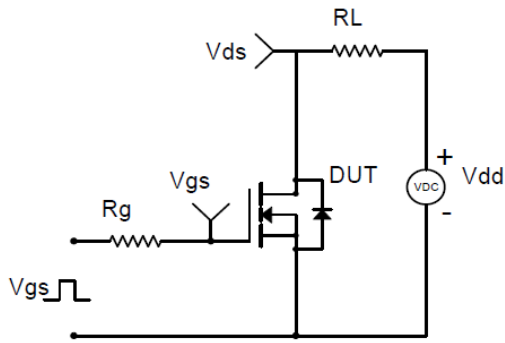
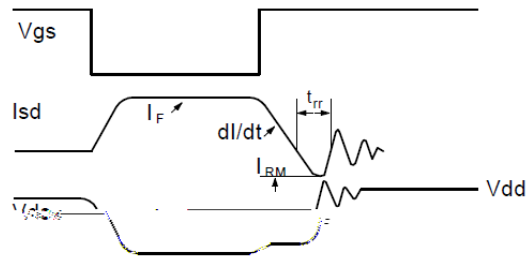
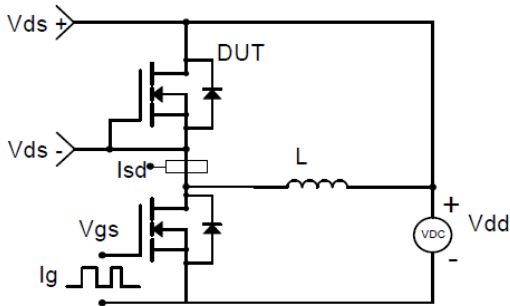


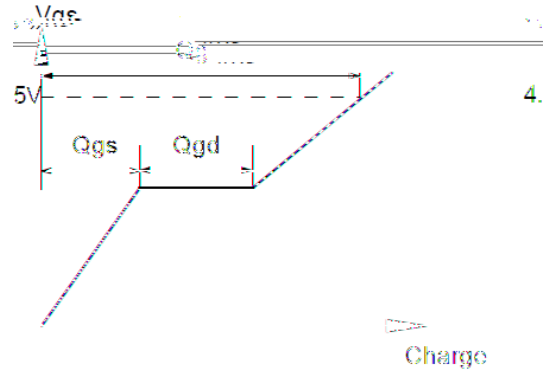
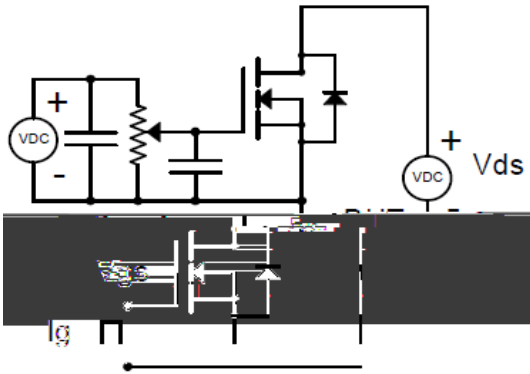
Figure 9. Normalized Maximum Transient Thermal Impedance



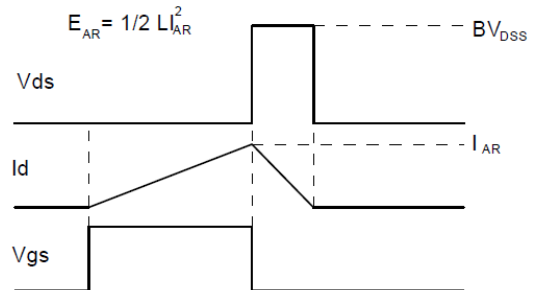
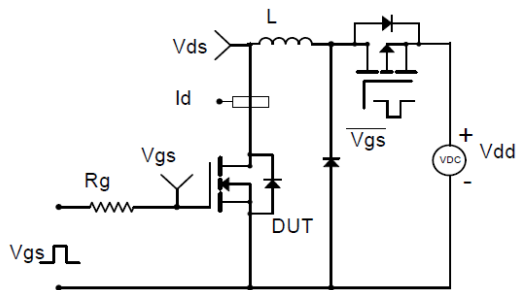
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



**DFN3.3X3.3 Package information**



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