



YJQ40G10A

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	100V
I_D	40A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	18.5 mohm
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	22.5 mohm
100% EAS Tested	

General Description

Split gate trench MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Moisture Sensitivity Level 3
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

Consumer electronic power supply
Motor control
Synchronous-rectification
Isolated DC/DC convertor
Invertors

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	20	V
Drain Current	$T_A=25^{\circ}C$	I_D	8	A
	$T_A=100^{\circ}C$		5	
	$T_C=25^{\circ}C$		40	
	$T_C=100^{\circ}C$		25.3	
Pulsed Drain Current ^A		I_{DM}	160	A
Avalanche energy ^B		EAS	81	mJ
Total Power Dissipation ^C	$T_A=25^{\circ}C$	P_D	2	W
	$T_A=100^{\circ}C$		0.9	
	$T_C=25^{\circ}C$		43	



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Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V			1	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = 20V, V _{DS} =0V			100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		15	18.5	m
		V _{GS} =4.5V, I _D =20A		18	22.5	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V			1.3	V
Maximum Body-Diode Continuous Current	I _S				40	A
Gate resistance	R _G	f=1MHz, Open drain		1		
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHZ		1051		pF
Output Capacitance	C _{oss}			399		
Reverse Transfer Capacitance	C _{rss}			18		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =25A		16		nC
Gate-Source Charge	Q _{gs}			5.6		
Gate-Drain Charge	Q _{gd}			2.4		
Reverse Recovery Charge	Q _{rr}	I _r =20A, di/dt=100A/us		42		
Reverse Recovery Time	t _{rr}			39.8		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _{DS} =25A R _{GEN} =2.2		39.2		ns
Turn-on Rise Time	t _r			11		
Turn-off Delay Time	t _{D(off)}			53.2		
Turn-off fall Time	t _f			15.8		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V_{DD}=50V, R_G , / & 2mH, I_{AS}=9A

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. + , -4 board with 2oz. Copper, in a still air environment with T_A =25 C. The temperature of 150 C. The value in any given application depends on the user's specific board design.



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Typical Performance Characteristics

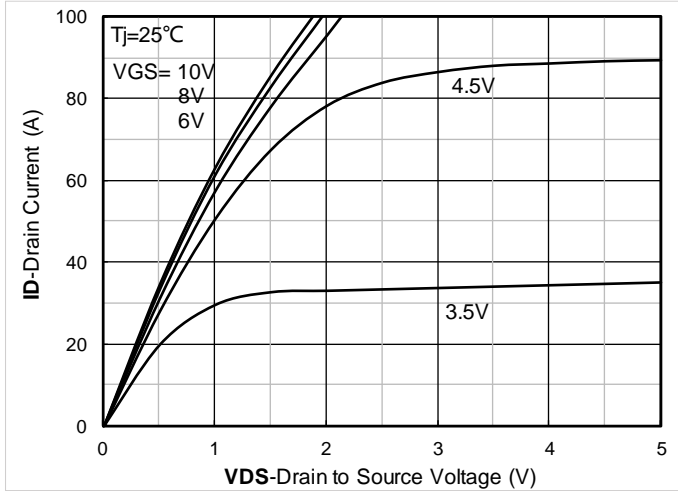


Figure1. Output Characteristics

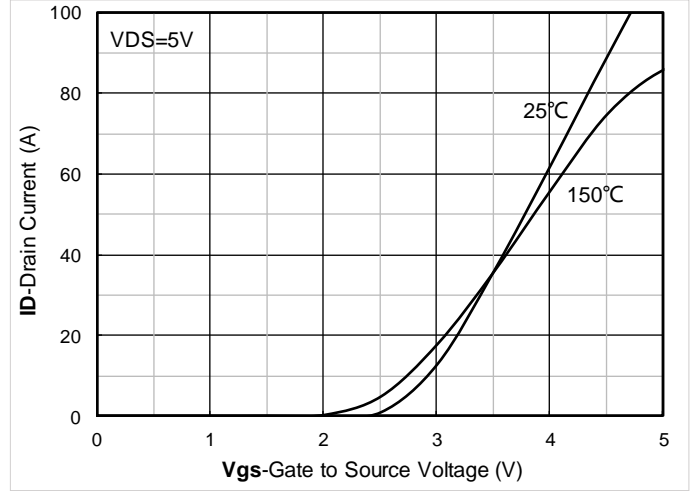


Figure2. Transfer Characteristics



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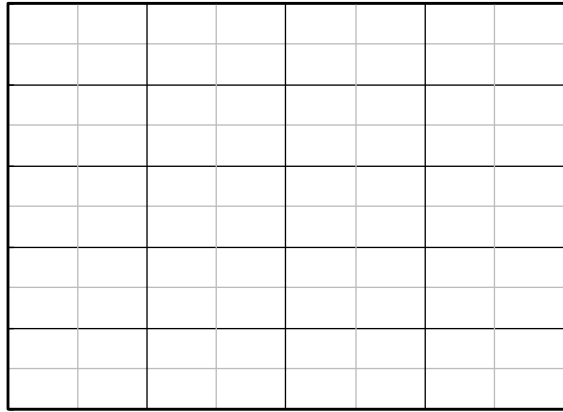


Figure 7. Drain current

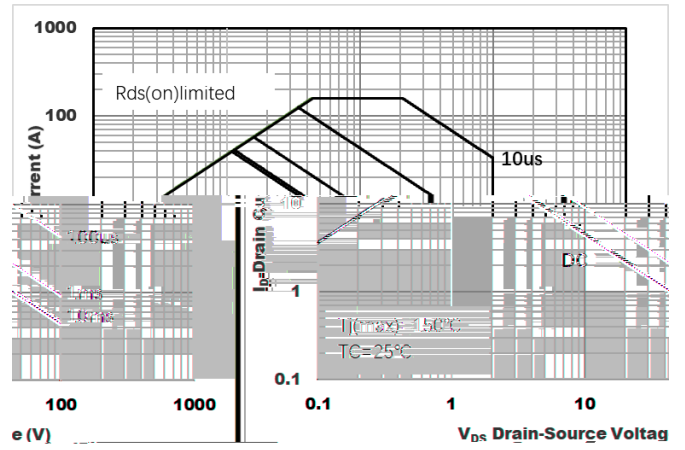


Figure 8. Safe Operation Area

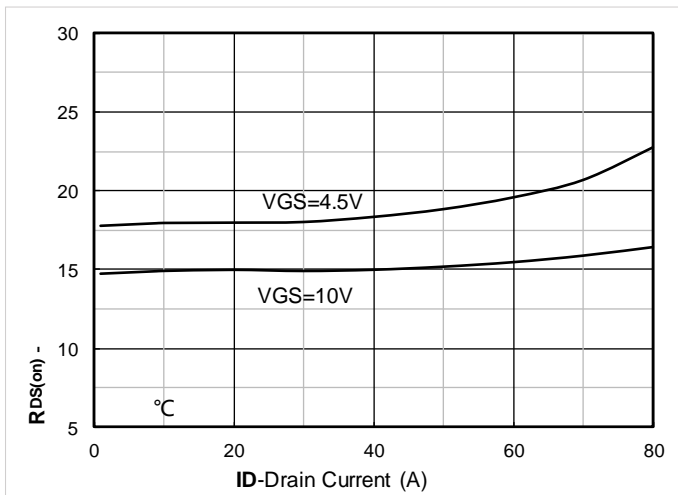


Figure 9. $R_{DS(on)}$ VS Drain Current

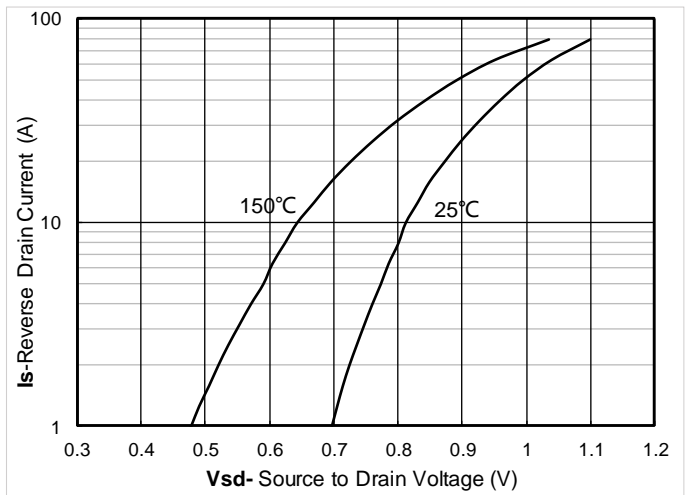


Figure 10. Forward characteristics of reverse diode

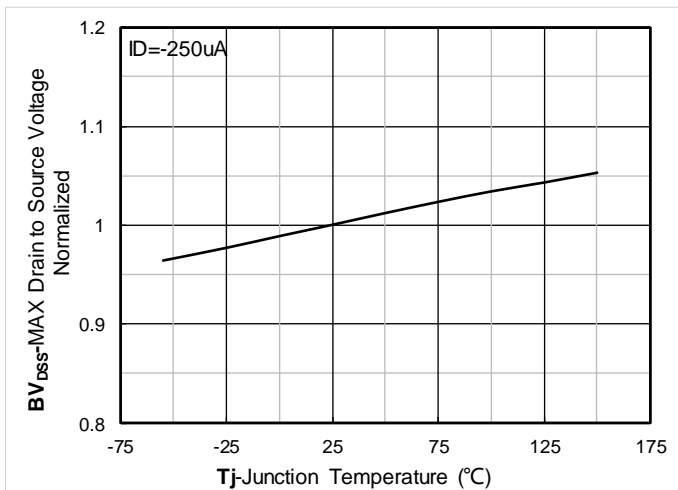


Figure 11. Normalized breakdown voltage

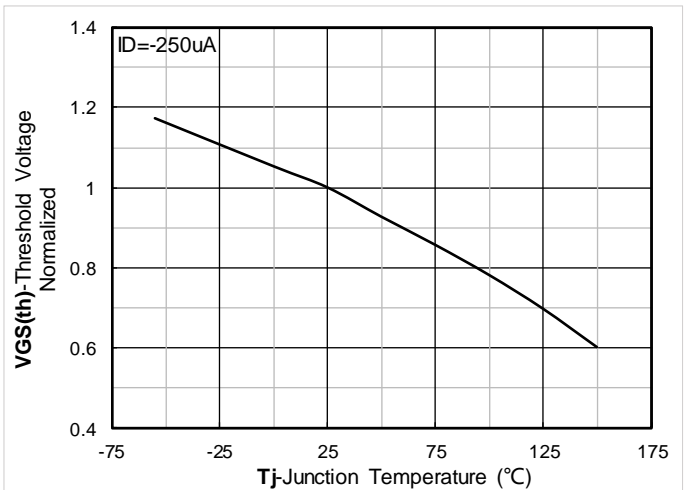


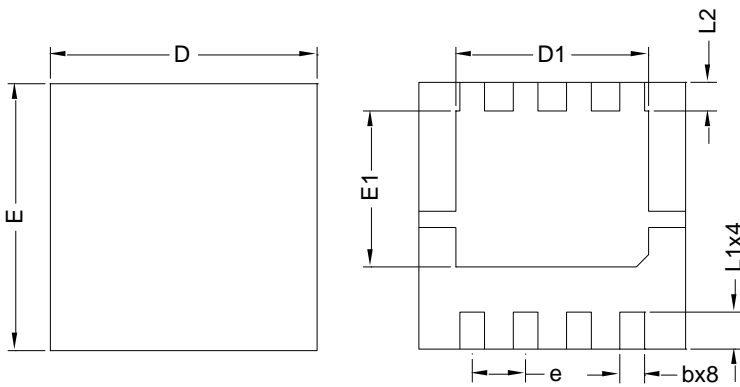
Figure 12. Normalized Threshold voltage

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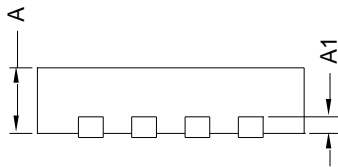
DFN3333-8L-A Package information



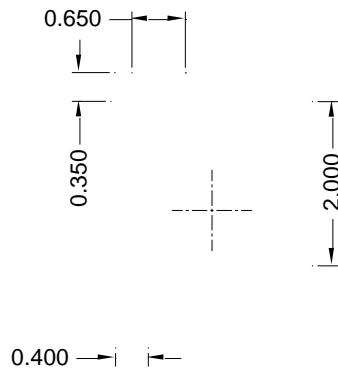
Top View

Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1		0.20 BSC	



Side View



Suggested Solder Pad Layout
Top View

- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.10 mm.
 3. The pad layout is for reference purposes only.



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