



P-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	-30 V
I_D	-40 A
$R_{DS(ON)}$ (at $V_{GS}=-10V$)	12 m
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	16 m
100% EAS Tested	

General Description

Trench Power LV MOSFET technology
Low $R_{DS(on)}$ & FOM
Extremely low switching loss
Excellent stability and uniformity

Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	-12	A
	$T_A=100^\circ\text{C}$		-7.5	
	$T_C=25^\circ\text{C}$		-40	
	$T_C=100^\circ\text{C}$		-25	
Pulsed Drain Current ^A		I_{DM}	-140	A
Avalanche energy ^B		EAS	98	mJ
Total Power Dissipation ^C	$T_A=25^\circ\text{C}$	P_D	2	W
	$T_A=100^\circ\text{C}$		0.8	
	$T_C=25^\circ\text{C}$		50	
	$T_C=100^\circ\text{C}$		20	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	$^\circ\text{C}$

Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	R	50	60	$^\circ\text{C/W}$

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Typical Electrical and Thermal Characteristics Diagrams

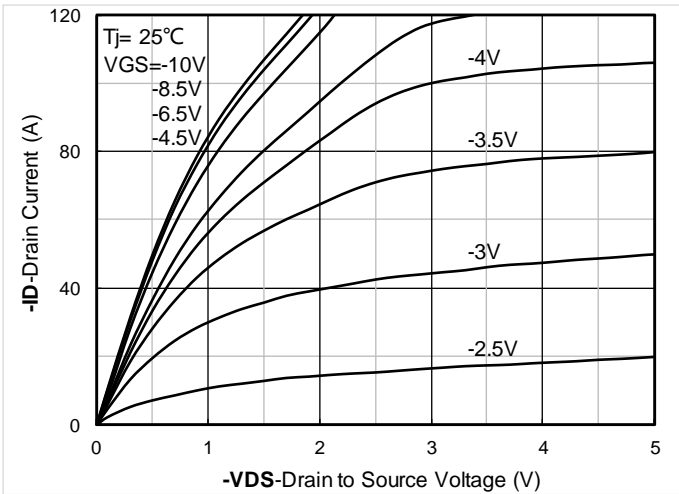


Figure 1. Output Characteristics

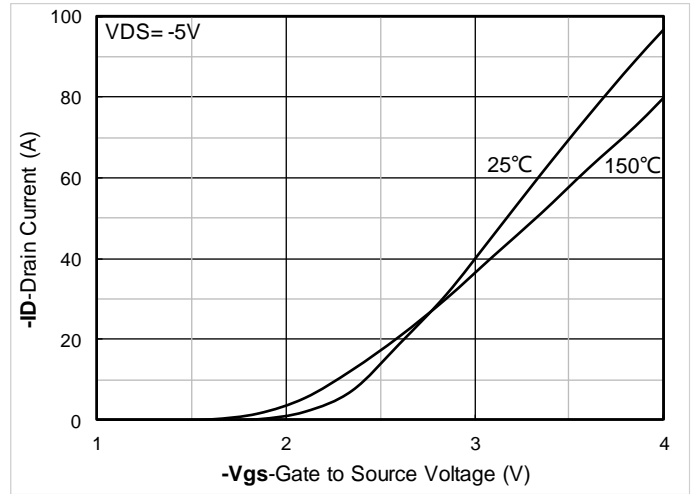


Figure 2. Transfer Characteristics

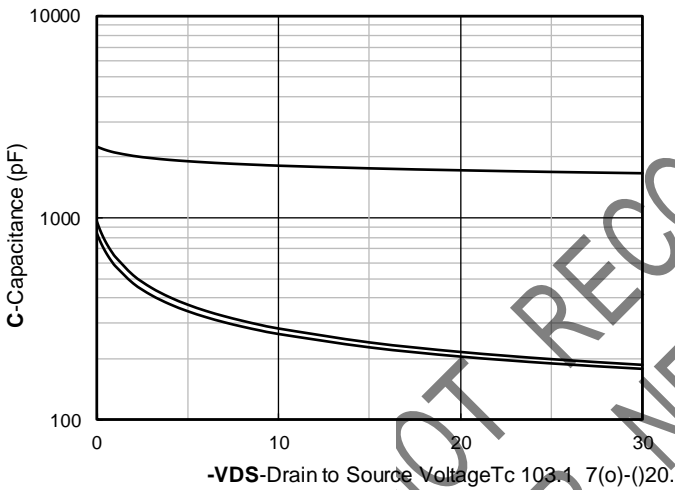


Figure 3. Capacitance Characteristics

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Figure 4. Gate Charge

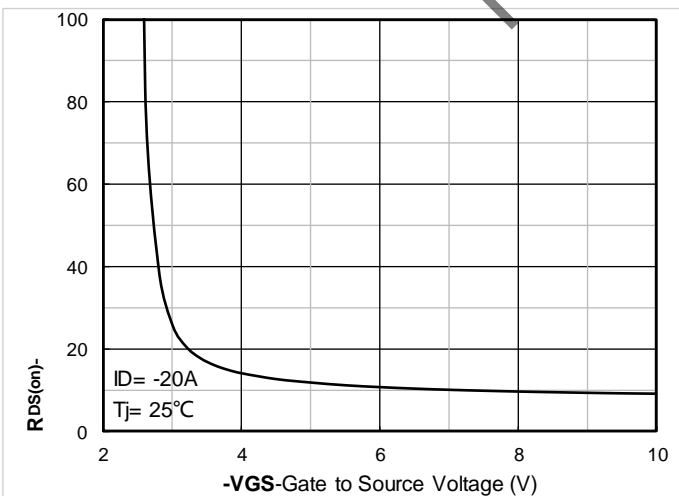


Figure 5. On-Resistance vs Gate to Source Voltage

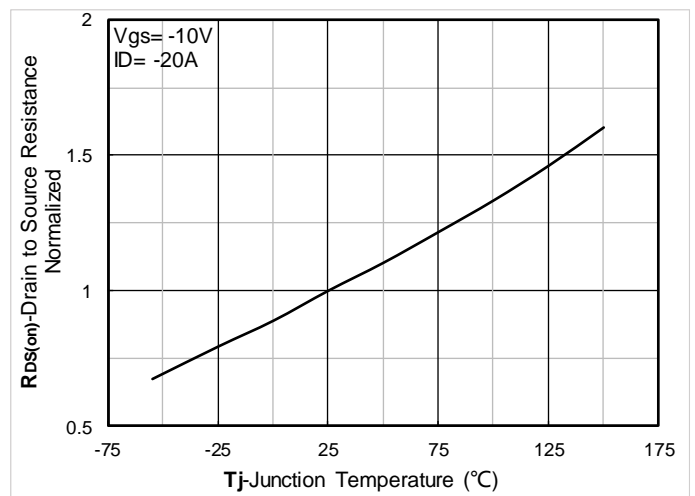


Figure 6. Normalized On-Resistance

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Figure 13. Maximum Transient Thermal Impedance

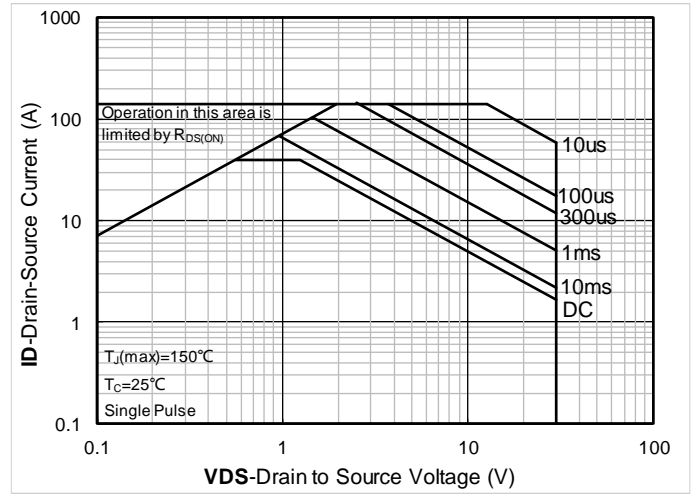


Figure 14. Safe Operation Area

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