



# YJQ45G06A

## N-Channel Enhancement Mode Field Effect Transistor

### Product Summary

$V_{DS}$	60V
$I_D$	45A
$R_{DS(ON)}$ ( at $V_{GS}=10V$ )	9.5m
$R_{DS(ON)}$ ( at $V_{GS}=4.5V$ )	13.5m
100% EAS Tested	

### General Description

Split gate trench MOSFET technology  
 Low  $R_{DS(on)}$  & FOM  
 Extremely low switching loss  
 Excellent stability and uniformity  
 Moisture Sensitivity Level 3  
 Epoxy Meets UL 94 V-0 Flammability Rating  
 Halogen Free

### Applications

Power switching application  
 Uninterruptible power supply  
 DC-DC convertor

### Absolute Maximum Ratings ( $T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	60	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ C$	$I_D$	10	A
	$T_A=100^\circ C$		6	
	$T_C=25^\circ C$		45	
	$T_C=100^\circ C$		28	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	180	A
Avalanche energy <sup>B</sup>		EAS	78	mJ
Total Power Dissipation <sup>B</sup>	$T_A=25^\circ C$	$P_D$	2	W
	$T_A=100^\circ C$		0.8	
	$T_C=25^\circ C$		50	
	$T_C=100^\circ C$		20	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 +150	$^\circ C$

### Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>C</sup>	Steady-State	$R_{JA}$	50	60	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{JC}$	2	2.5	

### Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE



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## Electrical Characteristics ( $T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$	-	-	1	$\mu A$
		$V_{DS}=60V, V_{GS}=0V, T_J=150^\circ C$	-	-	100	
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA

Gate Threshold Voltage



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## Typical Electrical and Thermal Characteristics Diagrams

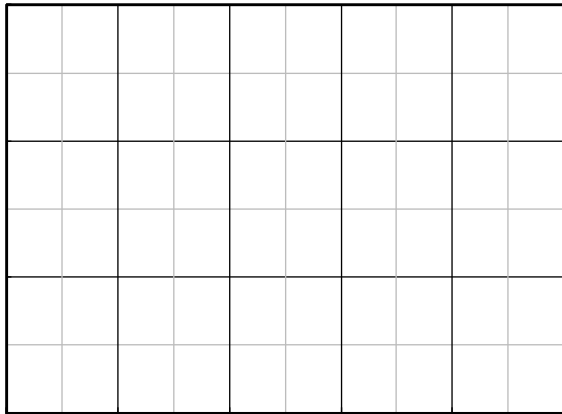


Figure 1. Output Characteristics

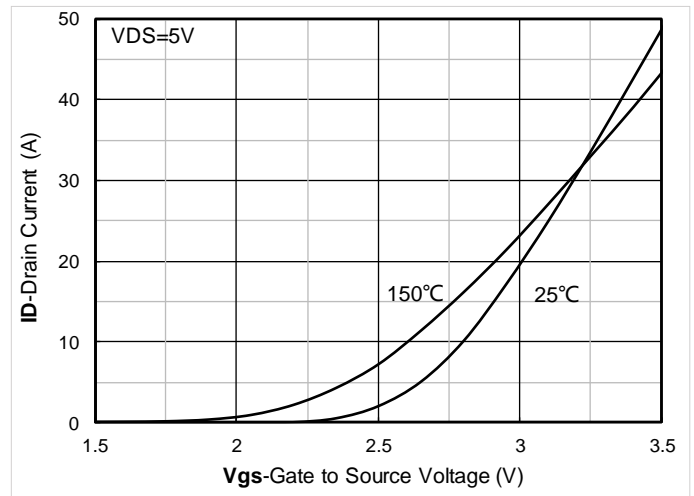


Figure 2. Transfer Characteristics

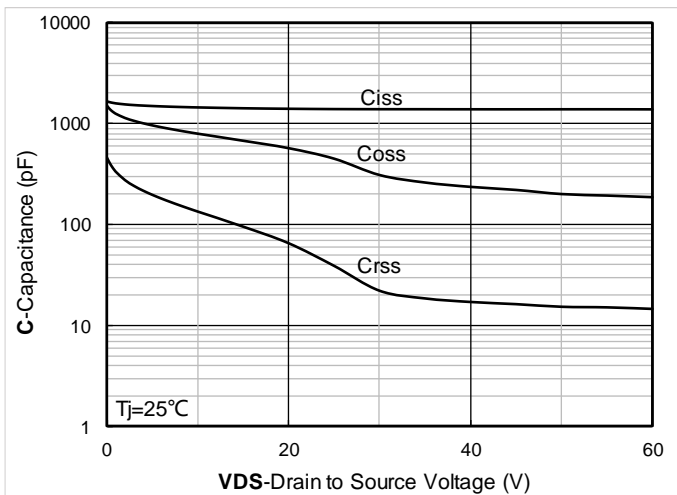


Figure 3. Capacitance Characteristics

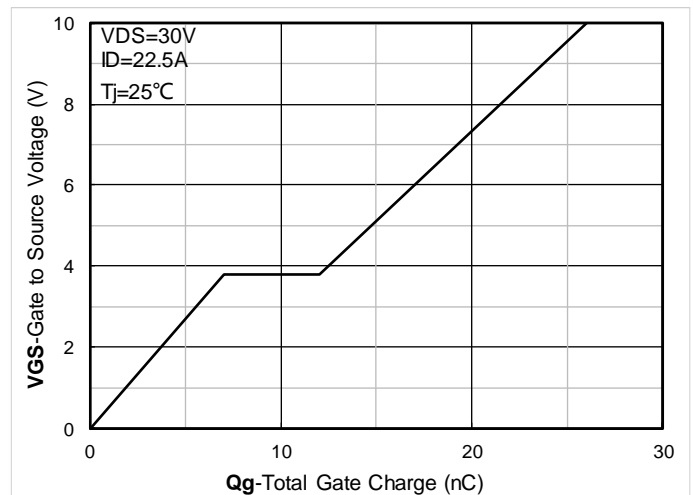


Figure 4. Gate Charge

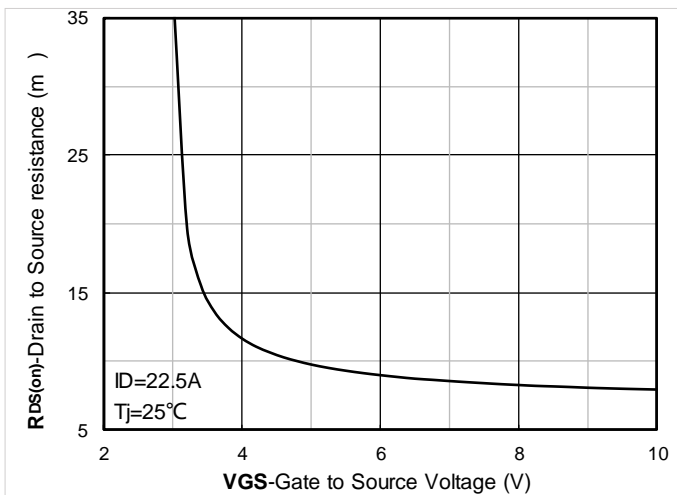


Figure 5. On-Resistance vs Gate to Source Voltage

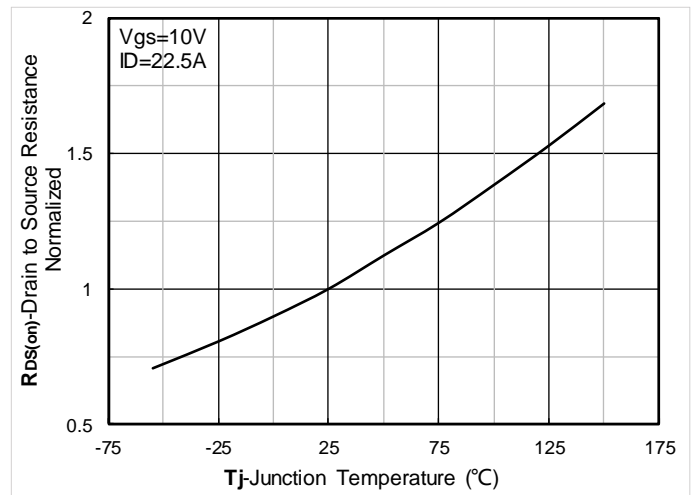


Figure 6. Normalized On-Resistance



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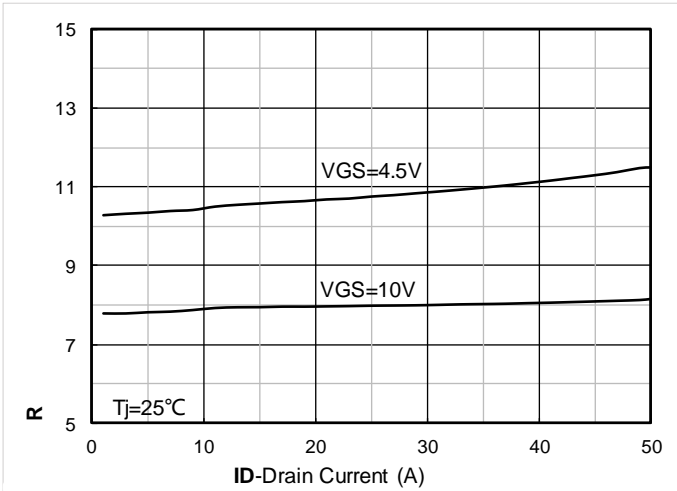


Figure 7.  $R_{DS(on)}$  VS Drain Current

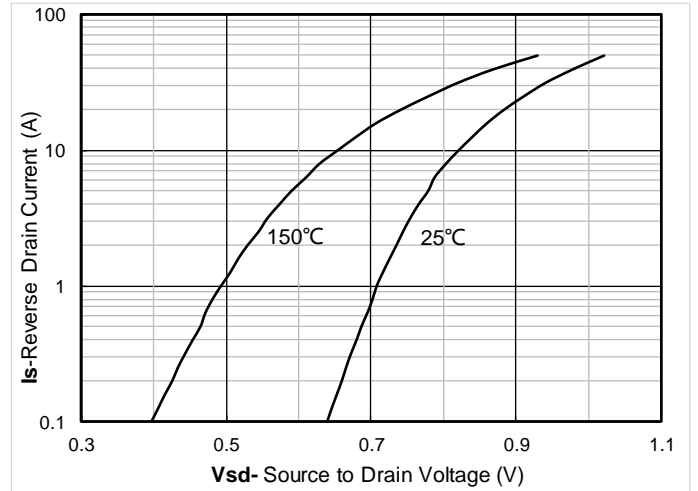


Figure 8. Forward characteristics of reverse diode

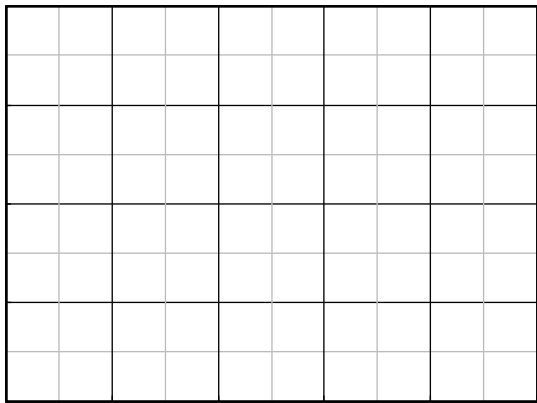


Figure 9. Normalized breakdown voltage

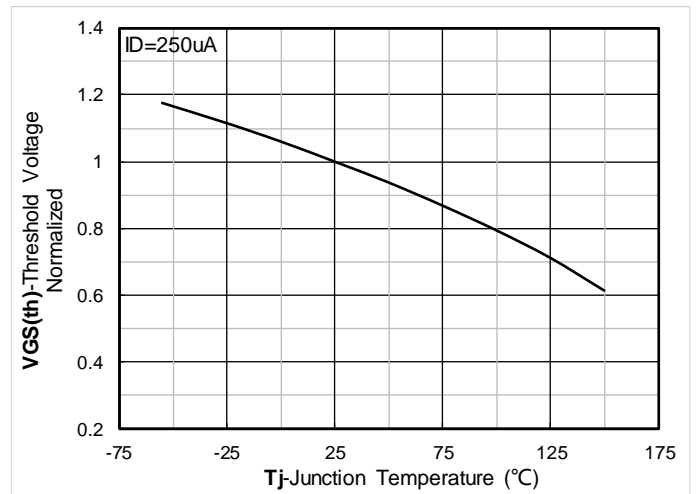


Figure 10. Normalized Threshold voltage

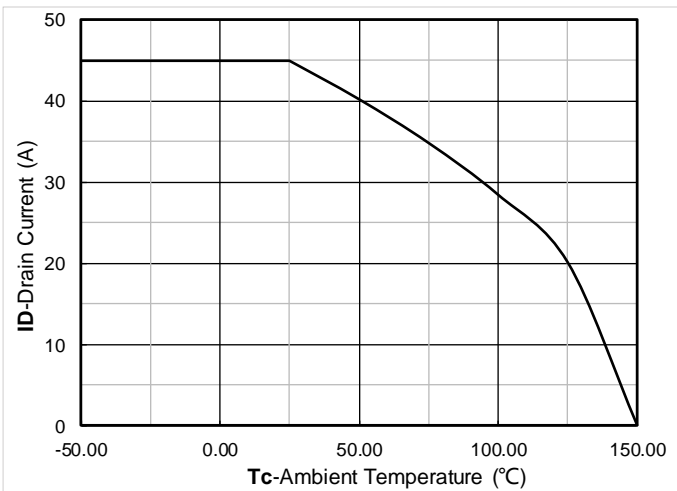


Figure 11. Current dissipation

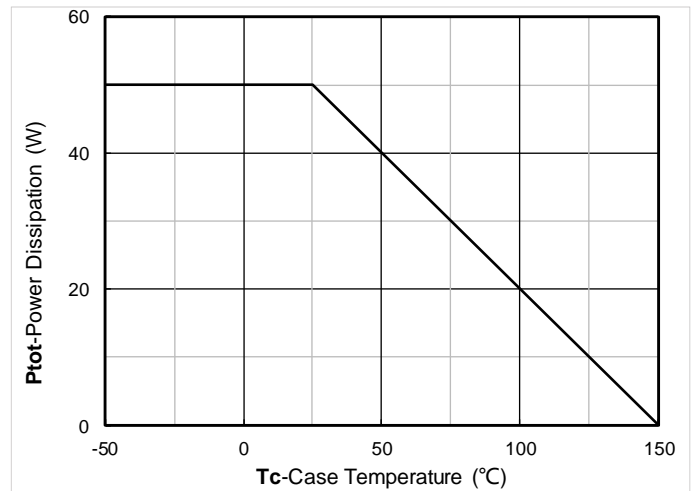


Figure 12. Power dissipation



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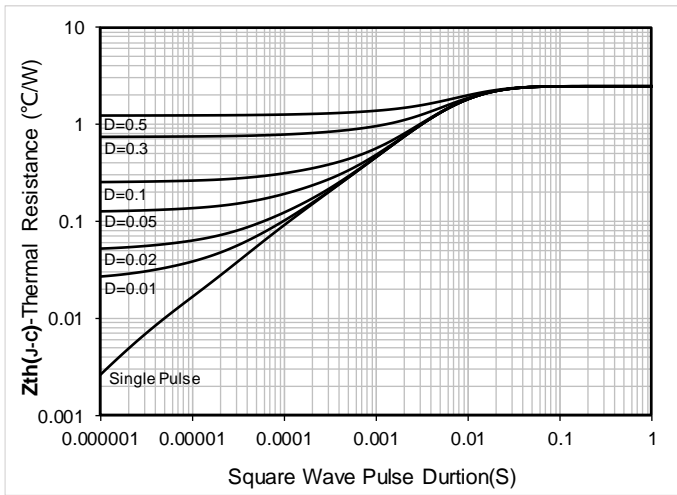


Figure 13. Maximum Transient Thermal Impedance

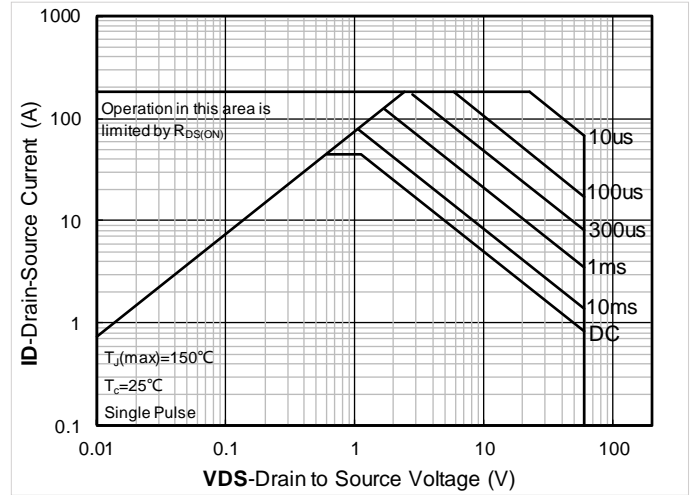


Figure 14. Safe Operation Area

## Test Circuits & Waveforms

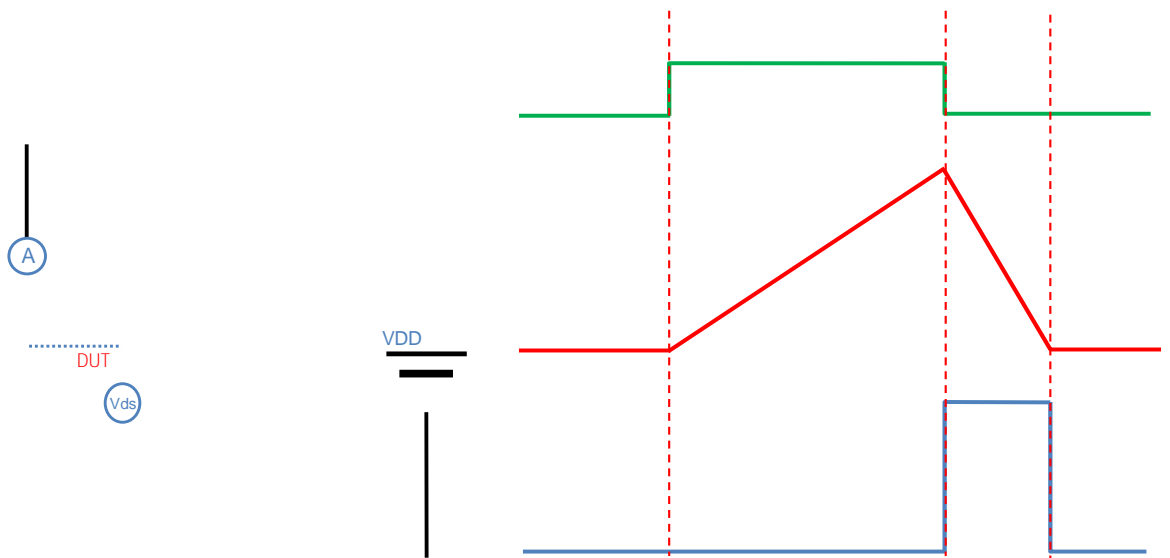


Figure A

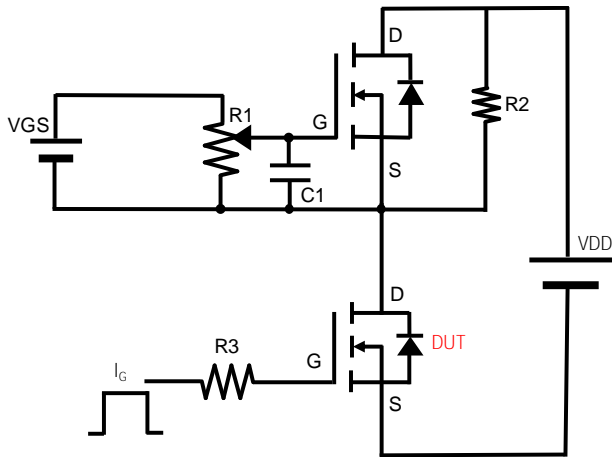


Figure B. Gate Charge Test Circuit & Waveform

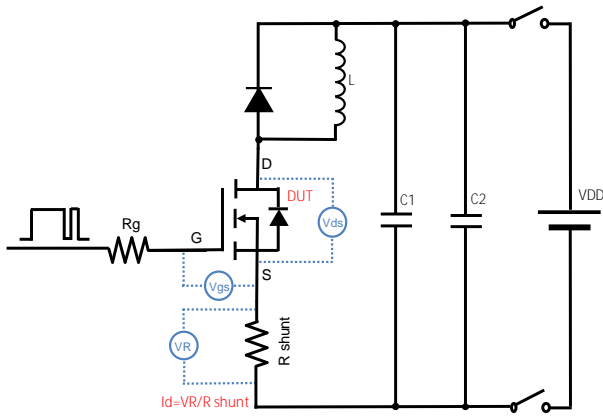


Figure C. Resistive Switching Test Circuit & Waveform

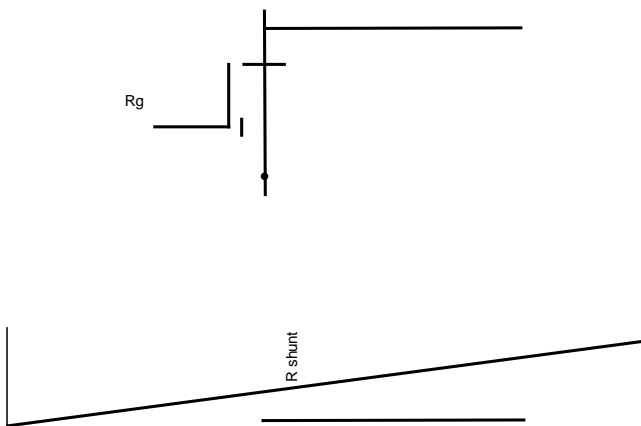
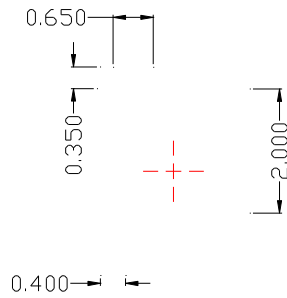
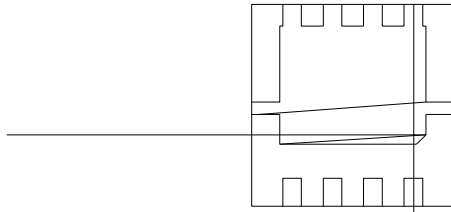


Figure D. Diode Recovery Test Circuit & Waveform



DFN3333-8L Package information



Suggested Solder Pad Layout  
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



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