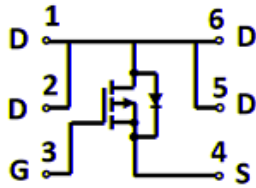


V_{DS}	-20V
I_D	-7A
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	36.5mohm
$R_{DS(ON)}$ (at $V_{GS}=-2.5V$)	46.5mohm
$R_{DS(ON)}$ (at $V_{GS}=-1.8V$)	60.5mohm

Trench Power LV MOSFET technology
High density cell design for Low $R_{DS(ON)}$
High Speed switching

Battery protection
Power management
Load switch

N2x2-6L



DF

($T_A=25$ unless otherwise noted)

Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	± 10	V
Drain Current	$T_C=25$ @ Steady State	I_D	-7	A
	$T_C=70$ @ Steady State		-5.6	
Pulsed Drain Current ^A		I_{DM}	-28	A
Total Power Dissipation @ $T_C=25$ ^C		P_D	2.2	W
Thermal Resistance Junction-to-Ambient @ Steady State ^D		R_{JA}	57	/ W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 +150	

(Example)

YJQ4666B	F1	..G66B	3000	30000	120000	7 " reel
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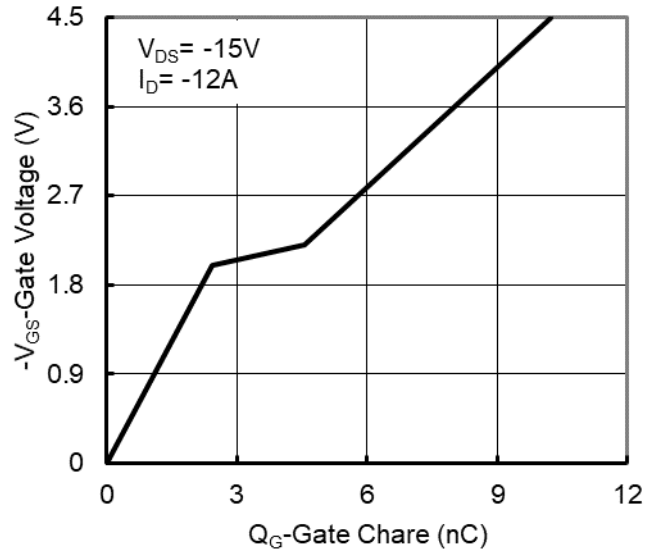
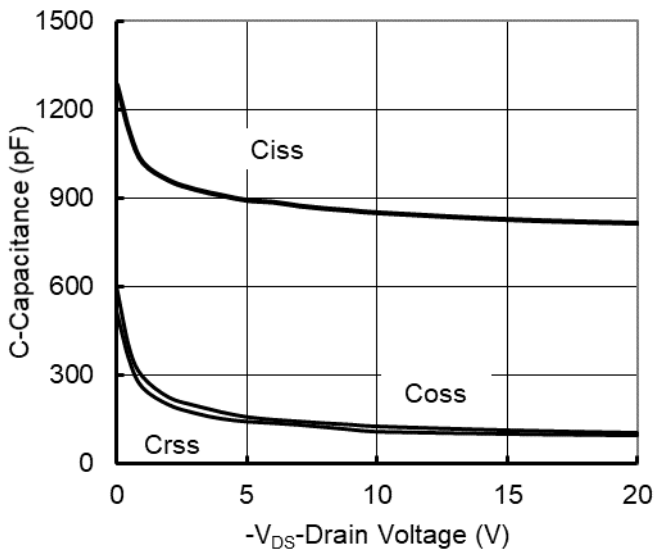
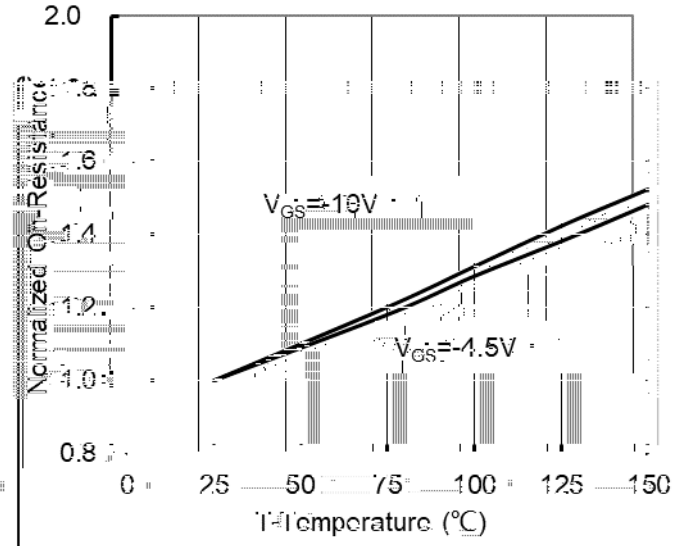
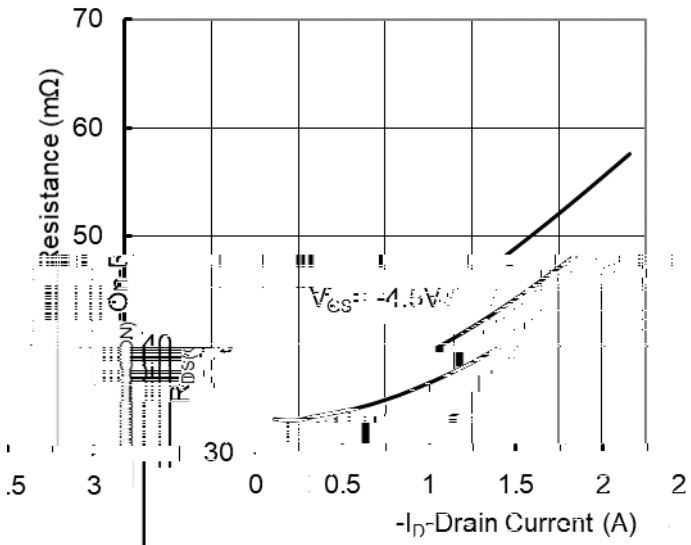
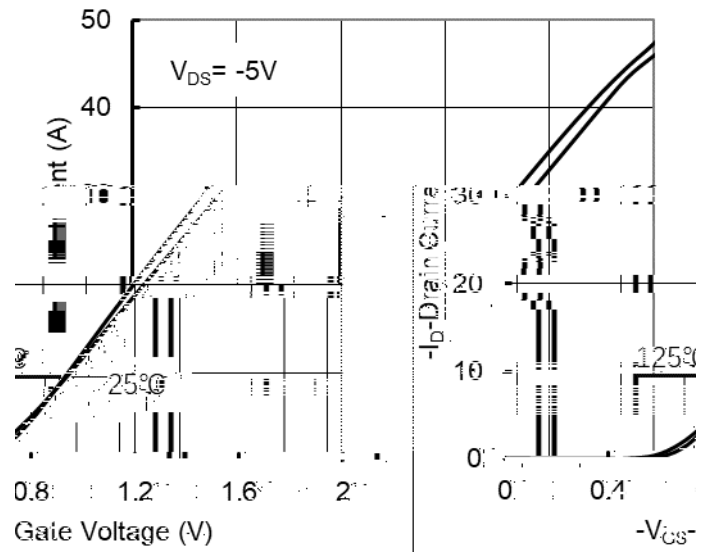
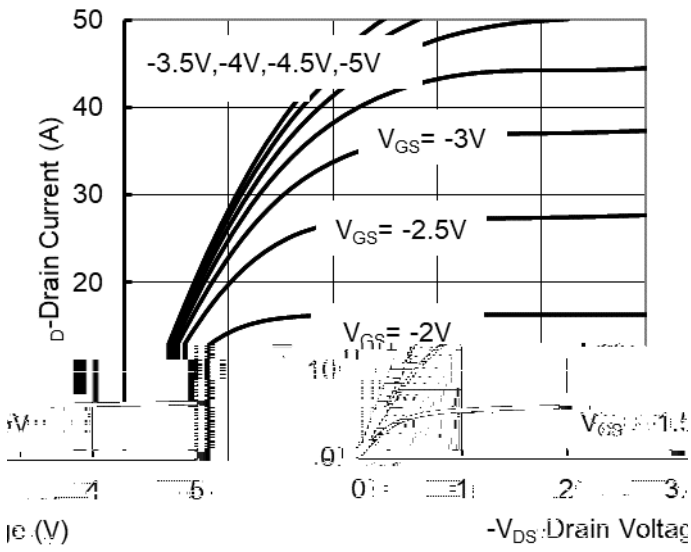


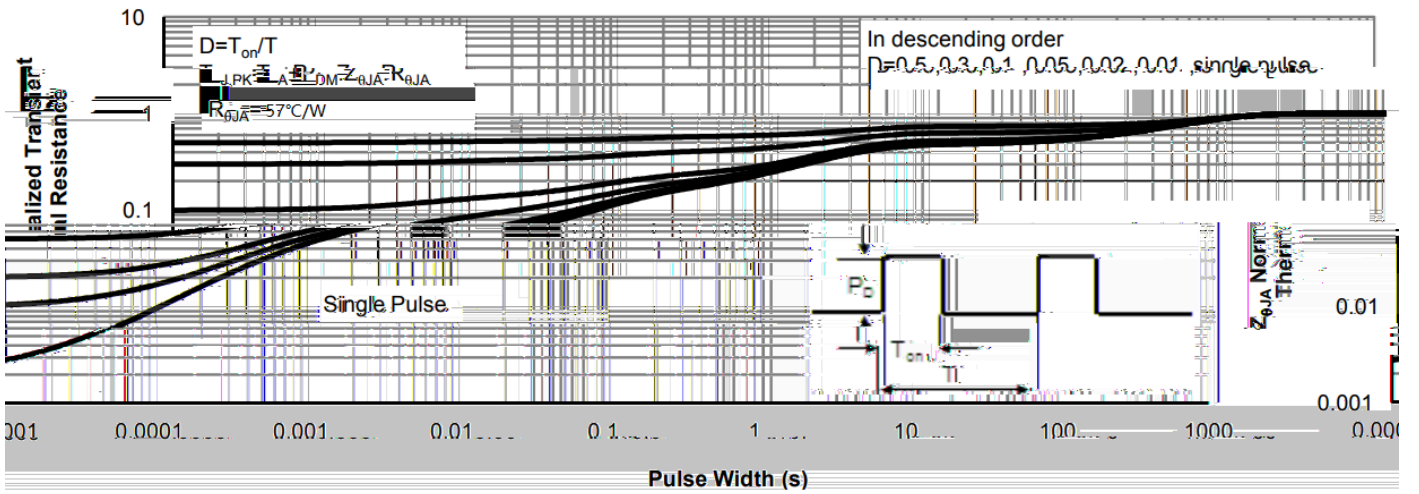
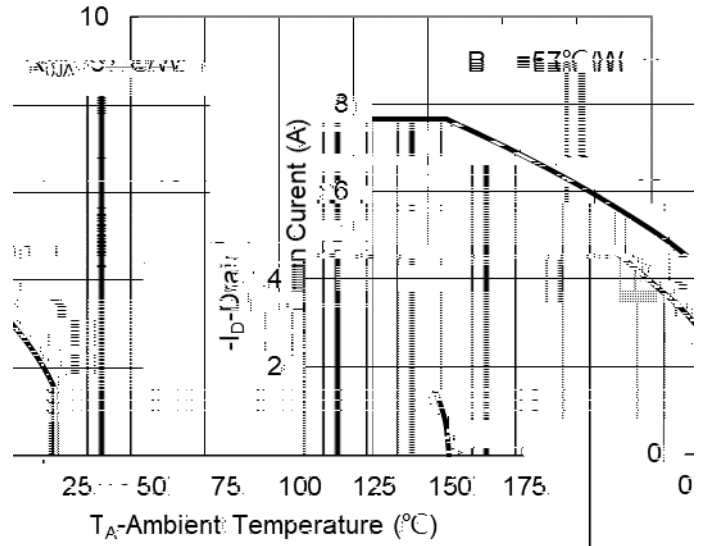
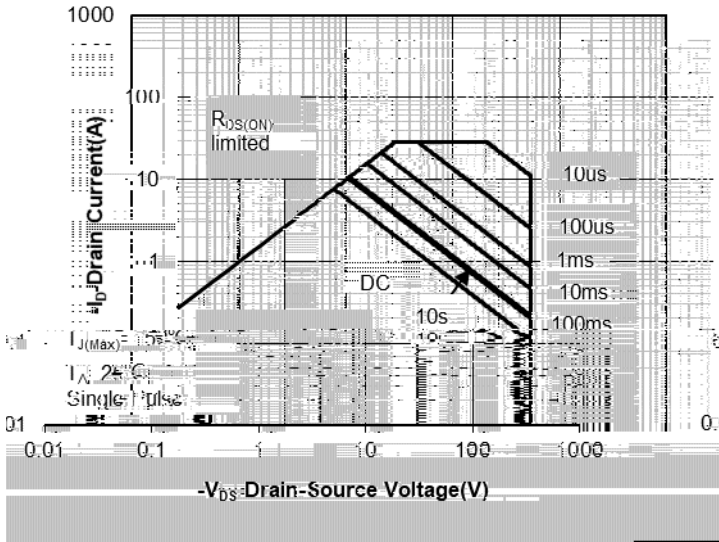
(T_J=25 unless otherwise noted)

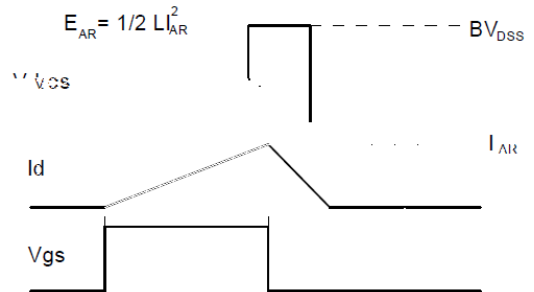
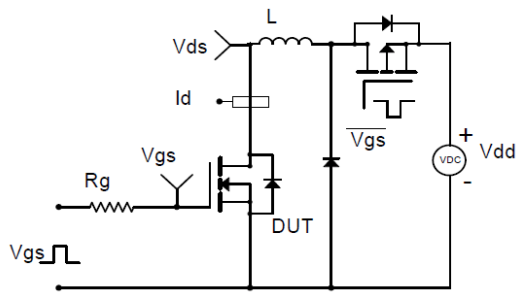
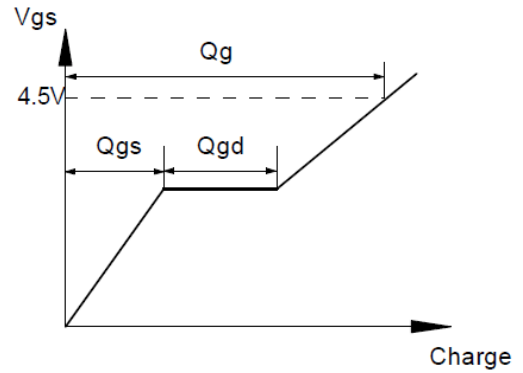
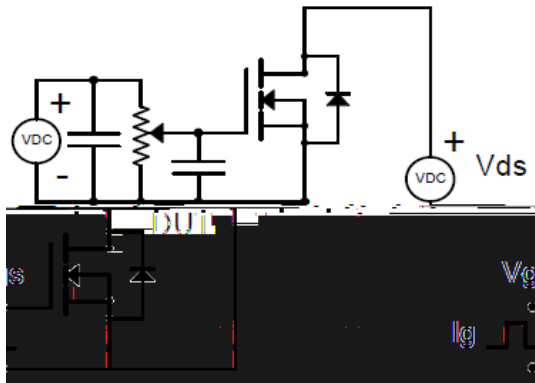
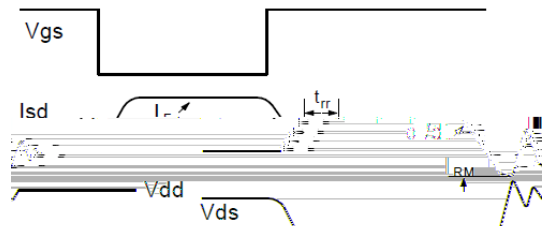
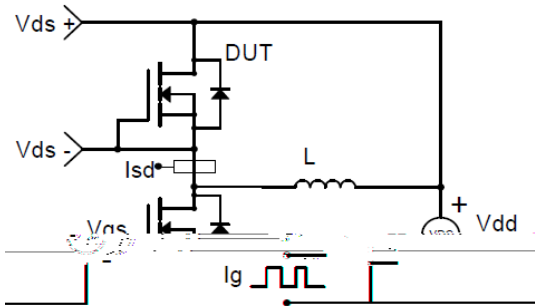
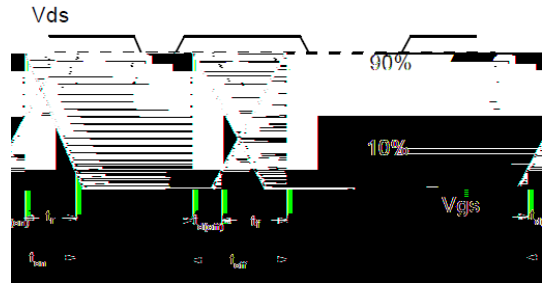
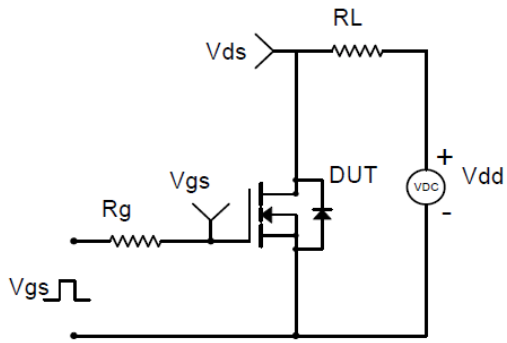
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ± 10V, V _{DS} =0V			± 100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -4.5V, I _D =-7A		24.5	36.5	m
		V _{GS} = -2.5V, I _D =-5A		33.5	46.5	
		V _{GS} = -1.8V, I _D =-2A		45.5	60.5	
Diode Forward Voltage	V _{SD}	I _S =-7A, V _{GS} =0V		-0.7	-1.2	V
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1MHZ		852		pF
Output Capacitance	C _{oss}			127		
Reverse Transfer Capacitance	C _{rss}			109		
Total Gate Charge	Q _g	V _{GS} =-4.5V, V _{DS} =-9V, I _D =-7A		40.1		nC
Gate Source Charge	Q _{gs}			8.4		
Gate Drain Charge	Q _{gd}			8.6		
Reverse Recovery Charge	Q _{rr}	I _F = -15A, di/dt=100A/us		7.8		ns
Reverse Recovery Time	t _{rr}			18		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-4.5V, V _{DD} =-9V, I _D =-1A, R _{GEN} =2.5		8		ns
Turn-on Rise Time	t _r			19		
Turn-off Delay Time	t _{D(off)}			75		
Turn-off Fall Time	t _f			46		

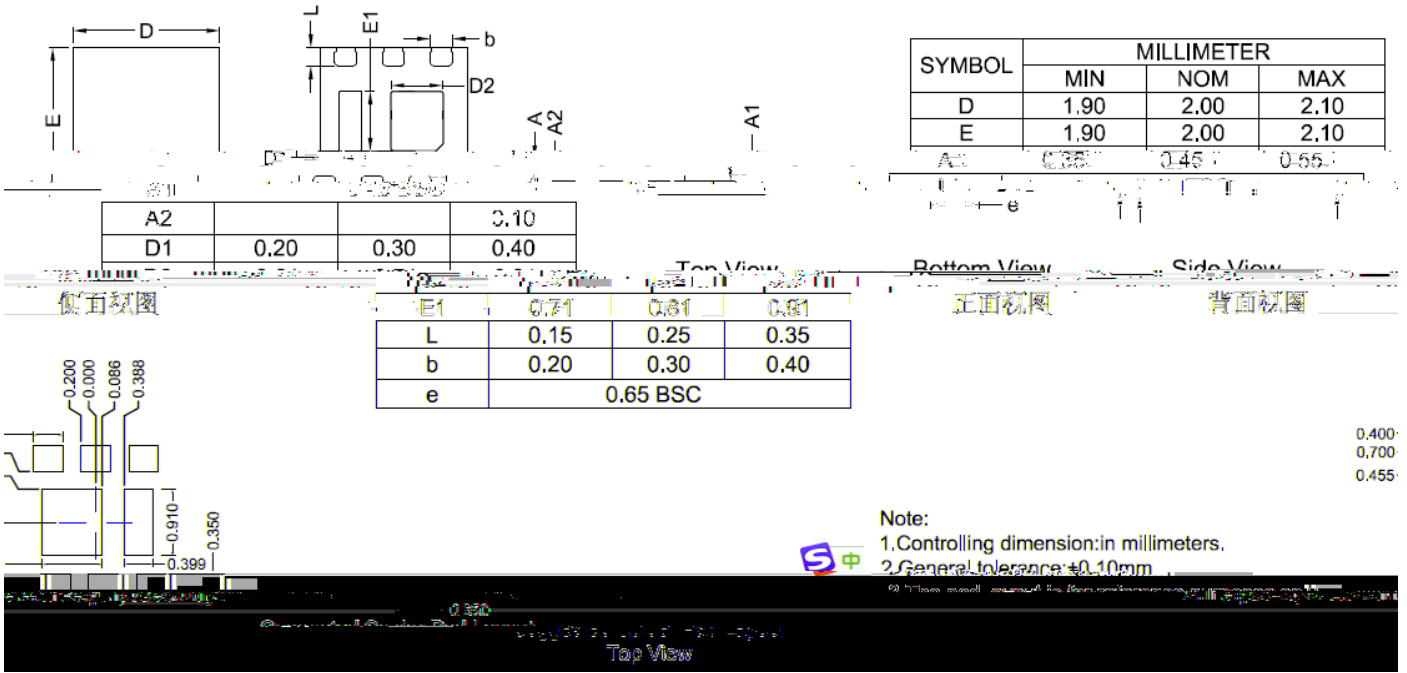
A. Pulse Test: Pulse Width 300us, Duty cycle 2%.

B. R_{JA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{JC} is guaranteed by design, while R_{JA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.











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