



YJQ4D8G04H

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	40V
I_D	75A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	4.8m
100% EAS Tested	
100% V_{DS} Tested	

General Description

Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$



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Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D	40	-	-	V
		V _{GS} = 0V, I _D =1mA	40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	
		V _{DS} =40V, V _{GS} =0V, T _J =125°C	-	-	100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D	2	2.8	4	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	3.8	4.8	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V	-	-	1.2	V
Gate resistance	R _G	f=1MHz	-	1.6	-	
Maximum Body-Diode Continuous Current	I _S		-	-	75	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, f=1MHz	-	880	-	pF
Output Capacitance	C _{oss}		-	495	-	
Reverse Transfer Capacitance	C _{rss}		-	42	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =20V, I _D =20A	-	15.7	-	nC
Gate-Source Charge	Q _{gs}		-	4.6	-	
Gate-Drain Charge	Q _{gd}		-	4.9	-	
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=100A/us	-	11.3	-	nC
Reverse Recovery Time	t _{rr}		-	20.6	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =20V, I _D =20A R _{GEN} =3	-	11.6	-	ns
Turn-on Rise Time	t _r		-	58	-	
Turn-off Delay Time	t _{D(off)}		-	16.2	-	
Turn-off fall Time	t _f		-	6	-	

- Note
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
 - The value of R_θ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with T_A =25 .The maximum allowed junction temperature of 175 . The value in any given application depends on the user's specific board design.
 - Thermal resistance from junction to soldering point (on the exposed drain pad).



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Typical Electrical and Thermal Characteristics Diagrams

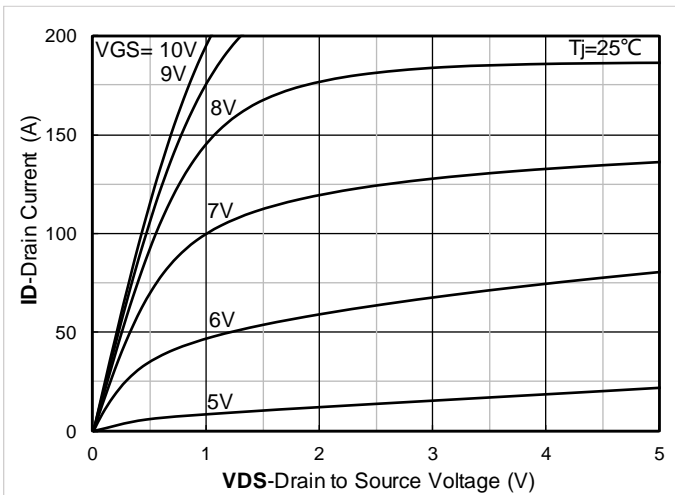


Figure 1. Output Characteristics

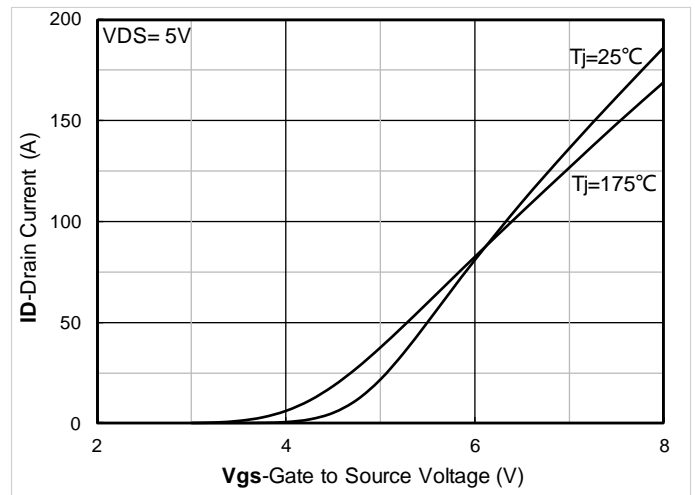


Figure 2. Transfer Characteristics

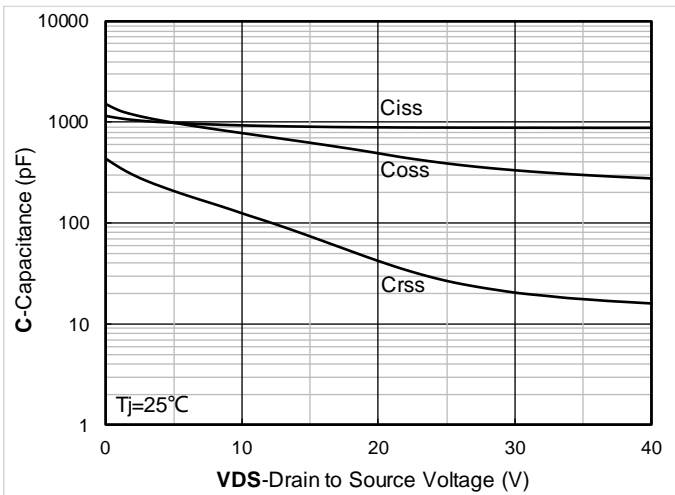


Figure 3. Capacitance Characteristics

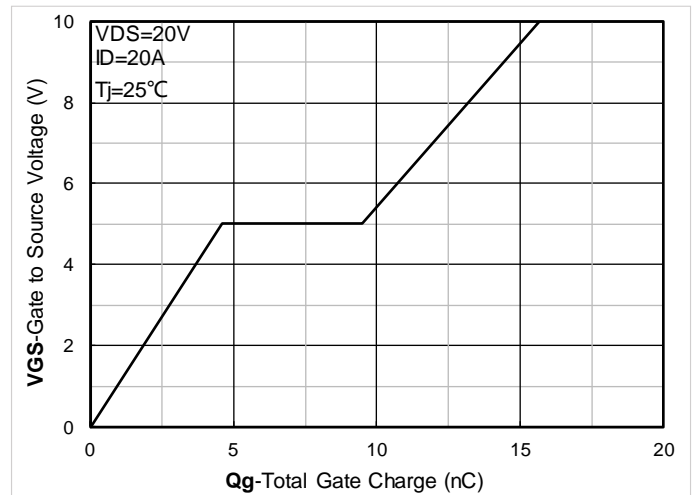


Figure 4. Gate Charge

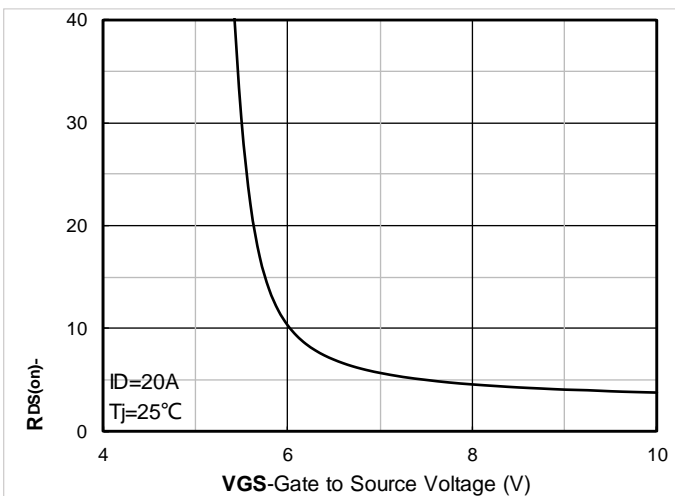


Figure 5. On-Resistance vs Gate to Source Voltage

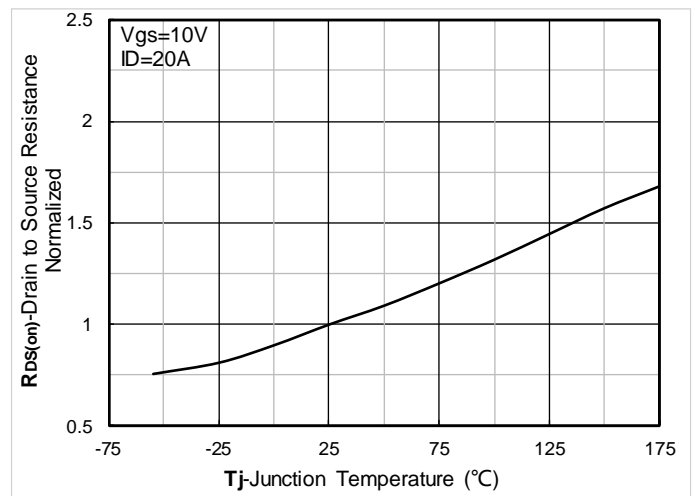


Figure 6. Normalized On-Resistance



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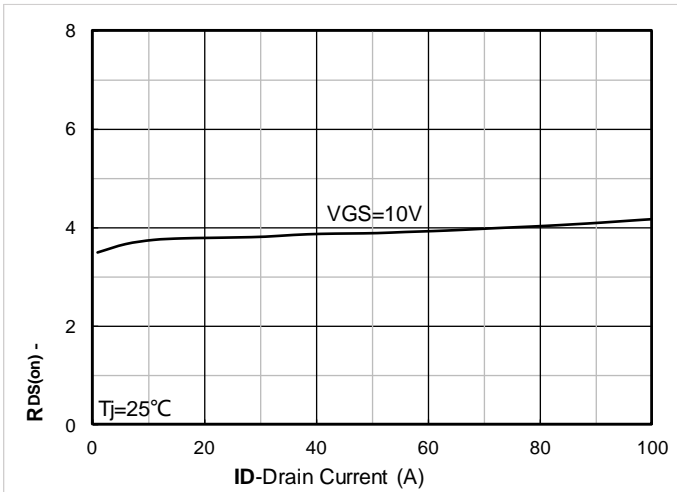


Figure 7. RDS(on) VS Drain Current

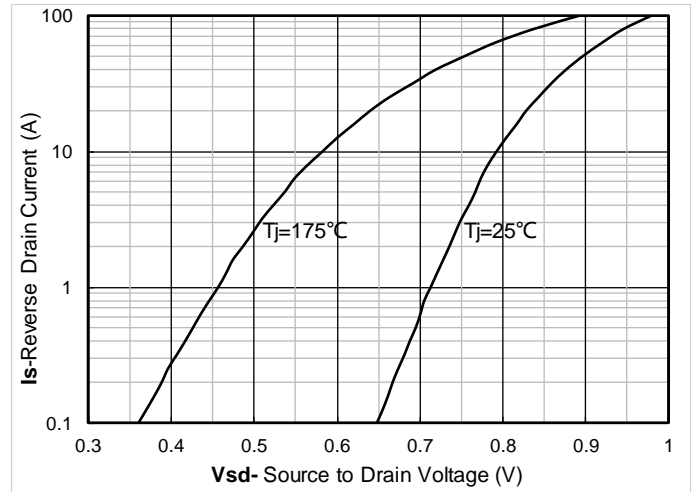


Figure 8. Forward characteristics of reverse diode

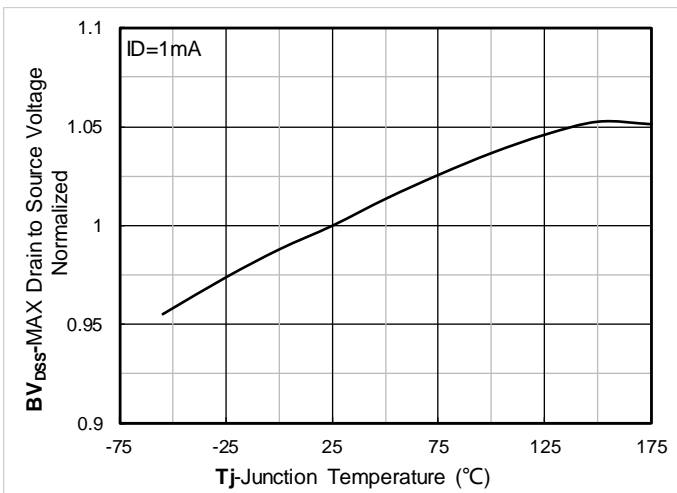


Figure 9. Normalized breakdown voltage

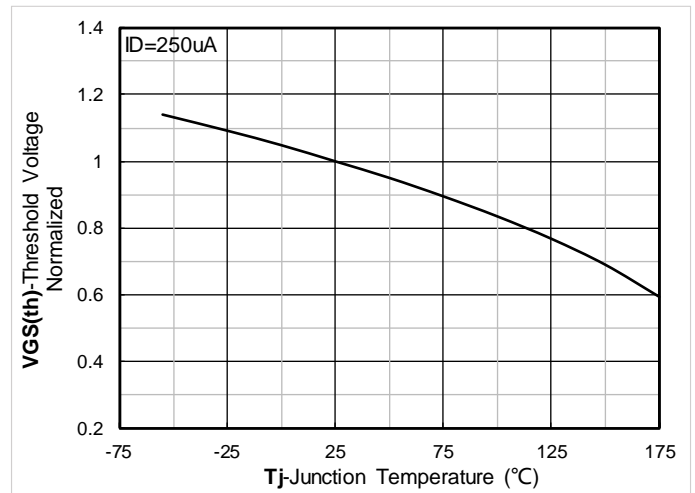


Figure 10. Normalized Threshold voltage

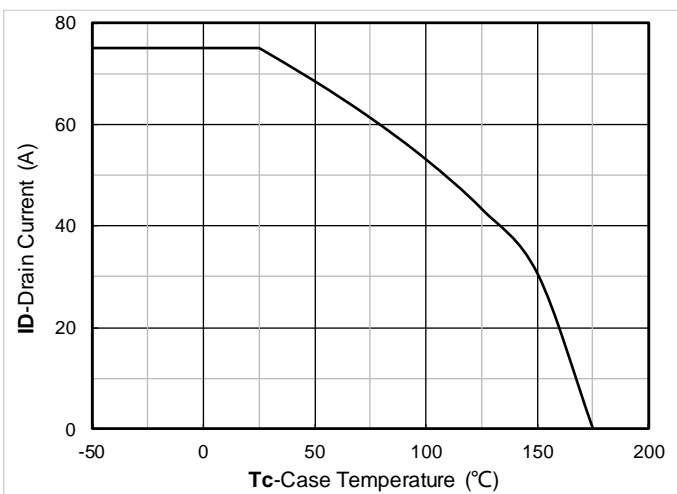


Figure 11. Current dissipation

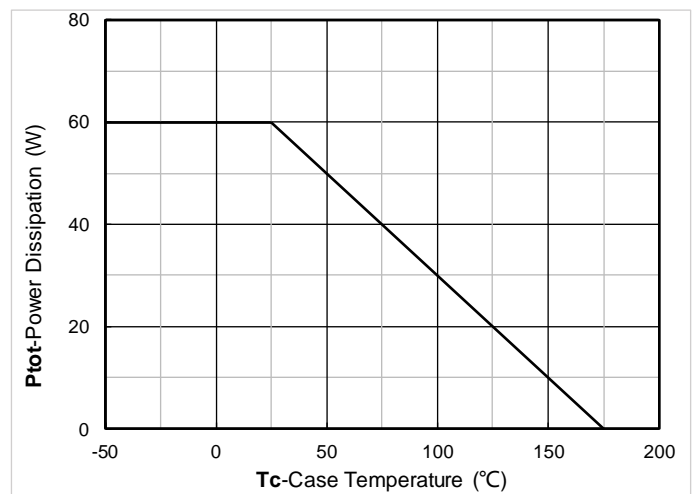


Figure 12. Power dissipation



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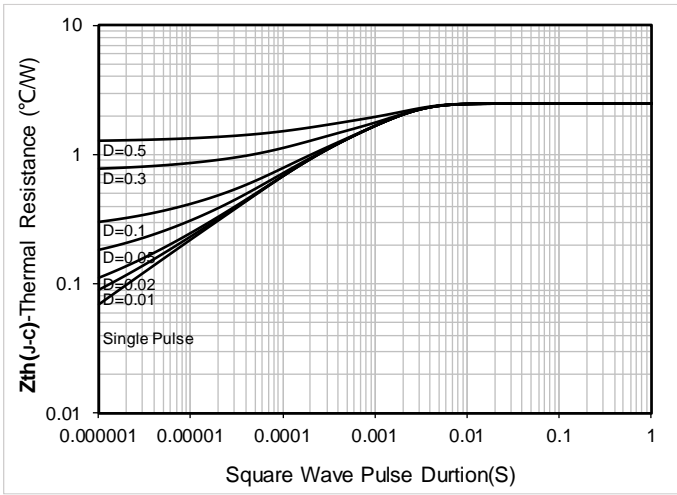


Figure 13. Maximum Transient Thermal Impedance

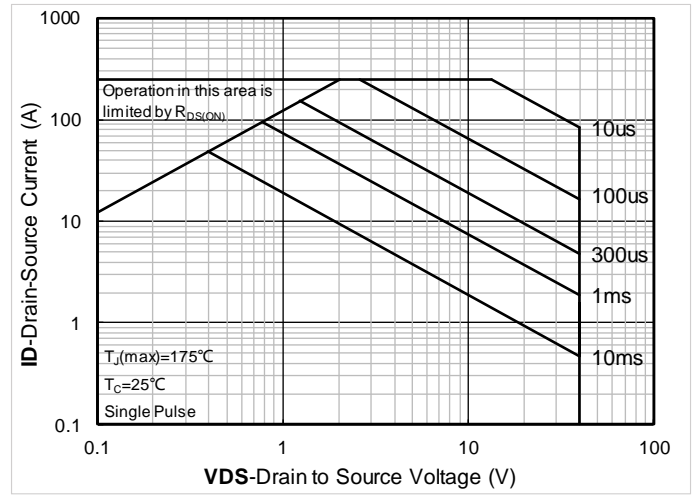


Figure 14. Safe Operation Area

Test Circuits & Waveforms

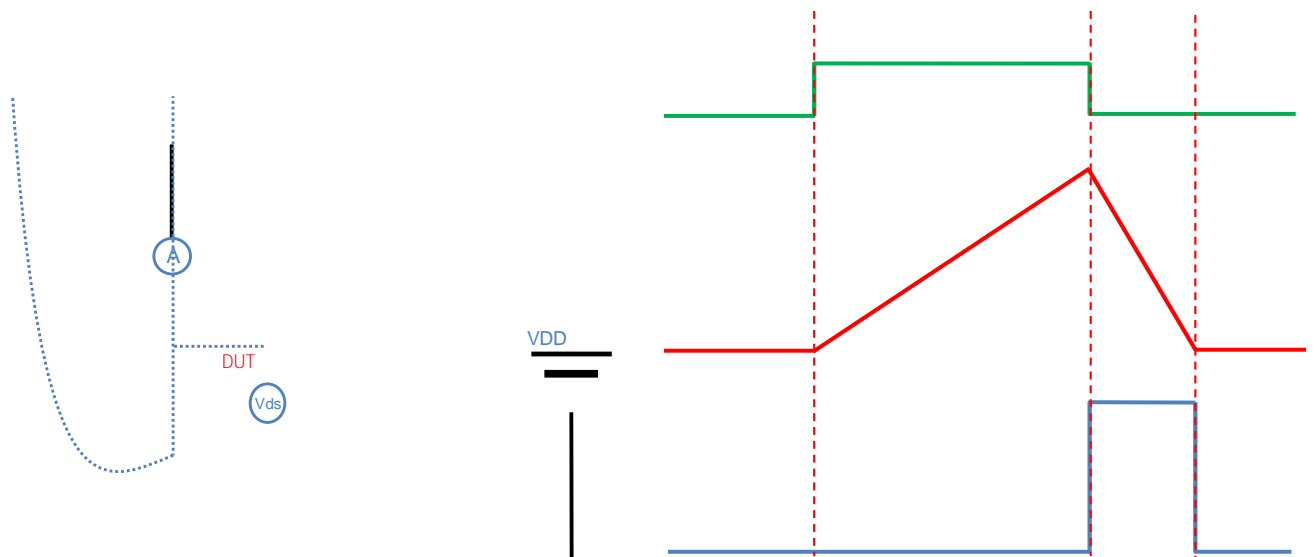


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

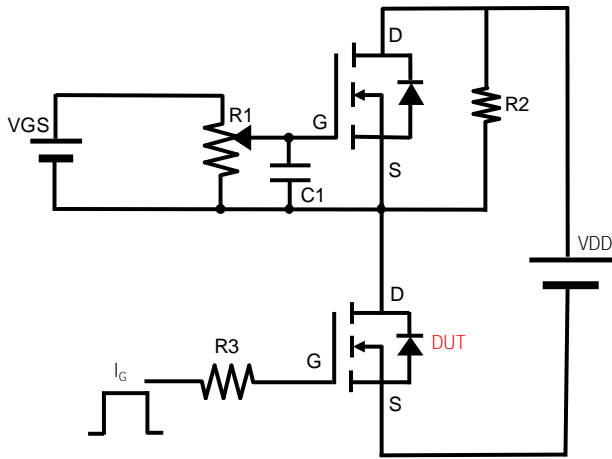


Figure B. Gate Charge Test Circuit & Waveform

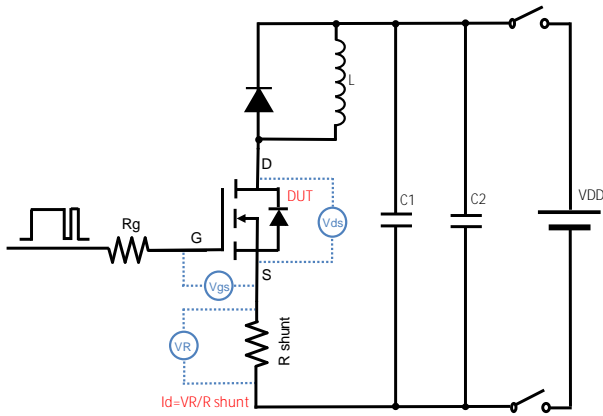


Figure C. Resistive Switching Test Circuit & Waveform

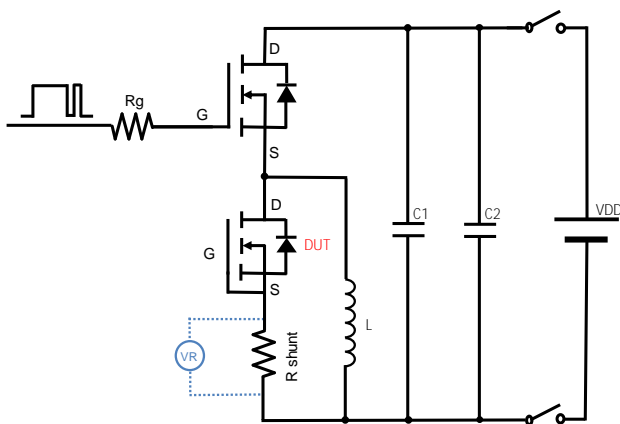
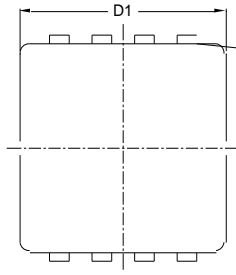


Figure D. Diode Recovery Test Circuit & Waveform

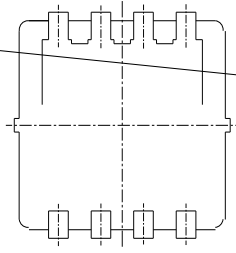


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PDFN3333-8L-B-0.75MM Package information



TOP VIEW



BOTTOM VIEW

SIDE VIEW

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

UNIT mm

SUGGESTED SOLDER PAD LAYOUT



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