



YJQ50G04H

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	40V
I_D	50A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	7m
100% EAS Tested	

General Description

Split gate trench MOSFET technology
 Excellent package for heat dissipation
 High density cell design for low $R_{DS(ON)}$
 Moisture Sensitivity Level 1
 Epoxy Meets UL 94 V-0 Flammability Rating
 Halogen Free

Applications

Power switching application
 Uninterruptible power supply
 DC-DC convertor

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	12	A
	$T_A=100^\circ C$		8.5	
	$T_C=25^\circ C$		50	
	$T_C=100^\circ C$		35	
Pulsed Drain Current ^A		I_{DM}	200	A
Avalanche energy ^B		EAS	72	mJ

$T_A=25$

Total Power Dissipation ^C



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Electrical Characteristics ($T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA
		$V_{DS}=40V, V_{GS}=0V, T_J=175^\circ C$	-	-	100	
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$	-	5.3	7	m
Diode Forward Voltage	V_{SD}	$I_S=20A, V_{GS}=0V$	-	-	1.2	V
Gate resistance	R_G	$f=1MHz$	-	2	-	
Maximum Body-Diode Continuous Current	I_S		-	-	50	A
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V, f=1MHz$	-	965	-	pF
Output Capacitance	C_{oss}		-	350	-	
Reverse Transfer Capacitance	C_{rss}		-	11	-	
Switching Parameters						
Total Gate Charge	Q_g		-	12.5	-	
		$V_{GS}=10V, V_{DS}=20V, I_D=25A$				nC



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Typical Electrical and Thermal Characteristics Diagrams

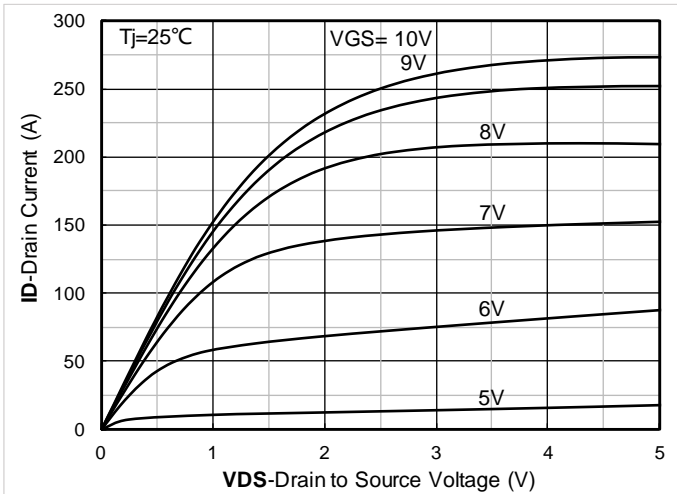


Figure 1. Output Characteristics

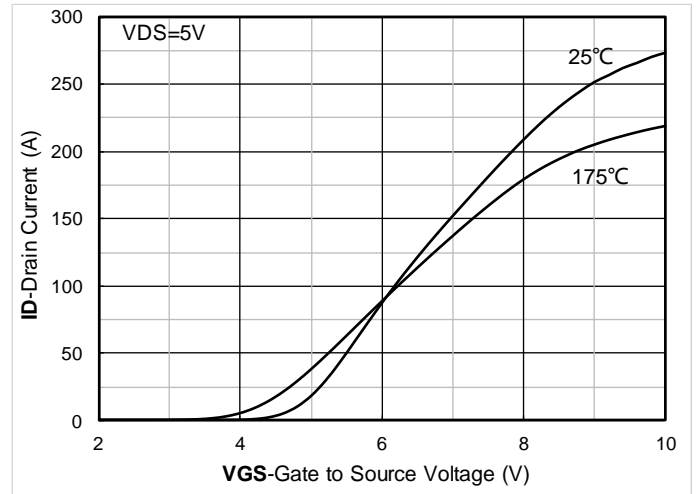


Figure 2. Transfer Characteristics

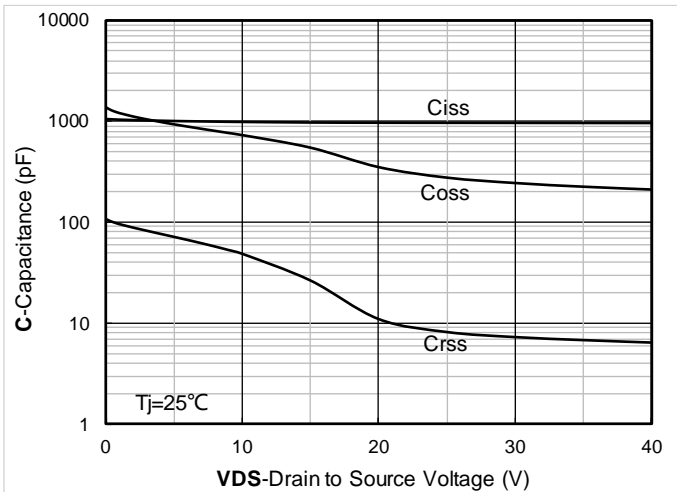


Figure 3. Capacitance Characteristics

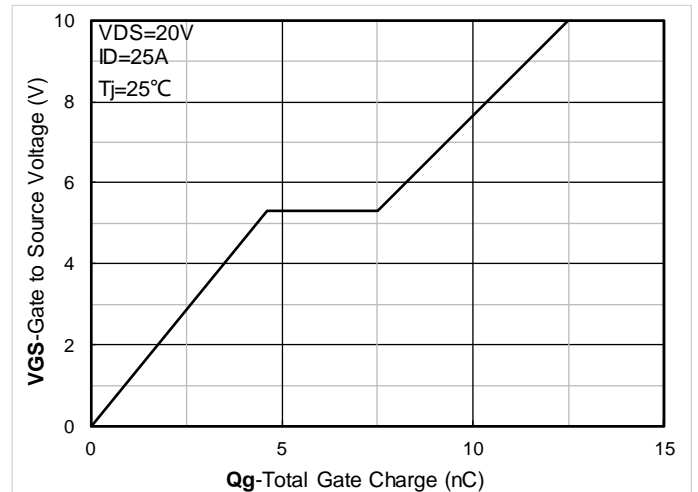


Figure 4. Gate Charge

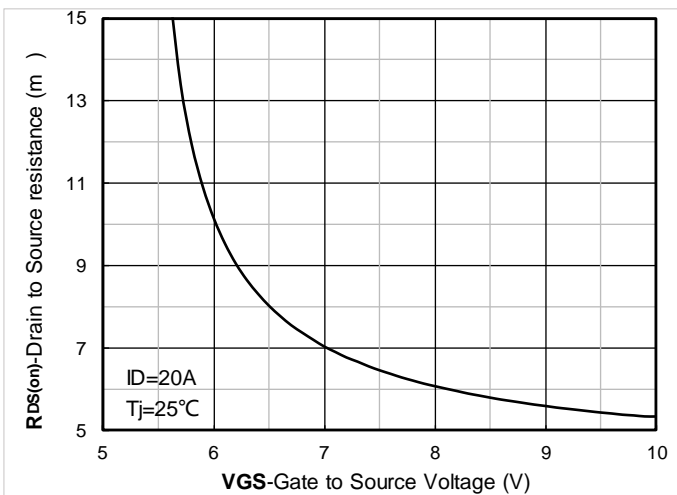


Figure 5. On-Resistance vs Gate to Source Voltage

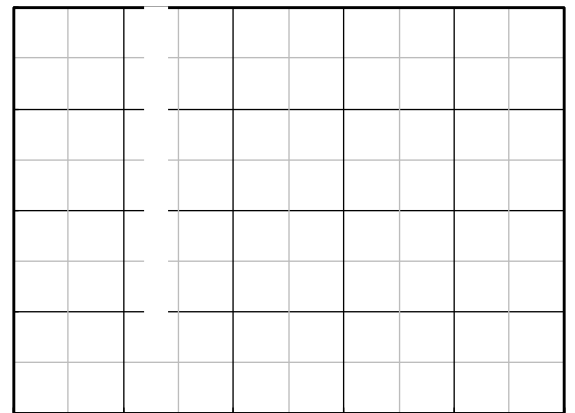


Figure 6. Normalized On-Resistance



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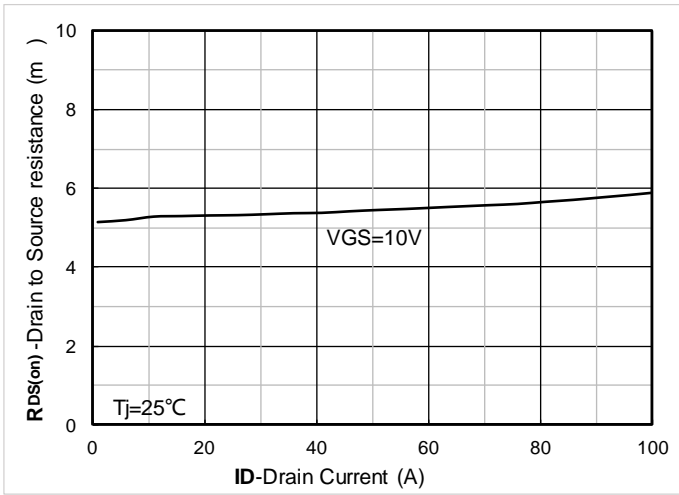


Figure 7. RDS(on) VS Drain Current

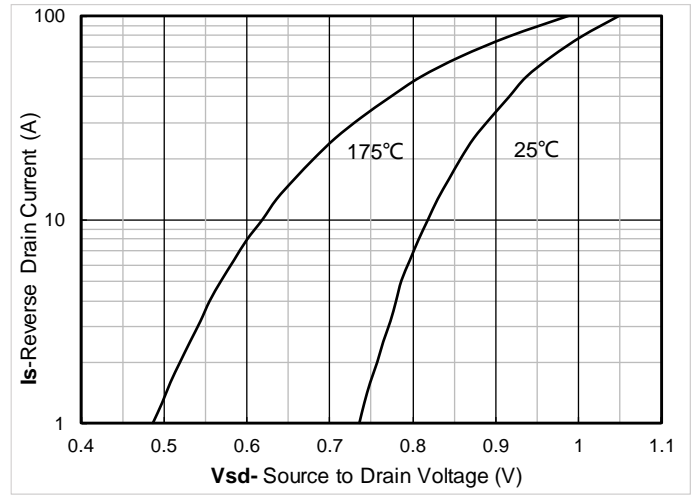


Figure 8. Forward characteristics of reverse diode

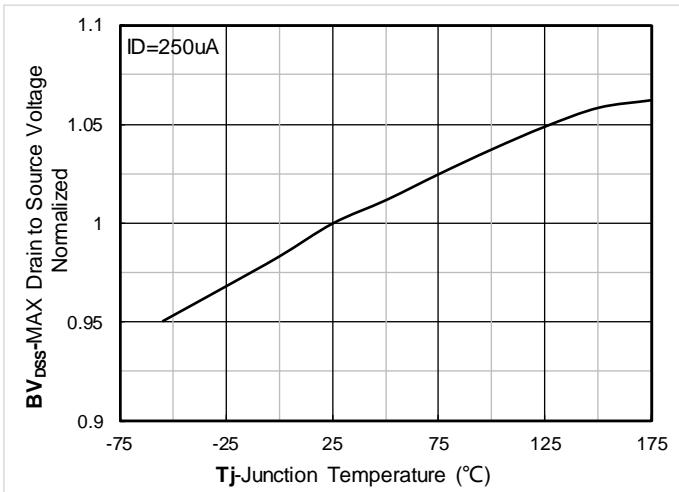


Figure 9. Normalized breakdown voltage

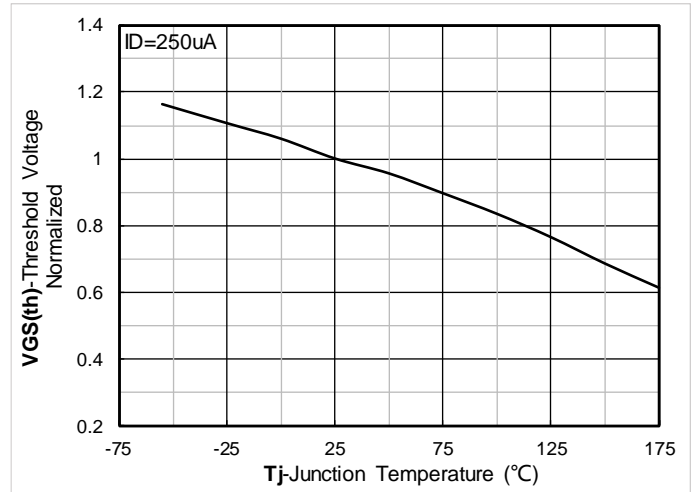


Figure 10. Normalized Threshold voltage

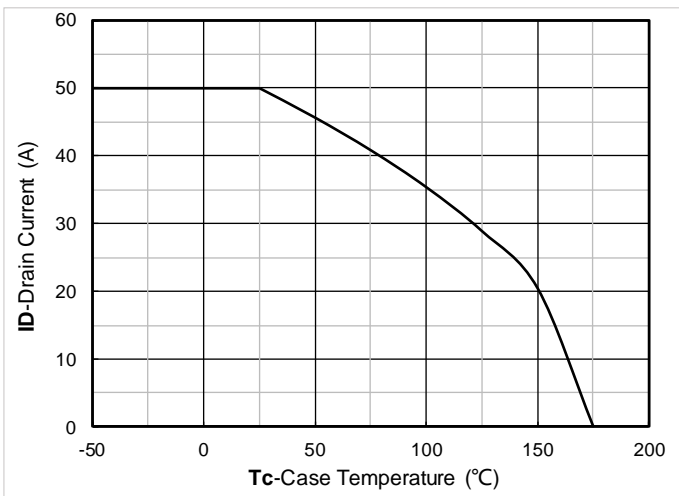


Figure 11. Current dissipation

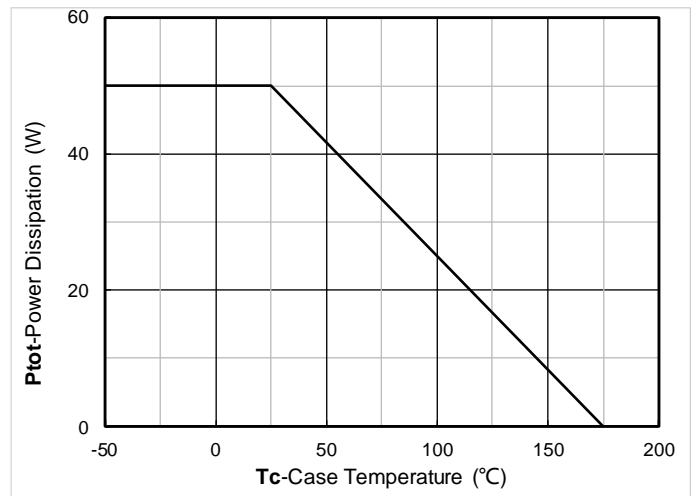


Figure 12. Power dissipation



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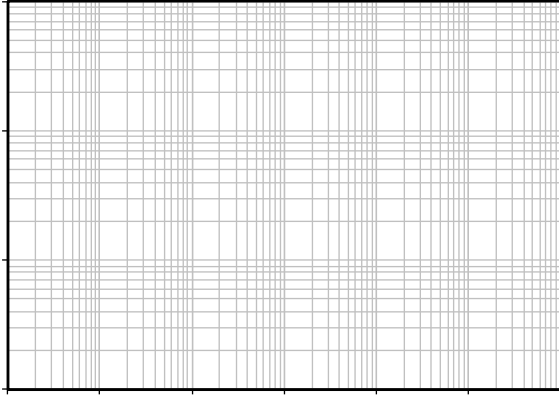


Figure 13. Maximum Transient Thermal Impedance

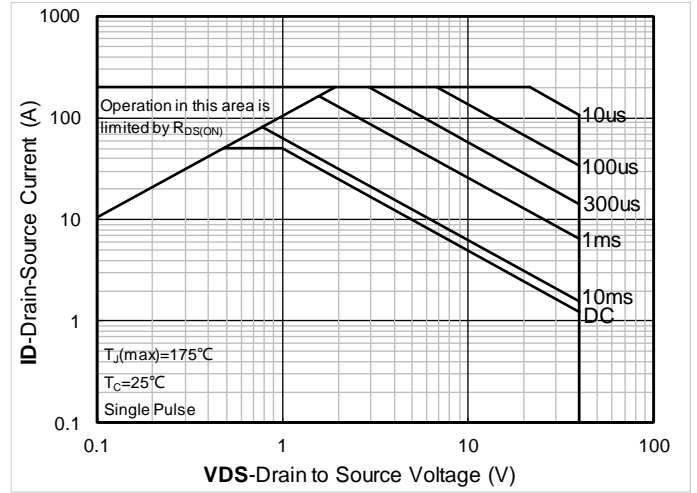


Figure 14. Safe Operation Area

Test Circuits & Waveforms

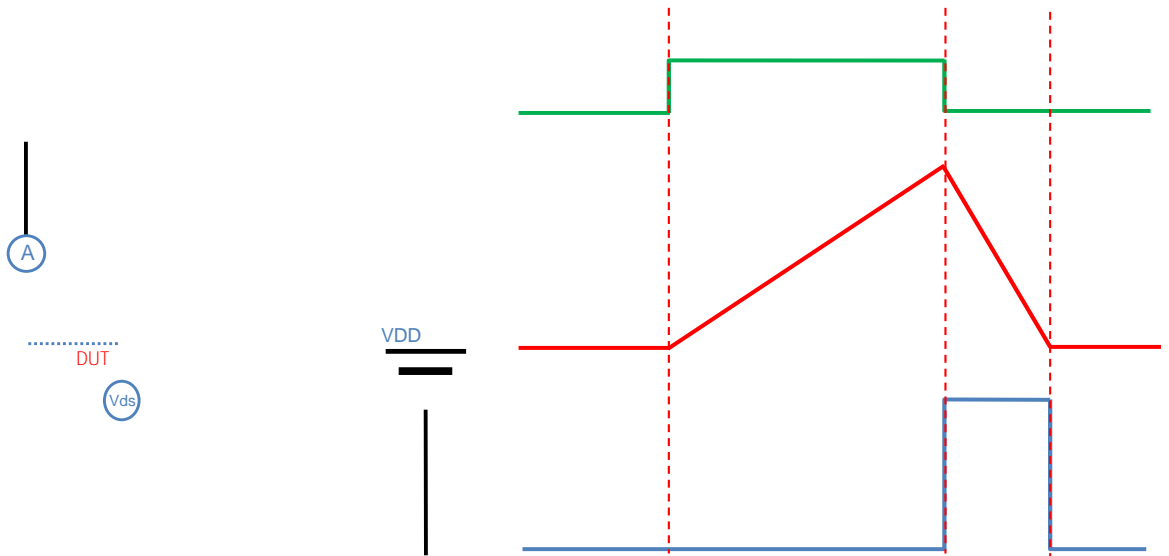


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform



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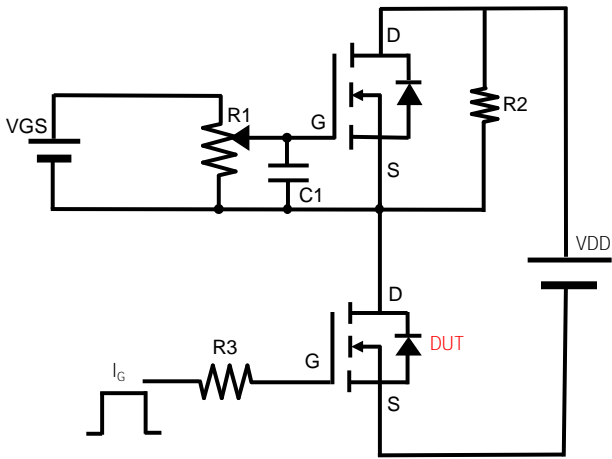


Figure B. Gate Charge Test Circuit & Waveform

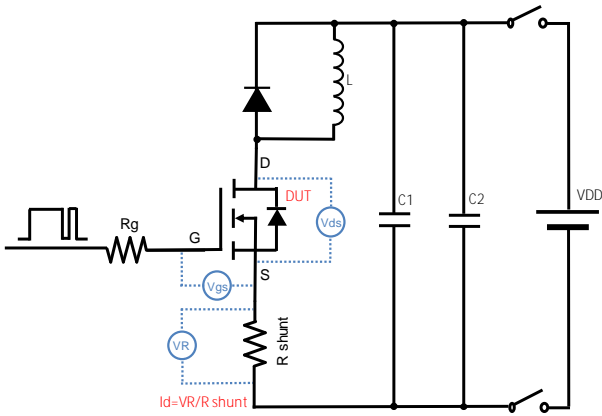


Figure C. Resistive Switching Test Circuit & Waveform

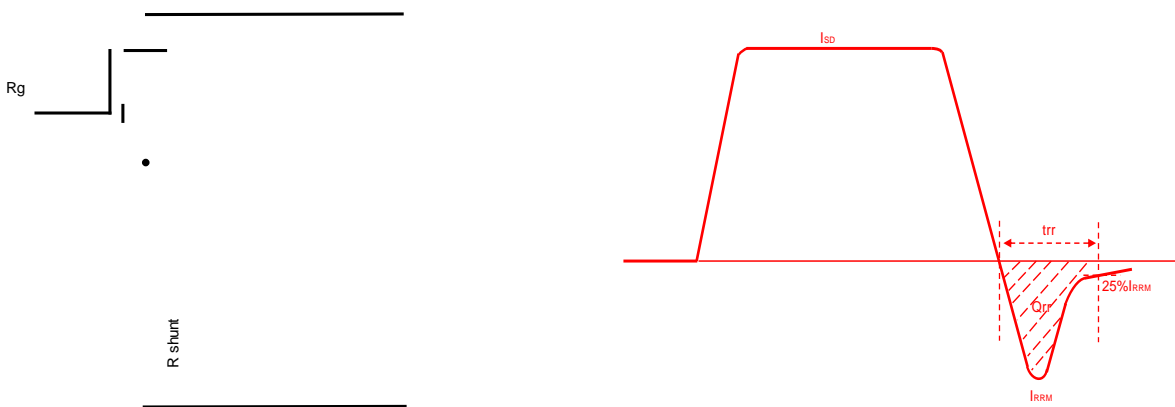
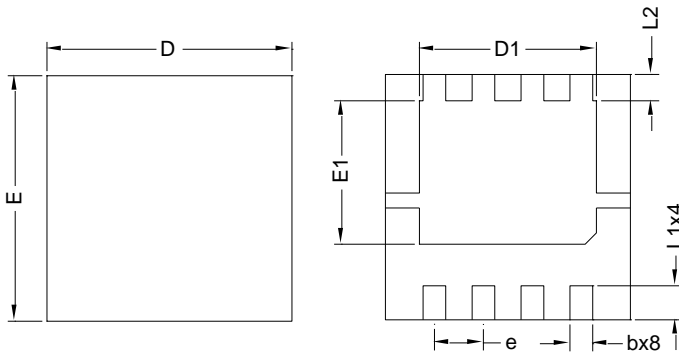


Figure D. Diode Recovery Test Circuit & Waveform



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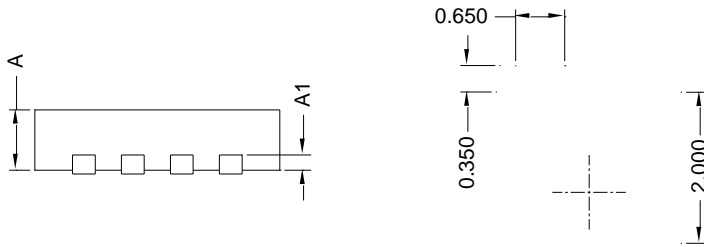
DFN3333-8L-A-0.8MM Package information



Top View

Bottom View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			



Side View

0.400

Suggested Solder Pad Layout
Top View

Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.10 mm.
 3. The pad layout is for reference purposes only.



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