



N-Channel Enhancement Mode Field Effect Transistor

Product Summary

V_{DS}	30V
I_D	50A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	6.0 mohm
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	7.0 mohm
100% EAS Tested	

General Description

Trench Power LV MOSFET technology
Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Moisture Sensitivity Level 3
Epoxy Meets UL 94 V-0 Flammability Rating
Halogen Free

Applications

High current load applications
Load switching
Hard switched and high frequency circuits
Uninterruptible power supply

Absolute Maximum Ratings ($T_A=25$ unless otherwise noted)

Parameter



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Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Static Parameter					
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D =250	30			V
Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			1	
Gate-Body Leakage Current	V _{GS} = ± 20V, V _{DS} =0V			± 100	nA
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	V _{GS} = 10V, I _D =15A		4.9	6.0	m
	V _{GS} = 4.5V, I _D =15A		5.9	7.0	
Diode Forward Voltage	I _S =20A, V _{GS} =0V			1.2	V
Maximum Body-Diode Continuous Current				50	A
Dynamic Parameters					
Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHZ		2504		pF
Output Capacitance			323		
Reverse Transfer Capacitance			283		
Gate resistance	F= 1MHZ		1.5		
Switching Parameters					
Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		54		nC
Gate-Source Charge			26		
Gate-Drain Charge			8.5		
Reverse Recovery Chrage	I _F =15A, di/dt=100A/us		10.2		
Reverse Recovery Time			15		
Turn-on Delay Time	V _{GS} =10V, V _{DD} =20V, I _D =2A R _{GEN} =3		11		ns
Turn-on Rise Time			20		
Turn-off Delay Time			41		



Typical Performance Characteristics

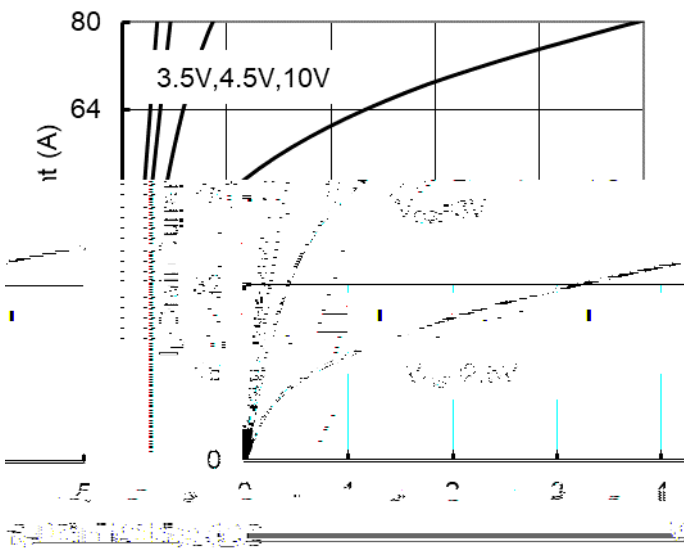


Figure1. Output Characteristics

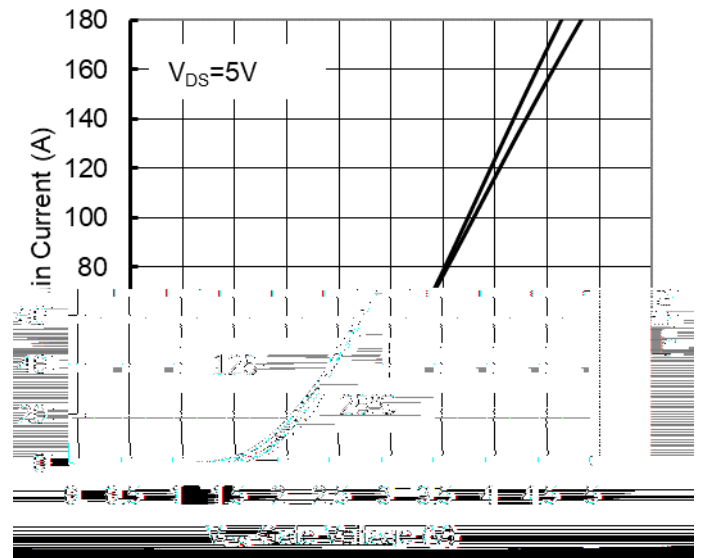


Figure2. Transfer Characteristics

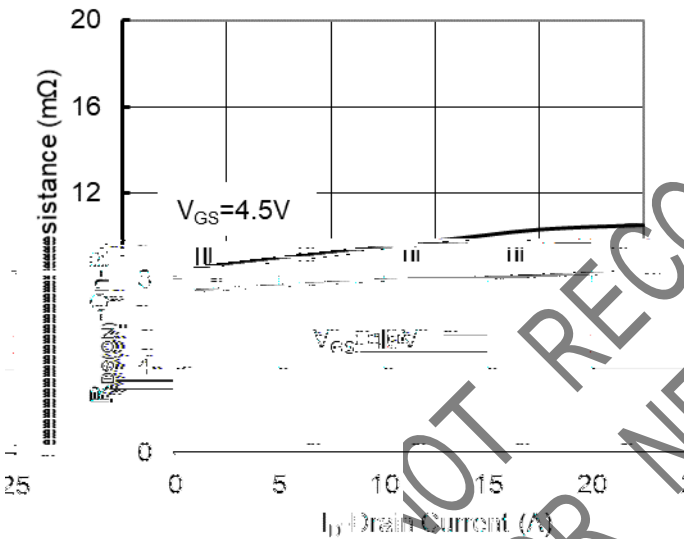


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

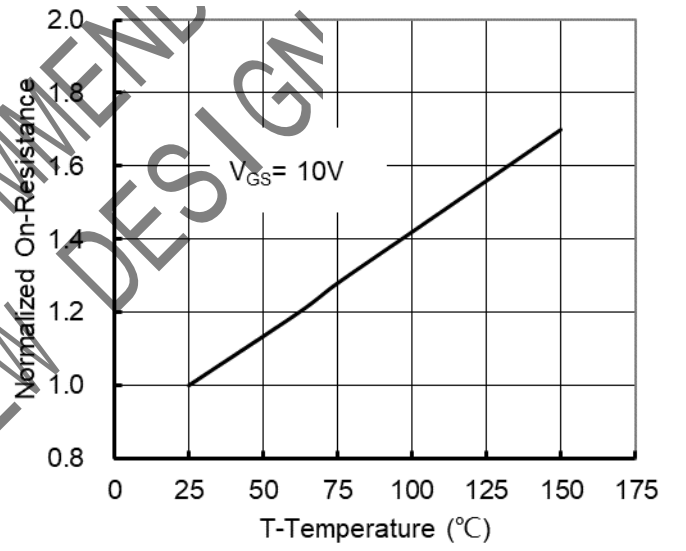


Figure 4: On-Resistance vs. Junction Temperature

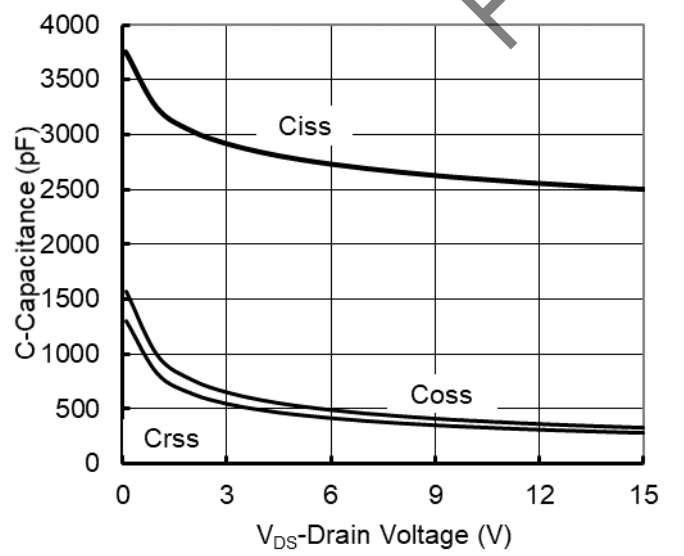


Figure5. Capacitance Characteristics

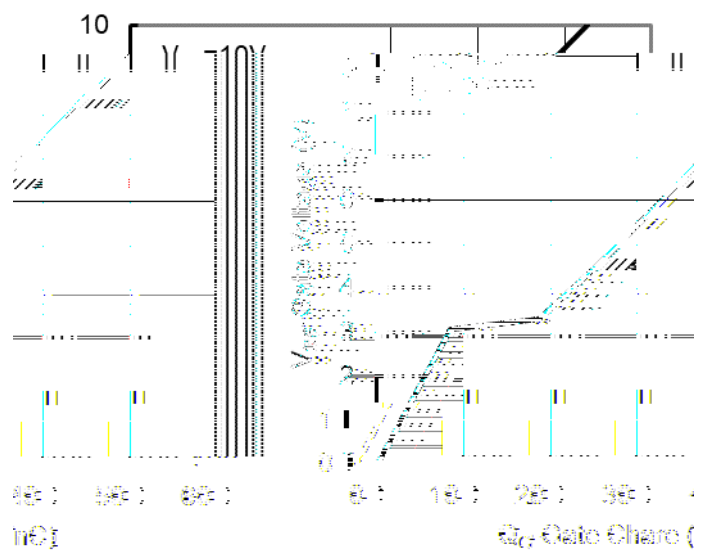


Figure6. Gate Charge

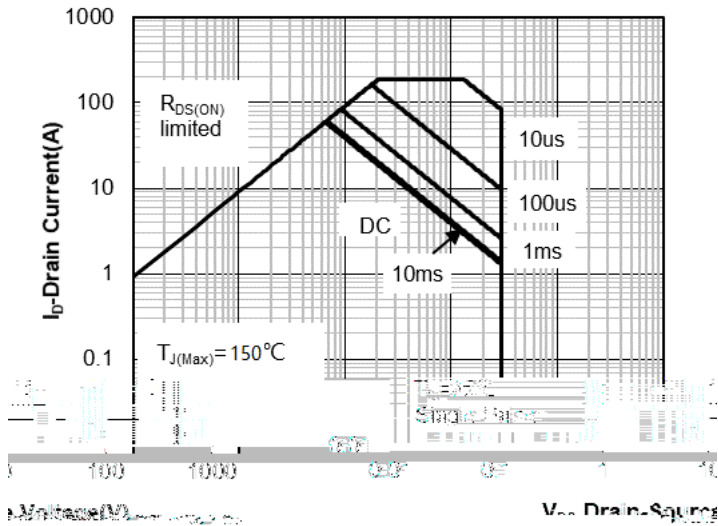


Figure7. Safe Operation Area

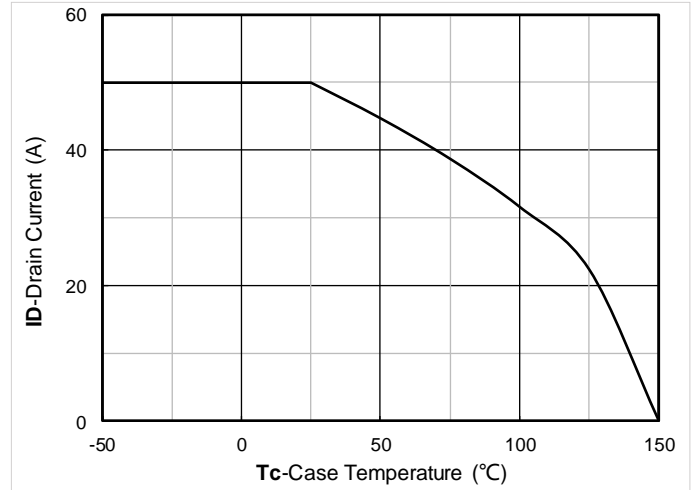


Figure8. Maximum Continuous Drain Current vs Case Temperature

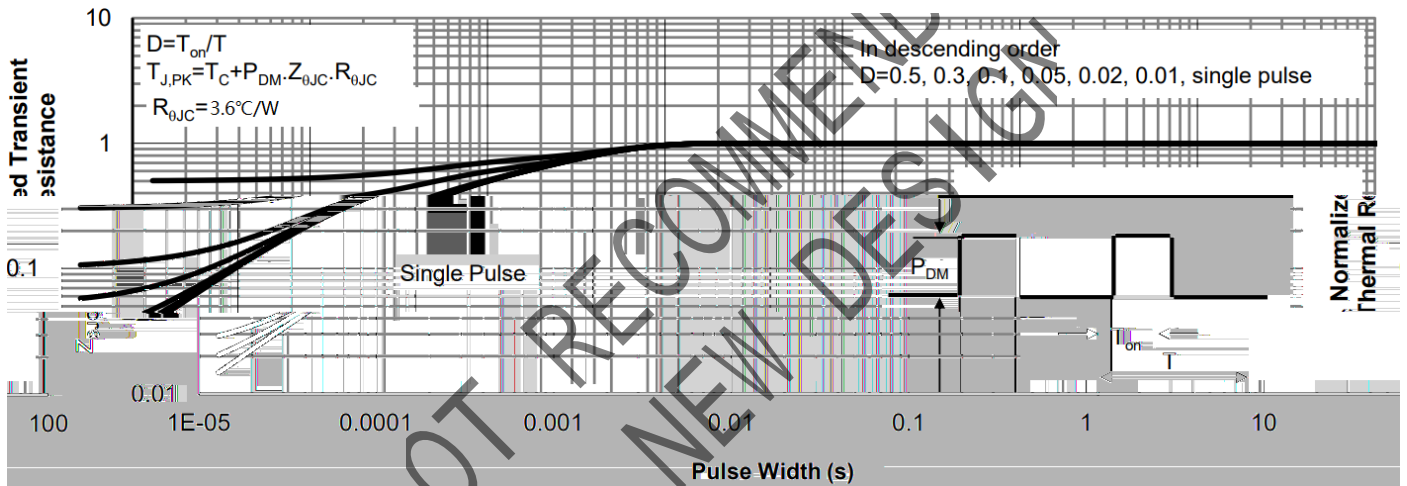


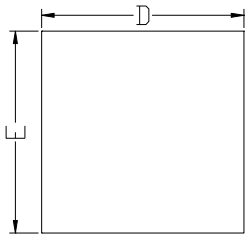
Figure9. Normalized Maximum Transient Thermal Impedance

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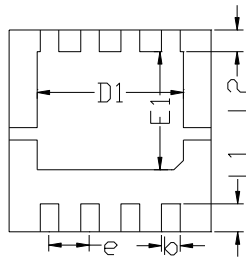
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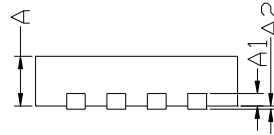
DFN3333-8L Package information



Top View

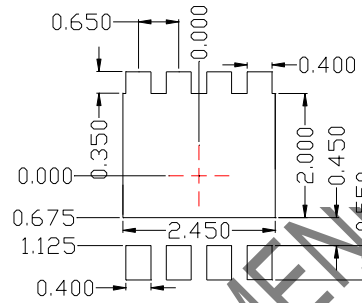


Bottom View



Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.

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